



Telecommunications Data Book

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DSTM	Memory Button™	Authorization Button™	Micro Monitor™
Dallastat	Touch Memory Probe™	Touch Pen™	Cyber Card™
Stick'Em Chip™	Certified Dallas Touch™	Time Button™	Cyber Key™
Button Holder™	UniqueWare™	Button Ready PC™	Soft Microcontroller™
Touch Memory EXecutive™	Dallas Registered™	MicroLan™	Secure Microcontroller™
TMEX™	Button™	ID Button™	Soft Silicon™
MultiButton™	Dallas Personal SignOn™	Dallas Protected Software™	All device numbers
TouchMemory Button™	Dallas SignOn™	Load & Lock™	

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557	D52291 T1 Loop Stick

GENERAL INFORMATION

PART NUMBER	DESCRIPTION	DATA BOOK
D80821	TMEX™ Professional Software Developer's Kit	Automatic Identification
D80830x	TMEX™ Performance Modules	Automatic Identification
D81000	5-Tap Silicon Delay Line	System Extension
D81003	4-Tap Silicon Delay Line for RISC Applications	System Extension
D81004	8-Tap High-Speed Silicon Delay Line	System Extension
D81005	5-Tap Silicon Delay Line	System Extension
D81007	7-Tap Silicon Delay Line	System Extension
D81010	10-Tap Silicon Delay Line	System Extension
D81015	2-to-1 Sub-Minimum Silicon Delay Line with Logic	System Extension
D81018	3-to-1 Silicon Delay Line	System Extension
D81020	Programmable 8-Bit Silicon Delay Line	System Extension
D81021	Programmable 8-Bit Silicon Delay Line	Supplement 4B5
D81033	3-to-1 Low-Voltage Silicon Delay Line	System Extension
D81035	3-to-1 High-Speed Silicon Delay Line	Supplement 4B5
D81040	Programmable One-Shot Pulse Generator	System Extension
D81044	4-to-1 High-Speed Silicon Delay Line	System Extension
D81045	4-Bit Dual Programmable Delay Line	System Extension
D81200	Serial RAM Chip	Timekeeping and NV RAM
D81201	Electronic Tag	Timekeeping and NV RAM
D81202, D81202S	Serial Timekeeping Chip	Timekeeping and NV RAM
D81204V	Electronic Key	Automatic Identification
D81205S	Multitap Chip	Automatic Identification
D81205V	Multitap	Automatic Identification
D81206	Phantom Serial Interface Chip	System Extension
D81207	TimeKey	Automatic Identification
D81210	Nonvolatile Controller Chip	Timekeeping and NV RAM
D81211	Nonvolatile Controller x 8 Chip	Timekeeping and NV RAM
D81212	Nonvolatile Controller x 16 Chip	Timekeeping and NV RAM
D81213B	SmartSocket 16Kx8K	Timekeeping and NV RAM
D81213C	SmartSocket 32K	Timekeeping and NV RAM
D81213D	SmartSocket 528Kx1M	Timekeeping and NV RAM
D81215	Phantom Time Chip	Timekeeping and NV RAM
D81216B	SmartWatchRAM 16Kx8K	Timekeeping and NV RAM
D81216C	SmartWatchRAM 64Kx32K	Timekeeping and NV RAM
D81216D	SmartWatchRAM 528Kx1M	Timekeeping and NV RAM
D81216E	SmartWatchROM 64Kx32K	Timekeeping and NV RAM
D81216F	SmartWatchROM 64Kx528Kx1M	Timekeeping and NV RAM
D81217A	Nonvolatile Read/Write Cache	Timekeeping and NV RAM
D81217M	Nonvolatile Read Write Cache	Timekeeping and NV RAM
D81218	Nonvolatile Controller	Timekeeping and NV RAM
D81220ABAD	16K Nonvolatile SRAM	Timekeeping and NV RAM
D81220V	16K Nonvolatile SRAM	Timekeeping and NV RAM
D81221	Nonvolatile Controller x 4 Chip	Timekeeping and NV RAM
D81222	BankSwitch Chip	System Extension
D81220ABAD	64K Nonvolatile SRAM	Timekeeping and NV RAM
D81225V	64K Nonvolatile SRAM	Timekeeping and NV RAM

PART NUMBER	DESCRIPTION	DATA BOOK
	for DS9092K	Automatic Identification
DS0621	TMEX™ Professional Software Developer's Kit	Automatic Identification
DS0630x	TMEX™ Performance Modules	Automatic Identification
DS1000	5-Tap Silicon Delay Line	System Extension
DS1003	4-Tap Silicon Delay Line for RISC Applications	System Extension
DS1004	5-Tap High-Speed Silicon Delay Line	System Extension
DS1005	5-Tap Silicon Delay Line	System Extension
DS1007	7-in-1 Silicon Delay Line	System Extension
DS1010	10-Tap Silicon Delay Line	System Extension
DS1012	2-in-1 Sub-Miniature Silicon Delay Line with Logic	System Extension
DS1013	3-in-1 Silicon Delay Line	System Extension
DS1020	Programmable 8-Bit Silicon Delay Line	System Extension
DS1021	Programmable 8-Bit Silicon Delay Line	Supplement 4/95
DS1033	3-in-1 Low-Voltage Silicon Delay Line	System Extension
DS1035	3-in-1 High-Speed Silicon Delay Line	Supplement 4/95
DS1040	Programmable One-Shot Pulse Generator	System Extension
DS1044	4-in-1 High-Speed Silicon Delay Line	System Extension
DS1045	4-Bit Dual Programmable Delay Line	System Extension
DS1200	Serial RAM Chip	Timekeeping and NV RAM
DS1201	Electronic Tag	Timekeeping and NV RAM
DS1202, DS1202S	Serial Timekeeping Chip	Timekeeping and NV RAM
DS1204V	Electronic Key	Automatic Identification
DS1205S	MultiKey Chip	Automatic Identification
DS1205V	MultiKey	Automatic Identification
DS1206	Phantom Serial Interface Chip	System Extension
DS1207	TimeKey	Automatic Identification
DS1210	Nonvolatile Controller Chip	Timekeeping and NV RAM
DS1211	Nonvolatile Controller x 8 Chip	Timekeeping and NV RAM
DS1212	Nonvolatile Controller x 16 Chip	Timekeeping and NV RAM
DS1213B	SmartSocket 16K/64K	Timekeeping and NV RAM
DS1213C	SmartSocket 256K	Timekeeping and NV RAM
DS1213D	SmartSocket 256K/1M	Timekeeping and NV RAM
DS1215	Phantom Time Chip	Timekeeping and NV RAM
DS1216B	SmartWatch/RAM 16K/64K	Timekeeping and NV RAM
DS1216C	SmartWatch/RAM 64K/256K	Timekeeping and NV RAM
DS1216D	SmartWatch/RAM 256K/1M	Timekeeping and NV RAM
DS1216E	SmartWatch/ROM 64K/256K	Timekeeping and NV RAM
DS1216F	SmartWatch/ROM 64K/256K/1M	Timekeeping and NV RAM
DS1217A	Nonvolatile Read/Write Cartridge	Timekeeping and NV RAM
DS1217M	Nonvolatile Read/Write Cartridge	Timekeeping and NV RAM
DS1218	Nonvolatile Controller	Timekeeping and NV RAM
DS1220AB/AD	16K Nonvolatile SRAM	Timekeeping and NV RAM
DS1220Y	16K Nonvolatile SRAM	Timekeeping and NV RAM
DS1221	Nonvolatile Controller x 4 Chip	Timekeeping and NV RAM
DS1222	BankSwitch Chip	System Extension
DS1225AB/AD	64K Nonvolatile SRAM	Timekeeping and NV RAM
DS1225Y	64K Nonvolatile SRAM	Timekeeping and NV RAM

PART NUMBER	DESCRIPTION	DATA BOOK
DS1350YLP/ABLPM	4096K Nonvolatile SRAM with	Timekeeping and NV RAM
DS1380	Power Monitors	Timekeeping and NV RAM
DS1381	RAMport	Timekeeping and NV RAM
DS1385/DS1387	NV RAMport	Timekeeping and NV RAM
DS1386	RAMified Real Time Clock 4K x 8	Timekeeping and NV RAM
DS1395/DS1397	RAMified Watchdog Timekeeper	Timekeeping and NV RAM
DS1401	RAMified Real Time Clock	Automatic Identification
DS1402	Front Panel Button Holder	Automatic Identification
DS1410D	Button Cable	Automatic Identification
DS1410K	Parallel Port Button Holder	Automatic Identification
DS1412	Parallel Holder Developer's Kit	Automatic Identification
DS1412K	Serial Port Button Holder	Automatic Identification
DS1414	Serial Holder Developer's Kit	Automatic Identification
DS1414K	Network Button Holder	Automatic Identification
DS1420	Authorization Button Developer's Kit	Automatic Identification
DS1422	Serial ID Button	Automatic Identification
DS1425	1Kbit Add—Only UniqueWare™ Button	Automatic Identification
DS1427	Multi Button™	Automatic Identification
DS14285/DS14287	Time Button™	Supplement 4/95
DS1485/DS1488	Real Time Clock with NVRAM Control	Timekeeping and NV RAM
DS1486	RAMified Real Time Clock 8K x 8	Timekeeping and NV RAM
DS1495/DS1497	RAMified Watchdog Timekeeper	Timekeeping and NV RAM
DS1585/DS1587	RAMified Real Time Clock	Timekeeping and NV RAM
DS1589/DS1593	Serialized Real Time Clocks	Timekeeping and NV RAM
DS1602	Serialized Real Time Clocks	Timekeeping and NV RAM
DS1603	Elapsed Time Counter	Timekeeping and NV RAM
DS1609	Elapsed Time Counter Module	Timekeeping and NV RAM
DS1610	Dual Port RAM	Timekeeping and NV RAM
DS1612	Partitioned NV Controller	Timekeeping and NV RAM
DS1613C	Lithium Battery Monitor	Timekeeping and NV RAM
DS1613D	Partitioned SmartSocket 256K	Timekeeping and NV RAM
DS1620	Partitioned SmartSocket 1M	Supplement 4/95
DS1621	Digital Thermometer and Thermostat	Supplement 4/95
DS1625	Digital Thermometer and Thermostat	Supplement 4/95
DS1630Y/AB,	Partitionable 256K NV SRAM	Timekeeping and NV RAM
DS1630YLP/ABLPM	PC Power Fail and Reset Controller	System Extension
DS1632	High-Speed Battery Recharger	System Extension
DS1633	High-Speed Battery Charger	Supplement 4/95
DS1633x	Personal Computer Power FET	System Extension
DS1640/DS1640C	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1642	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1643/DS1643LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1644/DS1644LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1645Y/AB,	Partitionable 1024K NV SRAM	Timekeeping and NV RAM
DS1645YLP/ABLPM	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1646/DS1646LPM	Nonvolatile Timekeeping RAM	Timekeeping and NV RAM
DS1647	Partitionable 4096K NV SRAM	Timekeeping and NV RAM
DS1650Y/AB,		
DS1650YLP/ABLPM		

PART NUMBER	DESCRIPTION	DATA BOOK
DS1651/DS1652	3-Code Lock/Key Match Memory System	System Extension
DS1652B	Code Memory Key	System Extension
DS1653/DS1652	4-Code Lock/Key Match Memory System	System Extension
DS1658Y/AB	Partitionable 128K x 16 NV SRAM	Timekeeping and NV RAM
DS1666, DS1666S	Audio Digital Resistor	System Extension
DS1667	Digital Resistor with OP AMP	System Extension
DS1668, DS1669, DS1669S	Dallastat™ Electronic Digital Rheostat	System Extension
DS1685/DS1687	3 Volt/5 Volt Real Time Clock	Supplement 4/95
DS1688/DS1691	3 Volt/5 Volt Serialized Real Time Clock	Supplement 4/95
DS1689/DS1693	5 Volt/3 Volt Serialized Real Time Clock	Supplement 4/95
DS1710	with NV RAM Control	Supplement 4/95
DS17285/DS17287	Partitioned NV Controller	Timekeeping and NV RAM
DS1730Y/YLPM	3 Volt/5 Volt Real Time Clock	Supplement 4/95
DS1745Y/YLPM	3 Volt Partitionable 256K NV SRAM	Timekeeping and NV RAM
DS17485/DS17487	3 Volt Partitionable 1024K NV SRAM	Timekeeping and NV RAM
DS1750Y/YLPM	3 Volt/5 Volt Real Time Clock	Supplement 4/95
DS1758Y	3 Volt Partitionable 4096K NV SRAM	Timekeeping and NV RAM
DS1801	3V Partitionable 128K x 16 NV SRAM	Timekeeping and NV RAM
DS1802	Dual Audio Taper Potentiometer	Supplement 4/95
DS1803	Dual Audio Taper Potentiometer	System Extension
DS1820	with Pushbutton Control	Supplement 4/95
DS1821	Addressable Dual Digital Potentiometer	Supplement 4/95
DS1830	1-Wire™ Digital Thermometer	Supplement 4/95
DS1832	Programmable Digital Thermostat	Supplement 4/95
DS1833	Programmable MicroMonitor	System Extension
DS1837	3.3 Volt MicroMonitor Chip	Supplement 4/95
DS1867	5V EconoReset	System Extension
DS1868	Quick Battery Recharger	System Extension
DS1869	Dual Digital Potentiometer with EEPROM	System Extension
DS1920	Dual Digital Potentiometer Chip	System Extension
DS1971	3V Dallastat™ Electronic Digital Rheostat	System Extension
DS1981U/DS1982U	Touch Thermometer™	Automatic Identification
DS1982	256-Bit EEPROM Touch Memory™	Automatic Identification
DS1985	UniqueWare™ Touch Memory	Automatic Identification
DS1986	1Kbit Add-Only Touch Memory™	Automatic Identification
DS1990A	16Kbit Add-Only Touch Memory™	Automatic Identification
DS1991L-F5A	64Kbit Add-Only Touch Memory™	Automatic Identification
DS1992/DS1993	Touch Serial Number™	Automatic Identification
DS1994	Touch MultiKey™	Automatic Identification
DS1995	1Kbit/4Kbit Touch Memory™	Automatic Identification
DS1996	4Kbit Plus Time Touch Memory™	Automatic Identification
DS2009	16Kbit Touch Memory™	Automatic Identification
DS2010	64Kbit Touch Memory™	Automatic Identification
DS2011	512 x 9 FIFO Chip	Timekeeping and NV RAM
DS2012	1024 x 9 FIFO Chip	Timekeeping and NV RAM
DS2013	2048 x 9 FIFO Chip	Timekeeping and NV RAM
DS2016	4096 x 9 FIFO Chip	Timekeeping and NV RAM
	8192 x 9 FIFO Chip	Timekeeping and NV RAM
	2K x 8 3V Operation Static RAM	Timekeeping and NV RAM

PART NUMBER
 DS2064
 DS21S07A
 DS2108
 DS2109
 DS211
 DS2110
 DS2112
 DS2130Q
 DS2132A/Q
 DS2141A
 DS21Q41B
 DS2143/DS2143Q
 DS21Q43A
 DS2151Q
 DS2153Q
 DS2164Q
 DS2165/DS2165Q
 DS2172
 DS2175
 DS2176
 DS2180A
 DS2181A
 DS2182A
 DS2186
 DS2187
 DS2188
 DS22B57
 DS222
 DS2223/DS2224
 DS2227
 DS2229
 DS2250(T)
 DS2251(T)
 DS2252(T)
 DS2282
 DS229
 DS2290
 DS2291
 DS232A
 DS233A
 DS2401
 DS2404
 DS2404S-C01
 DS2405
 DS2407
 DS2430A
 DS2434
 DS2435

DESCRIPTION
 8K x 8 3V Operation Static RAM
 SCSI Terminator
 Differential SCSI Switchable Terminator
 Plug and Play SCSI Terminator
 4 Driver/5Receiver RS-232 Serial Port
 Plug and Play SCSI Terminator with EEPROM
 BTL Terminator
 Voice Messaging Processor
 Digital Answering Machine Processor
 T1 Controller
 Quad T1 Framer
 E1 Controller
 Quad E1 Framer
 T1 Single-Chip Transceiver
 E1 Single-Chip Transceiver
 G.726 ADPCM Processor
 16/24/32Kbps ADPCM Processor
 Bit Error Rate Tester (BERT)
 T1/CEPT Elastic Store
 T1 Receive Buffer
 T1 Transceiver
 CEPT Primary Rate Transceiver
 T1 Line Monitor
 Transmit Line Interface
 Receive Line Interface
 T1/CEPT Jitter Attenuator
 32K x 8 Static RAM
 Dual RS-232 Transmitter/Receiver
 with Shutdown
 EconoRAM
 Flexible NV SRAM Stik
 Word-Wide 8 Meg SRAM Stik
 Soft Microcontroller
 128K Soft Microcontroller
 Secure Microcontroller
 T1 FDL Controller/Monitor Stik
 RS-232 Transmitter/Receiver
 T1 Isolation Stik
 T1 Long Loop Stik
 Dual RS-232 Transmitter/Receiver
 Dual RS-232 Transmitter/Receiver
 Silicon Serial Number
 EconoRAM Time Chip
 Dual Port Memory Plus Time
 Addressable Switch
 Dual Addressable Switch Plus 1K-Bit Memory
 256-Bit 1-Wire EEPROM
 Battery Identification Chip
 Battery Identification Chip
 with Time/Temperature Histogram

DATA BOOK
 Timekeeping and NV RAM
 Supplement 4/95
 Supplement 4/95
 Supplement 4/95
 PC Data Book
 PC Data Book
 Supplement 4/95
 Telecommunications
 Telecommunications
 Telecommunications
 Telecommunications
 Telecommunications
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 Telecommunications
 Telecommunications
 Timekeeping and NV RAM
 Supplement 4/95
 Automatic Identification
 Timekeeping and NV RAM
 Timekeeping and NV RAM
 Soft Microcontroller
 Soft Microcontroller
 Soft Microcontroller
 Telecommunications
 Supplement 4/95
 Telecommunications
 Telecommunications
 Supplement 4/95
 Supplement 4/95
 Automatic Identification
 Timekeeping and NV RAM
 Automatic Identification
 Automatic Identification
 Automatic Identification
 System Extension
 System Extension

PART NUMBER	DESCRIPTION	DATA BOOK
DS2501—UNW/DS2502—UNW	UniqueWare™ Add—Only Touch Memory	Automatic Identification
DS2502	1Kbit Add—Only Memory	Automatic Identification
DS2505	16Kbit Add—Only Memory	Automatic Identification
DS2506	64Kbit Add—Only Memory	Automatic Identification
DS5000(T)	Soft Microcontroller	Soft Microcontroller
DS5000FP	Soft Microcontroller Chip	Soft Microcontroller
DS5000TK	Evaluation Kit	Soft Microcontroller
DS5001FP	128K Soft Micro Chip	Soft Microcontroller
DS5002FP	Secure Micro	Soft Microcontroller
DS620x	CyberKey	Timekeeping and NV RAM
DS6417	CyberCard EV 4M—Bit NV SRAM	Timekeeping and NV RAM
DS9000	Bytewide Cable Harness	Timekeeping and NV RAM
DS9002	Cartridge Housing	Timekeeping and NV RAM
DS9003	Cartridge Proto Board	Timekeeping and NV RAM
DS908xx	CyberKey/Card Receptacles	Timekeeping and NV RAM
DS9091K	1—Wire™ MicroLAN™ Evaluation Kit	Automatic Identification
DS9092	Touch Memory Probe	Automatic Identification
DS9092K	Touch Memory Starter Kit	Automatic Identification
DS9092R	Touch Port	Automatic Identification
DS9093x	Touch Memory Mount Products	Automatic Identification
DS9094	MicroCan Clip	Automatic Identification
DS9096P	Touch Memory Adhesive Pads	Automatic Identification
DS9097/DS9097E	Touch COM Port Adapter	Automatic Identification
DS9098	MicroCan Retainer	Automatic Identification
DS9100	Touch and Hold Probe Stampings	Automatic Identification
DS9101	Multi—Purpose Clip	Automatic Identification
DS9103K	Touch Memory Access Control Demo Kit	Automatic Identification

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2130	28-Pin DIP	0 to +70	DS2130	
	28-Pin DIP	-40 to +85	DS2130N	
	28-Pin PLCC	0 to +70	DS2130Q	
	28-Pin PLCC	-40 to +85	DS2130QN	
DS2132A	28-Pin DIP	0 to +70	DS2132A	
	28-Pin DIP	-40 to +85	DS2132AN	
	28-Pin PLCC	0 to +70	DS2132AQ	
	28-Pin PLCC	-40 to +85	DS2132AQN	
DS2141A	40-Pin DIP	0 to +70	DS2141A	
	40-Pin DIP	-40 to +85	DS2141AN	
	44-Pin PLCC	0 to +70	DS2141AQ	
	44-Pin PLCC	-40 to +85	DS2141AQN	
DS21Q41B	128-Pin TQFP	0 to +70	DS21Q41BT	
	128-Pin TQFP	-40 to +85	DS21Q41BTN	
DS2143	40-Pin DIP	0 to +70	DS2143	
	40-Pin DIP	-40 to +85	DS2143N	
	44-Pin PLCC	0 to +70	DS2143Q	
	44-Pin PLCC	-40 to +85	DS2143QN	
DS21Q43A	128-Pin TQFP	0 to +70	DS21Q43AT	
	128-Pin TQFP	-40 to +85	DS21Q41ATN	
DS2151	44-Pin PLCC	0 to +70	DS2151Q	
	44-Pin PLCC	-40 to +85	DS2151QN	
DS2153	44-Pin PLCC	0 to +70	DS21453Q	
	44-Pin PLCC	-40 to +85	DS2153QN	
DS2164	28-Pin PLCC	0 to +70	DS2164Q	
	28-Pin PLCC	-40 to +85	DS2164QN	
DS2165	24-Pin DIP	0 to +70	DS2165	
	24-Pin DIP	-40 to +85	DS2165N	
	28-Pin PLCC	0 to +70	DS2165Q	
	28-Pin PLCC	0 to +70	DS2165QL	3 Volt
	28-Pin PLCC	-40 to +85	DS2165QN	
DS2172	32-Pin TQFP	0 to +70	DS2172T	
	32-Pin TQFP	-40 to +85	DS2172TN	
DS2175	16-Pin DIP	0 to +70	DS2175	
	16-Pin DIP	-40 to +85	DS2175N	
	16-Pin SOIC	0 to +70	DS2175S	
	16-Pin SOIC	-40 to +85	DS2175SN	
DS2176	24-Pin DIP	0 to +70	DS2176	
	24-Pin DIP	-40 to +85	DS2176N	
	28-Pin PLCC	0 to +70	DS2176Q	
	28-Pin PLCC	-40 to +85	DS2176QN	
DS2180A	40-Pin DIP	0 to +70	DS2180A	
	40-Pin DIP	-40 to +85	DS2180AN	
	44-Pin PLCC	0 to +70	DS2180AQ	
	44-Pin PLCC	-40 to +85	DS2180AQN	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2181A	40-Pin DIP	0 to +70	DS2181A	
	40-Pin DIP	-40 to +85	DS2181AN	
	44-Pin PLCC	0 to +70	DS2181AQ	
	44-Pin PLCC	-40 to +85	DS2181AQN	
DS2182A	28-Pin DIP	0 to +70	DS2182A	
	28-Pin DIP	-40 to +85	DS2182AN	
	28-Pin PLCC	0 to +70	DS2182AQ	
	28-Pin PLCC	-40 to +85	DS2182AQN	
DS2186	20-Pin DIP	0 to +70	DS2186	
	20-Pin DIP	-40 to +85	DS2186N	
	20-Pin SOIC	0 to +70	DS2186S	
	20-Pin SOIC	-40 to +85	DS2186SN	
DS2187	18-Pin DIP	0 to +70	DS2187	
	20-Pin SOIC	0 to +70	DS2187S	
DS2188	16-Pin DIP	0 to +70	DS2188	
	16-Pin DIP	-40 to +85	DS2188N	
	16-Pin SOIC	0 to +70	DS2188S	
	16-Pin SOIC	-40 to +85	DS2188SN	
DS2282	STIK	0 to +70	DS2282	
DS2290	STIK	0 to +70	DS2290	
DS2291	STIK	0 to +70	DS2291	

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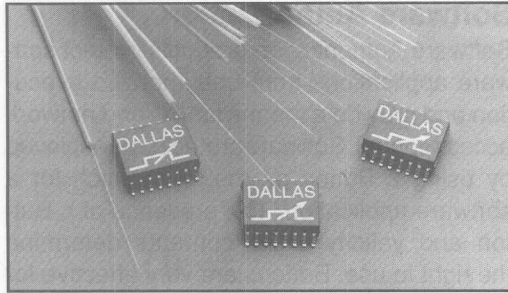
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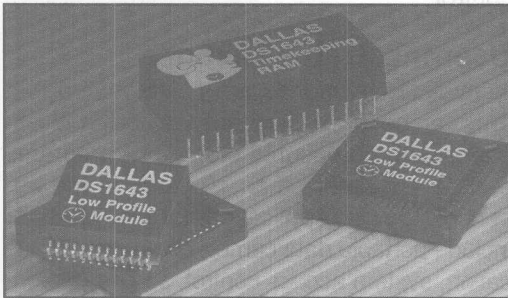
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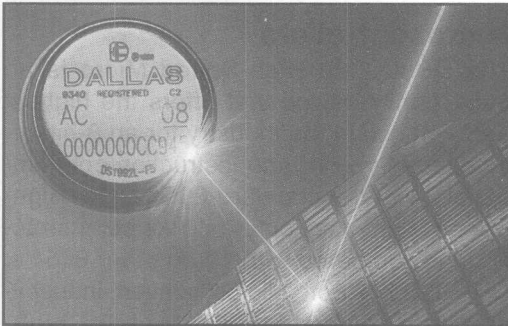
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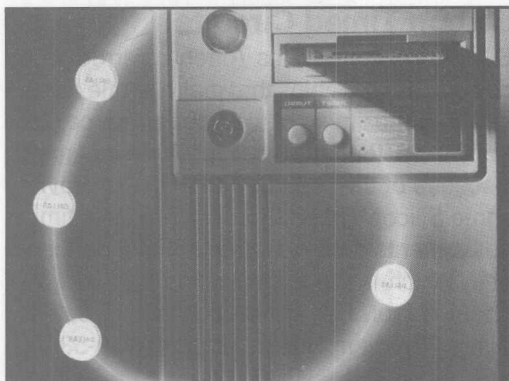
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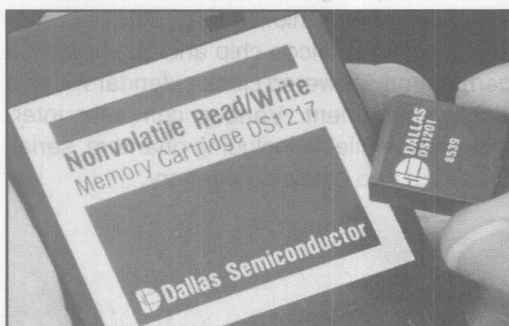
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Touch Memory™ is a self-stick, Silicon Label™ in a stainless steel can. This MicroCan™ provides all the advantages canning has to offer, such as low cost, ruggedness, and the ability to preserve contents. The MicroCan's greatest advantage, however, is that a standalone chip can leave the confines of the computer and travel virtually anywhere to bring digital data to the point of use. Information can be updated time after time while the label is still affixed to its object. Wherever the silicon-labelled object goes, information is served up on the spot without recourse to remote networks. This family also includes low-cost memory chips in T0-92 packages.



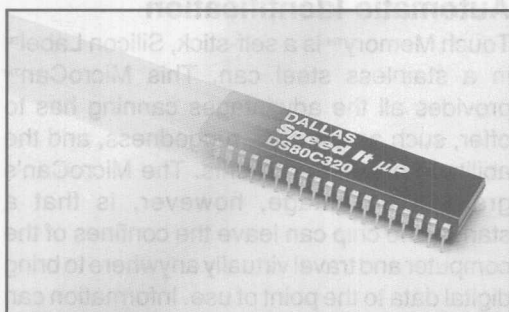
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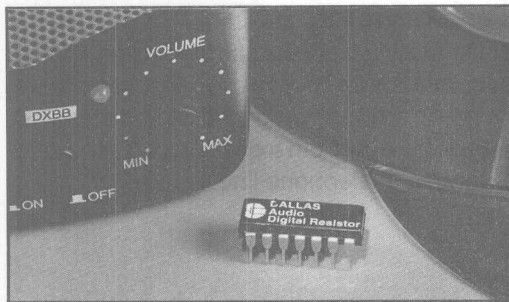
User-Insertable Memory

Nonvolatile memories are packaged so that they can be simply plugged in. A built-in lithium energy source ensures storage of programs and data for more than 10 years in the absence of power. Applications for such products include portable data carrier, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work records. All products can be read or written by a PC.



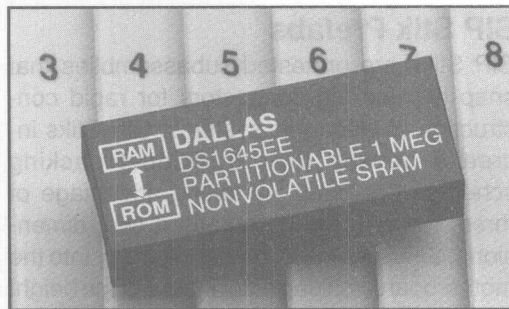
Microcontrollers

The DS80C320 High-Speed Micro is an 8051 family device that offers the highest performance in the industry for an 8-bit microcontroller. Pin- and instruction set-compatible with the standard 80C32, the High-Speed Micro uses only 4 clocks per instruction, as compared with 12 on other 8051's. Our DS500x Soft Micros convert industry-standard byte-wide SRAM into high-performance, nonvolatile read/write storage.



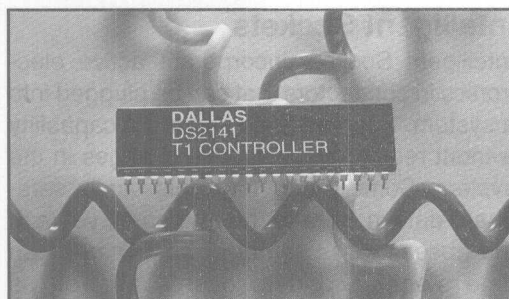
System Extension

These products add a variety of special features to systems without encumbering design. A digital potentiometer is an all-silicon version of an electrical element used in almost all electronic equipment. CPU supervisors monitor vital conditions for a microprocessor. Digital Thermometers measure temperature and directly output a digital number.



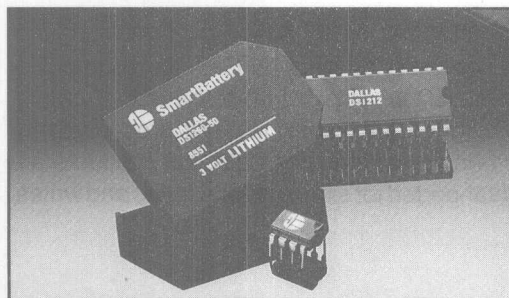
Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for more than 10 years in the absence of main power.



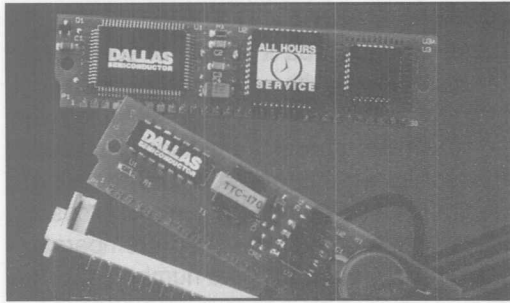
Telecommunications

A comprehensive product family addresses the requirements of high-speed, digital voice/data transmission and monitoring in T1, CEPT, or Primary Rate ISDN networks. The DS2151/53 T1/E1 Single-Chip Transceivers combine all the circuitry needed to connect to a T1 or E1 line in a single package.



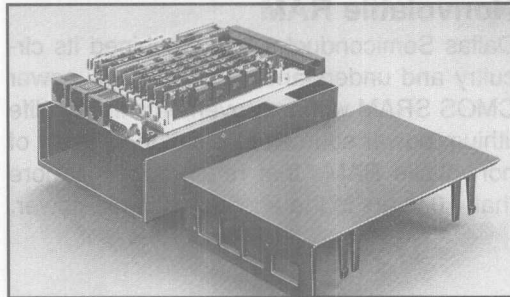
Battery Backup & Chargers

The Battery Backup chip set crashproofs microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred. Battery Chargers contain all the circuitry needed to recharge a 3-cell NiCad or lithium battery pack in a 3-pin package.



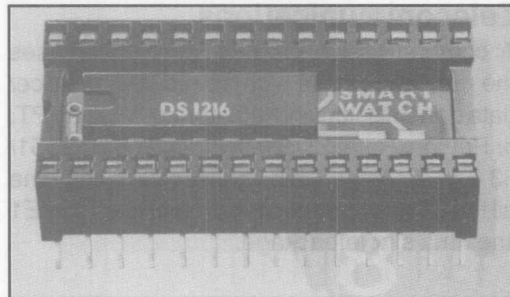
Teleservicing

Teleservicing products can monitor equipment performance 24 hours a day, release software revisions, perform diagnostics, and make adjustments — all from a desktop computer over an ordinary telephone line.



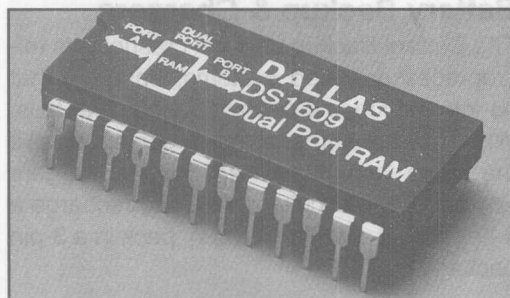
SIP Stik Prefabs

SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.



Intelligent Sockets

Intelligent Sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.



Multiport Memory

A complete family of FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out processing for storing and retrieving data, the products are dual-ported for simultaneous reads and writes.

Dallas Semiconductor Corporation designs, manufactures, and markets electronic chips and chip-based subsystems. Founded in 1984, the Company uses customer problems as an entry point to develop products with widespread applications. The Company is committed to new product development as a means to increase future revenues and to diversify its markets, products, and customers.

Advanced technologies have given the Company a competitive edge over traditional approaches to semiconductors. Combining lithium energy cells with low-power CMOS chips powers chips for the useful life of the equipment. Direct laser writing enhances chip capabilities with high levels of precision and unique identities.

In its 11-year history, Dallas Semiconductor has developed 215 base products with over 1,000 variations shipped to more than 8,000 customers worldwide. A direct sales force and distribution network sell to original equipment manufacturers (OEMs) in personal computers and workstations, scientific and medical equipment, industrial controls, automatic identification, telecommunications, consumer electronics, and other markets.

Sales for 1994 totaled \$181,432,000. Dallas Semiconductor has 850 employees. On March 19, 1990, the Company started trading on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions—dynamic, flexible, chip-based products that can be molded in the final manufacturing stages or during use. Soft Silicon is made possible by lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks (snap-in subassemblies) are made virtually crashproof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having similar design. Direct laser writing allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

As of January 1, 1995, the Company owns 342,500 square feet of building space and 22.9 acres of land in Dallas. The Company's wafer fabrication facility is a model of efficiency. In order to add capacity for growth the Company built a new advanced wafer fabrication facility that began production in 1994. The new fab is an important asset in terms of its capacity and process capabilities.

QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSES

- *Incoming Quality Control (IQC):* Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL-STD-105.
- *In-Process Inspections:* Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- *Statistical Process Control (SPC):* Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- *In-Process Sample Tests:* In order to guarantee the accuracy and completeness of in-process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL-STD-105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state-of-the-art environmental facility allows accelerated stresses to be performed and monitored in-house. In addition, a metallurgical laboratory has been equipped to perform real-time x-ray, x-ray fluorescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer-based tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production-ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- *Prototype or Engineering Sample:* Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- *Prequal:* Prequal products meet prototype requirements and are characterized to all data sheet limits. Final test and all processes used to manufacture the product are stable and under manufacturing control. Qualification of the product has started.
- *Fully Qualified:* Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

Tables 1, 2 and 3 list the tests which a Dallas Semiconductor product must pass in order to be classified as fully qualified.

RELIABILITY MONITOR PROGRAM

In order to maintain continuous qualification status on all products, Dallas Semiconductor has implemented an extensive Reliability Monitor Program (RMP). The RMP monitors all design, wafer fabrication, and assembly processes in the qualified products database. Product is selected monthly from finished goods and subjected to a series of reliability tests similar to those used in the original qualification. Any failures generated from these tests require analysis to root cause and corrective action.

Data from the RMP is published quarterly and is available on demand.

FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUIT PRODUCTS Table 1

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Infant Life	125°C, 7.0V	48 Hr.	0.3%
High Temperature Operating Life	125°C, 5.5V	1000 Hr.	*0.4%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Voltage Life	125°C, 7.0V	1000 Hr.	*0.4%
High Temperature Storage	150°C, No Bias	1000 Hr.	2.0%
Temperature Humidity Bias	85°C/85% RH, 5.5V	1000 Hr.	1.0%
Autoclave	121°C, 2 ATM Steam, Unbiased	168 Hr.	1.5%
Temperature Cycle	-55°C to +125°C	1000 cycle	1.0%
X-Ray	MIL-STD-883 Method 2012		15%
Bond Pull	MIL-STD-883 Method 2011	Premold	1.5%
Dimensions	MIL-STD-883 Method 2016		15%
Lead Integrity	MIL-STD-883 Method 2004		3.0%
Solderability	MIL-STD-883 Method 2003	8 Hr. Steamage	3.0%
ESD	MIL-STD-883 Method 3015		> ±1000 volts
Latch-up	JEDEC Std. 17		> 100 mW/pin

* Combined high voltage life and operating life requirement.

FULL QUALIFICATION REQUIREMENTS FOR MODULE PRODUCTS Table 2

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Temperature Storage	85°C, No Bias	1000 Hr.	2.0%
*Temperature Humidity Bias	85°C/85% RH, 5.5V	959 Hr.	1.0%
Temperature Cycle	-40°C to +85°C	1000 cycle	1.0%
X-Ray	MIL-STD-883 Method 2012		15%
Dimensions	MIL-STD-883 Method 2016		15%
Lead Integrity	MIL-STD-883 Method 2004		3.0%
Solderability	MIL-STD-883 Method 2003	8 Hr. Steamage	3.0%

* Selected products.

FULL QUALIFICATION REQUIREMENTS FOR SIP STICK AND TOUCH MEMORY PRODUCTS Table 3

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
High Temperature Storage	85°C, No Bias	1000 Hr.	7.0%
Temperature Humidity	60°C/90% RH	288 Hr.	7.0%
Temperature Cycle	-40°C to +85°C	500 cycle	7.0%

CONCLUSIONS

DALLAS

SEMICONDUCTOR

DS2130Q

Voice Messaging Processor

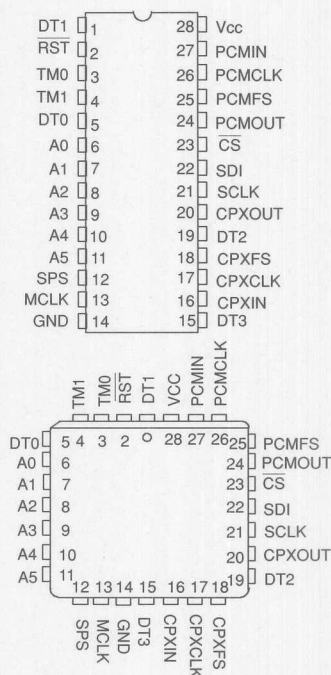
FEATURES

- Per-channel voice messaging processor for digitized voice storage and retrieval
- High fidelity speech recording and playback at 8, 12, 16, 24 and 32 Kbits/sec
- Integral DTMF transceiver for remote touch-tone control and dialing
- Connects to popular PCM codec/filters for analog interfacing
- Direct PCM serial data bus interfaces to any of 32 possible TDM time slots
- Monitors and reports audio energy levels for call progress and voice detection
- Selectable beep generator for sound prompts
- 3-wire synchronous serial control port
- 28-pin DIP or PLCC (DS2130Q) packages

DESCRIPTION

The DS2130 Voice Messaging Processor is a CMOS DSP processor that serves as a voice messaging engine for digitized voice storage and retrieval applications. It offers half-duplex speech compression or expansion at either 8, 12, 16, 24 or 32 Kbits/sec. The advanced speech compression algorithm maintains excellent audio clarity even at low bit rates. The algorithm also incorporates a DTMF transceiver for decoding or generating touch-tone signals for remote control and automatic dialing. The tone generator can be used to create single-tone beeps used in popular answering machines. Voice and call progress detection can be easily implemented using the energy threshold detect outputs.

PIN ASSIGNMENT

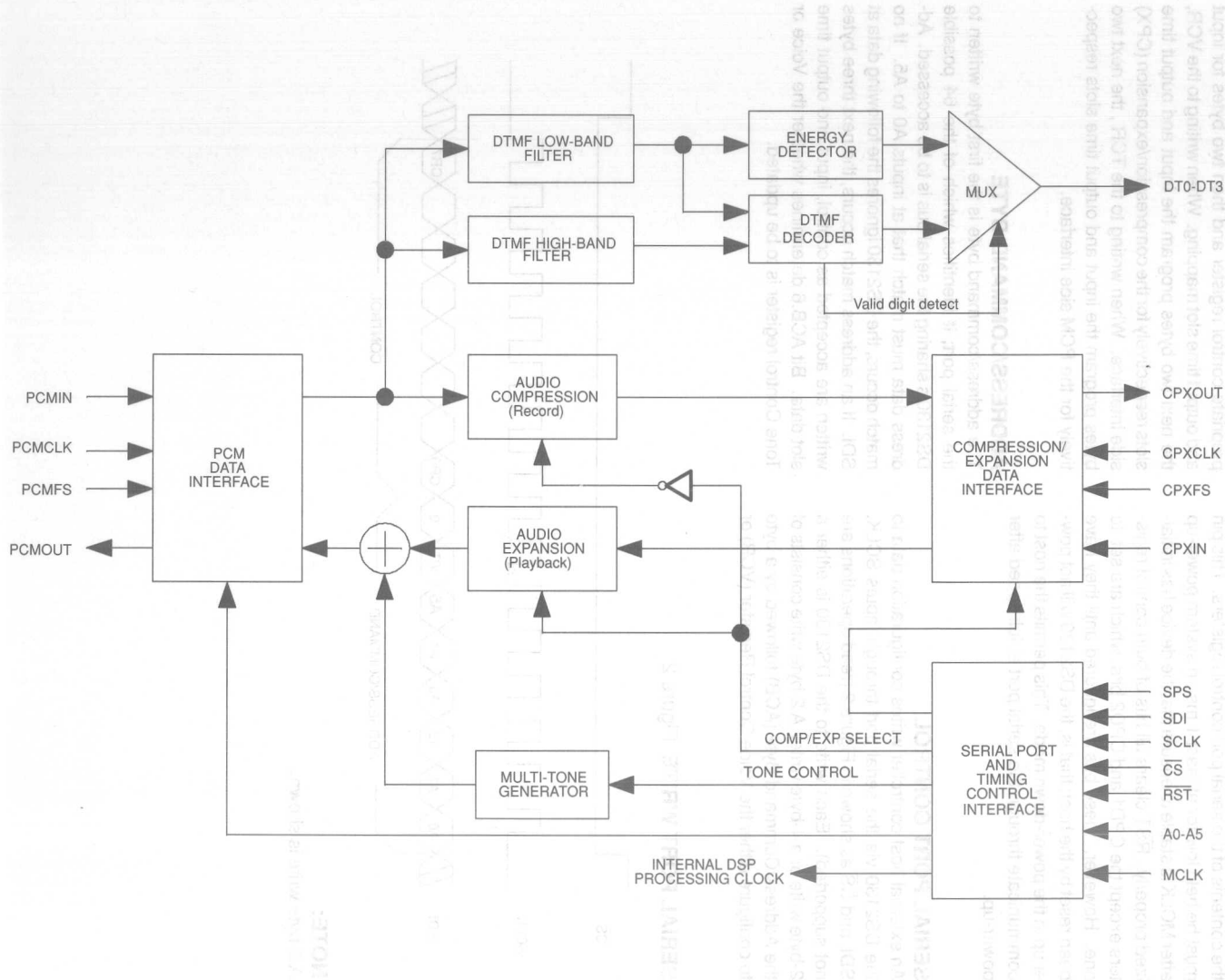


PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
5	DT0	O	Detect outputs 0-3. These are the four output detect lines that report energy threshold levels and DTMF tones. DTMF tone detection always has precedence over energy level reporting.
1	DT1	O	
19	DT2	O	
15	DT3	O	
2	RST	I	Reset input. When this pin is low, the internal DSP algorithm is in a reset state for proper initialization. The DS2130 should always be reset for at least 1 ms after each power-up occurrence.
3	TM0	I	Test mode pins. These pins are used for factory testing and must be tied to GND for proper operation.
4	TM1	I	
6	A0	I	Address Select. Provides serial address ID of the DS2130. The states of A0-A5 must match the address sent in the command byte to enable the serial port. A0 = LSB.
7	A1	I	
8	A2	I	
9	A3	I	
10	A4	I	
11	A5	I	
12	SPS	I	Serial Port Select. This pin must be tied to V_{CC} for proper operation of the serial port. The hardware mode is <u>not</u> supported on the DS2130.
13	MCLK	I	Master processing clock. This is the clock used for the internal DSP engine and should be in the range of 10.5 - 13 MHz. MCLK can be asynchronous to any other clock signal on the DS2130. The duty cycle should be nominally 50%.
14	GND	-	Ground. Tie this pin to the system logic ground.
16	CPXIN	I	Compressed data in. This is the serial data input for the compressed audio data sampled on falling edges of CPXCLK during selected time slots. This data is expanded to 8-bit PCM that is output on PCMOUT except in PCM bypass mode.
17	CPXCLK	I	Compression/expansion side data clock. This is the clock used to sample data at CPXIN, to output data at CPXOUT and to determine the proper time slot. CPXCLK must be synchronous with CPXFS. See "Special Clock Requirements" section for more details.
18	CPXFS	I	Compression/expansion side frame sync. This input must be an 8 KHz clock for proper operation. CPXFS must be the same frequency as PCMFS (normally they are tied together).
20	CPXOUT	O	Compressed data out. This is the serial data output for the compressed audio data, updated on rising edges of CPXCLK during selected time slots.
21	SCLK	I	Serial port clock. This is the clock used to write configuration data to the serial port registers.
22	SDI	I	Serial data input. Data source for the serial port registers.
23	CS	I	Chip select input. This pin must transition high to low before each write operation to the serial port.
24	PCMOUT	O	PCM output. This is the output for expanded data which is in the standard 8-bit PCM u/A-law format. Data is updated on rising edges of PCMCLK.

PIN	SYMBOL	TYPE	DESCRIPTION
25	PCMFS	I	PCM side frame sync. An 8 KHz clock signal must be applied for the PCM data interface. Lower sample rates can be used to reduce the effective bit rate but may result in unusable DTMF detection and generation as well as lower voice quality. PCMFS is normally tied to CPXFS.
26	PCMCLK	I	PCM side data clock. This is the clock used to sample PCM serial data at PCMIN, to output data at PCMOUT and to determine the proper time slot. PCMCLK must be synchronous with PCMFS.
27	PCMIN	I	PCM data input. This is the input for the 8-bit serial PCM data which would normally be supplied by a codec/filter device. Data is sampled on falling edges of PCMCLK.
28	V _{CC}	-	Positive supply input. Tie to system +5 volt supply.
29	PCMAX	O	PCM w/4-law format. Data is updated on rising edges of PCMCLK.
30	CPXOUT	O	Compressed data out. This is the serial data output for the compressed audio data, updated on rising edges of CPXCLK during selected time slots.
31	SCLK	I	Serial port clock. This is the clock used to write configuration data to the serial port register.
32	SDI	I	Serial data input. Data source for the serial port register.
33	CS	I	Chip select input. This pin must transition high to low before each write operation to the serial port.
34	PCMOUT	O	PCM output. This is the output for expanded data which is in the standard 8-bit PCM w/4-law format.
35	CPXCLK	I	Compressed data clock. This is the clock used to sample data at CPXIN, to output data at CPXOUT and to determine the proper time slot. CPXCLK must be synchronous with CPXFS. See "Special Clock Requirements" section for more details.
36	CPXFS	I	Compressed data frame sync. This input must be an 8 KHz clock for proper operation. CPXFS must be the same frequency as PCMFS (normally they are tied together).
37	GROUND	-	Ground. Tie this pin to the system logic ground.
38	MCLK	I	Master processing clock. This is the clock used for the internal DSP engine and should be in the range of 10.5 - 13 MHz. MCLK can be asynchronous to any other clock signal on the DS2130. The duty cycle should be nominally 50%.
39	SPS	I	Serial Port Select. This pin must be tied to V _{CC} for proper operation of the serial port. The hardware mode is not supported on the DS2130.
40	A5	I	Address bit 5. Must match the address sent in the command byte to enable the serial port.
41	A4	I	Address bit 4.
42	A3	I	Address bit 3.
43	A2	I	Address bit 2.
44	A1	I	Address bit 1.
45	A0	I	Address bit 0.

DS21300 SIGNAL FLOW DIAGRAM Figure 1



HARDWARE RESET

RST allows the host to reset the DSP algorithms and the contents of the serial port control registers. This pin must be held low for at least 1 ms on system power-up after MCLK is stable to ensure that the device has initialized properly. $\overline{\text{RST}}$ clears all bits of both control registers except the CPD1 and CPD2 bits, which are set to one. However, these bits are ignored until they have been reset by the host; that is, the DS2130 will not power up in the power-down mode. This permits the host to communicate through the serial port at full speed after power-up.

SERIAL PORT CONTROL

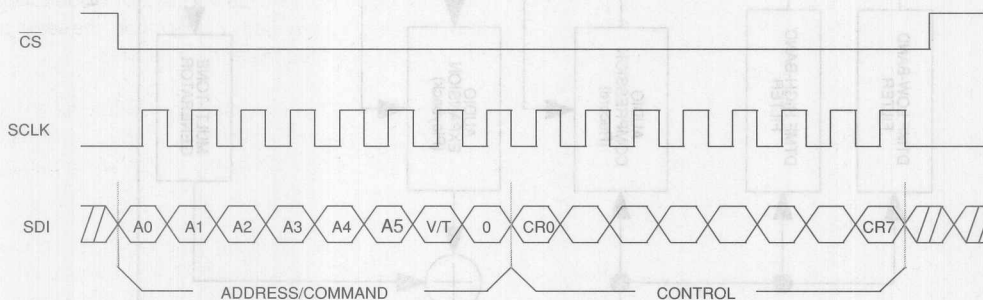
An external host controller writes configuration data to the DS2130 via the serial port through inputs SCLK, SDI, and CS as shown in Figure 2 (read operations are not supported). Each write to the DS2130 is either a 2-byte write or a 4-byte write. A 2-byte write consists of the Address/Command Byte (ACB) followed by a byte to configure either the Voice Control Register (VCR) or

the Tone Control Register (TCR). The 4-byte write consists of the ACB followed by a byte to configure the appropriate control register and then two bytes for input and output time slot mapping. When writing to the VCR, the next two bytes program the input and output time slots respectively for the compression/expansion (CPX) side interface. When writing to the TCR, the next two bytes program the input and output time slots respectively for the PCM side interface.

ADDRESS/COMMAND BYTE

The address/command byte is the first byte written to the serial port; it identifies which of the 64 possible DS2130's sharing the serial bus is to be accessed. Address data must match that at inputs A0 to A5. If no match occurs, the DS2130 ignores the following data at SDI. If an address match occurs, the next three bytes written are accepted as control, input and output time slot data. Bit ACB.6 determines whether the Voice or Tone Control register is to be updated.

SERIAL PORT WRITE Figure 2



NOTE:

A 2-byte write is shown.

(MSB)				(LSB)			
CXS3	V/T	A5	A4	A3	A2	A1	A0
SYMBOL	POSITION	NAME AND DESCRIPTION					
-	ACB.7	Reserved; must be zero for proper operation.					
V/T	ACB.6	Voice/Tone command byte select. 0 = write to Tone Generator Control register 1 = write to Voice Control register					
A5	ACB.5	MSB of Device Address.					
A4	ACB.4						
A3	ACB.3						
A2	ACB.2						
A1	ACB.1						
A0	ACB.0	LSB of Device Address.					

VOICE CONTROL REGISTER

The Voice Control Register (VCR) determines the compression/expansion bit rate and PCM data format. It also provides power-down and algorithm reset control.

The u/A bit selects either μ -law or A-law PCM data encoding for PCMIN and PCMOUT pins. When u/A = 1, μ -Law is selected; when u/A = 0, A-Law is selected.

Compression or expansion bit rates are determined by bits CXS1, CXS2 and CXS3. See Table 2 for the mapping of these bits. For the reduced bandwidth modes, the incoming PCM data is internally filtered with a 1.7 KHz low-pass and sampled at one-half of the CPXFS/PCMFS frequency. The PCM Bypass mode (CXS1=1, CXS2=0 and CXS3=1) permits input PCM data at either PCMIN or CPXIN to be routed out to CPXOUT or PCMOUT respectively, bypassing normal compression/expansion.

Voice compression/expansion can be disabled by setting CPD1 to a 1. In this mode, the compression/expansion algorithm is idled and CPXOUT is tri-stated. This

mode should be used when only DTMF/tone generation and detection are desired. When CPD1 and CPD2 (CPD2 is in the Tone Control register) are both equal to a 1, the device enters a low-power standby mode in which all DSP operation is halted. *In this mode, the serial port must not be operated faster than 39 KHz.*

CPXRST resets the algorithm coefficients for the expansion/compression algorithm to their initial values. CPXRST will be cleared by the device when the algorithm reset is complete.

The compression/expansion loopback feature is enabled when CXLB is set and CPD1 is cleared. During this loopback, no expansion or compression occurs and input data at CPXIN is looped back to the appropriate time slot at CPXOUT.

Compression or expansion operation is selected via the CP/EX bit (the DS2130 cannot perform both simultaneously).

NOTE:

These reduced bandwidth modes use an internal low-pass filter at 1.7 KHz to permit a lower bit rate. The normal bandwidth otherwise is 300 Hz to 3.4 KHz due to the filters typically present in the codec-filter device used with the DS2130.

VOICE CONTROL REGISTER Figure 4

(MSB)				(LSB)			
CP/EX	CXS1	CPD1	CXRST	CXLB	U/A	CXS2	CXS3
SYMBOL	POSITION	NAME AND DESCRIPTION		POSITION	SYMBOL		
CP/EX	VCR.7	Compression/expansion select. 1 = compress (record) 0 = expand (playback)					
CXS1	VCR.6	Compression/expansion bit rate select 1; see Table 2.					
CPD1	VCR.5	Compression/Expansion power-down 1. 0 = Compression/expansion enabled 1 = Compression/expansion disabled					
CXRST	VCR.4	Compression/expansion algorithm reset. 0 = normal operation 1 = reset algorithm to initial coefficients					
CXLB	VCR.3	Compression/expansion interface loopback. 0 = normal operation 1 = bypass selected channel					
U/A	VCR.2	PCM input/output data format. 0 = A-Law 1 = μ -Law					
CXS2	VCR.1	Compression/Expansion bit rate select 2; see Table 2.					
CXS3	VCR.0	Compression/Expansion bit rate select 3.					

COMPRESSION/EXPANSION BIT RATE SELECT Table 2

ALGORITHM SELECTED	CXS1	CXS2	CXS3
64Kbps to/from 32Kbps	0	0	0
64Kbps to/from 24Kbps	1	1	0
64Kbps to/from 16Kbps	0	1	0
Reserved for future operation	1	0	0
64Kbps to/from 16Kbps ¹	0	0	1
64Kbps to/from 12Kbps ¹	1	1	1
64Kbps to/from 8Kbps ¹	0	1	1
64Kbps to/from 64Kbps (PCM Bypass mode)	1	0	1

NOTE:

- These reduced bandwidth modes use an internal low-pass filter at 1.7 KHz to permit a lower bit rate. The normal bandwidth otherwise is 300 Hz to 3.4 KHz due to the filters typically present in the codec/filter device used with the DS2130.

TONE CONTROL REGISTER

The Tone Control register provides access to the tone generator and controls power-down and reset functions.

The tone generator is controlled by bits TS0-3, which cause either transmission of a DTMF digit or one of three possible single-tone sine waves. The DTMF digits that can be transmitted are 0-9, # and *. The single tones available are 350, 620 and 1004 Hz, any of which can be used as beeps for user prompting. Tone generation lasts for as long as the particular state is programmed; all tone generation ceases when TS0-3 equal 1111 (the power-up state). When writing a new value for TS0-3 (including the 1111 state), the TRST bit must be simultaneously set to a 1; otherwise, the old value of TS0-3 will continue to be used. It is recommended

that DTMF digits be sustained for at least 50 mS for proper network recognition.

The CPD2 bit is used in conjunction with CPD1 (in the VCR) to enable a power-down mode in which power consumption is reduced to a minimum. CPD1 and CPD2 must both equal a 1 to enter this mode. The PCMOUT output is three-stated when CPD2 = 1.

Testing of the DTMF generation and detection circuitry can be accomplished by setting TLB to a 1. In this mode, transmit DTMF tones are internally looped back to the DTMF receiver for test purposes (the DT0-3 pins can be monitored for proper operation). Also in this mode, input PCM data is looped back to the appropriate time slot on PCMOUT. This permits isolation and testing of the external codec/filter used with the DS2130.

TONE CONTROL REGISTER Figure 5

(MSB)				(LSB)			
TS3	TS2	CPD2	TRST	TLB	TS1	TS0	-
SYMBOL	POSITION	NAME AND DESCRIPTION					
TS3	TCR.7	Tone selects 0-3. See Table 3 for tone bit mapping.					
TS2	TCR.6	TRST must be written to a 1 when a new tone value is to be written.					
TS1	TCR.2						
TS0	TCR.1						
CPD2	TCR.5	Compression/Expansion power-down 2. 0 = Normal operation 1 = Power-down all DSP operation. CPD1 must equal 1 as well. CPD1=0 while CPD2=1 should not be programmed.					
TRST	TCR.4	Tone generation reload enable for TS0-3. 0 = normal operation/ready for new value 1 = load new tone value					
TLB	TCR.3	Tone generation loopback. 0 = normal operation 1 = loopback tone signals to DTMF receiver					
-	TCR.0	Should always be set to 1.					

TS3-TS0 **TONE GENERATION BIT MAPPING¹** Table 3

TS3-TS0	SIGNAL	LEVEL (dBm0)
0000	DTMF "0"	-3
0001	DTMF "1"	-3
0010	DTMF "2"	-3
0011	DTMF "3"	-3
0100	DTMF "4"	-3
0101	DTMF "5"	-3
0110	DTMF "6"	-3
0111	DTMF "7"	-3
1000	DTMF "8"	-3
1001	DTMF "9"	-3
1010	DTMF "**"	-3
1011	DTMF "#"	-3
1100	1004 Hz	0
1101	350 Hz	-12
1110	620 Hz	-12
1111	Silence	OFF

1. States 0000 through 1011 generate DTMF digit signals; states 1100, 1101 and 1110 generate single frequency tones; state 1111 disables all tone generation (DTMF or single tone).

INPUT TIME SLOT REGISTER Figure 6

(MSB)		(LSB)	
-	-	D5	D0
		D4	
		D3	
		D2	
		D1	
		D0	
SYMBOL	POSITION	NAME AND DESCRIPTION	
-	ITR.7	Reserved; must be zero for proper operation.	
-	ITR.6	Reserved; must be zero for proper operation.	
D5	ITR.5	MSB of input time slot register.	
D4	ITR.4		
D3	ITR.3		
D2	ITR.2		
D1	ITR.1		
D0	ITR.0	LSB of input time slot register.	

OUTPUT TIME SLOT REGISTER Figure 7

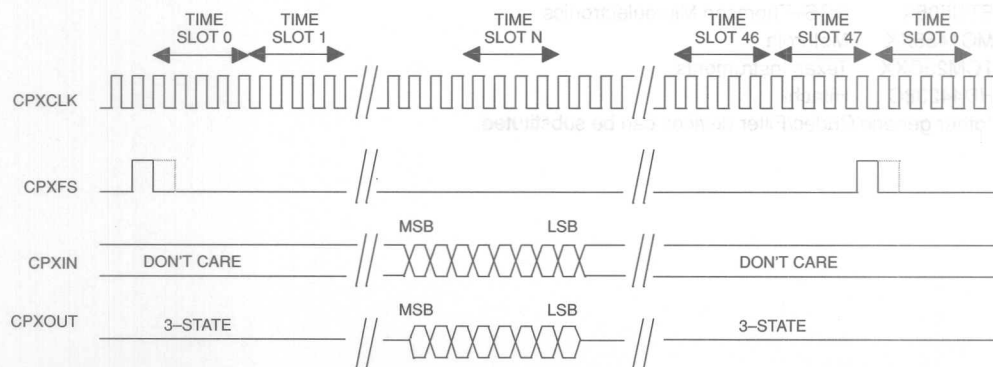
(MSB)				(LSB)			
-	-	D5	D4	D3	D2	D1	D0
SYMBOL	POSITION	NAME AND DESCRIPTION					
-	OTR.7	Reserved; must be zero for proper operation.					
-	OTR.6	Reserved; must be zero for proper operation.					
D5	OTR.5	MSB of output time slot register.					
D4	OTR.4						
D3	OTR.3						
D2	OTR.2						
D1	OTR.1						
D0	OTR.0	LSB of output time slot register.					

TIME SLOT ASSIGNMENT/ORGANIZATION

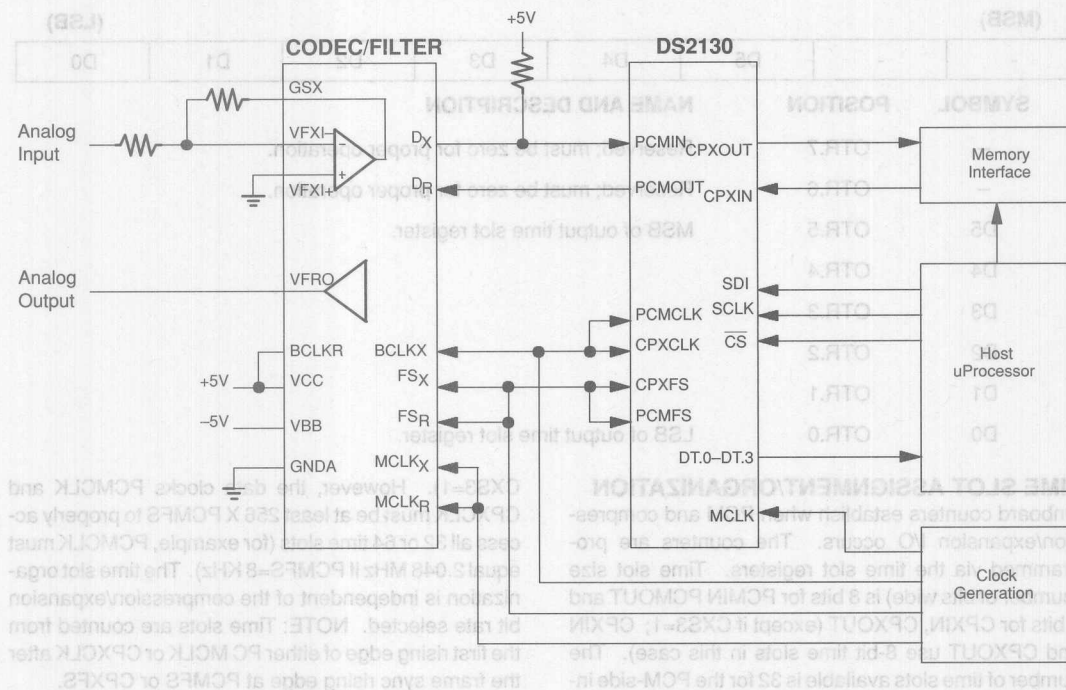
Onboard counters establish when PCM and compression/expansion I/O occurs. The counters are programmed via the time slot registers. Time slot size (number of bits wide) is 8 bits for PCMIN PCMOUT and 4 bits for CPXIN, CPXOUT (except if CXS3=1; CPXIN and CPXOUT use 8-bit time slots in this case). The number of time slots available is 32 for the PCM-side interface and 64 for the CPX-side interface (32 if

CXS3=1). However, the data clocks PCMCLK and CPXCLK must be at least 256 X PCMFS to properly access all 32 or 64 time slots (for example, PCMCLK must equal 2.048 MHz if PCMFS=8 KHz). The time slot organization is independent of the compression/expansion bit rate selected. NOTE: Time slots are counted from the first rising edge of either PC MCLK or CPXCLK after the frame sync rising edge at PCMFS or CPXFS.

DS2130 CPX-SIDE INTERFACE Figure 8



DS2130 CONNECTION TO CODEC/FILTER Figure 9

**NOTE:**

Suggested Codec/Filters

TP305X	National Semiconductor
ETC505X	SGS-Thomson Microelectronics
MC1455XX	Motorola
TCM29CXX	Texas Instruments
HD44238C	Hitachi

*other generic Codec/Filter devices can be substituted.

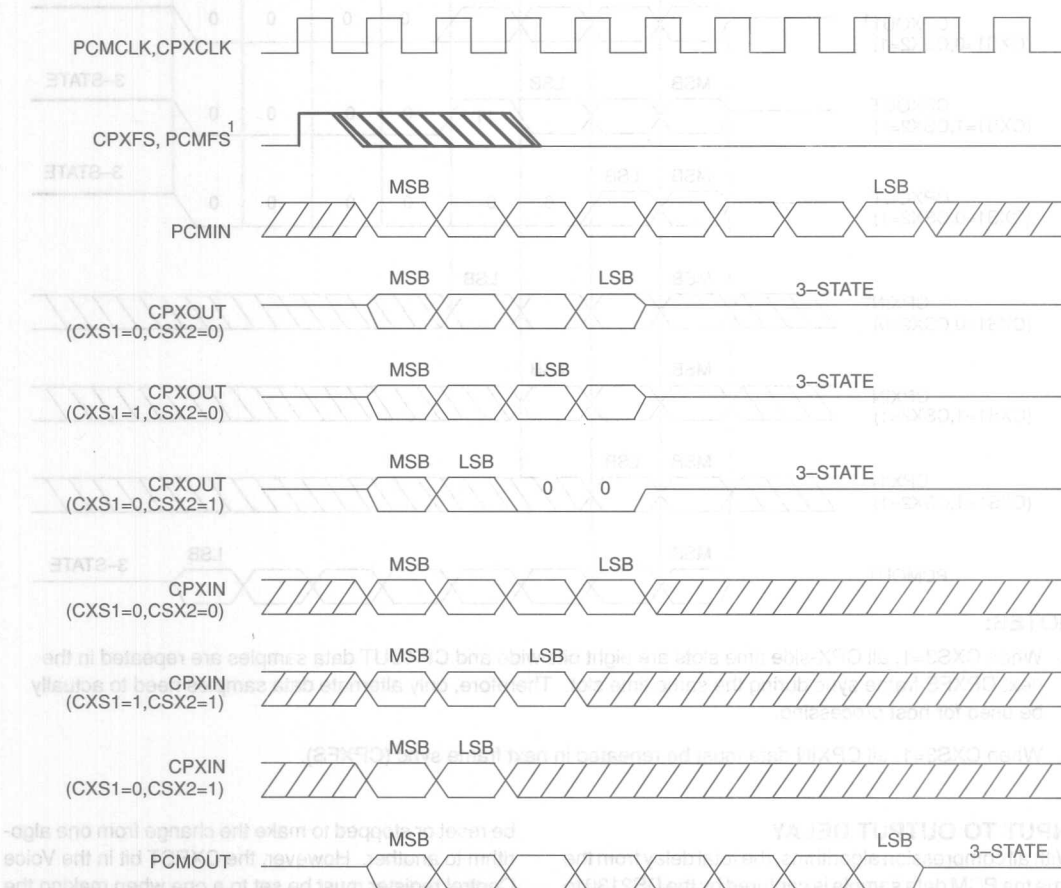
PCM AND CPX INPUT/OUTPUT

The organization of the CPX-side input and output time slots on the DS2130 depends upon the state of bit CXS3 in the VCR. When CXS3=0, all time slots for CPXOUT and CPXIN are four bits wide; when CXS3=1, all time slots are eight bits wide. Also, when CXS3=1, all CPXOUT data is repeated in the next CPXFS sample; therefore, only one out of every two CPXOUT samples

needs to be actually used. However, CPXIN data must be repeated twice when CXS3=1.

PCM-side time slots are always eight bits wide, regardless of CXS3. Figure 10 demonstrates how the DS2130 handles the I/O when CXS3=0; Figure 11 likewise shows the I/O when CXS3=1. It is assumed in both figures that the input and output time slots for both channels are set to zero.

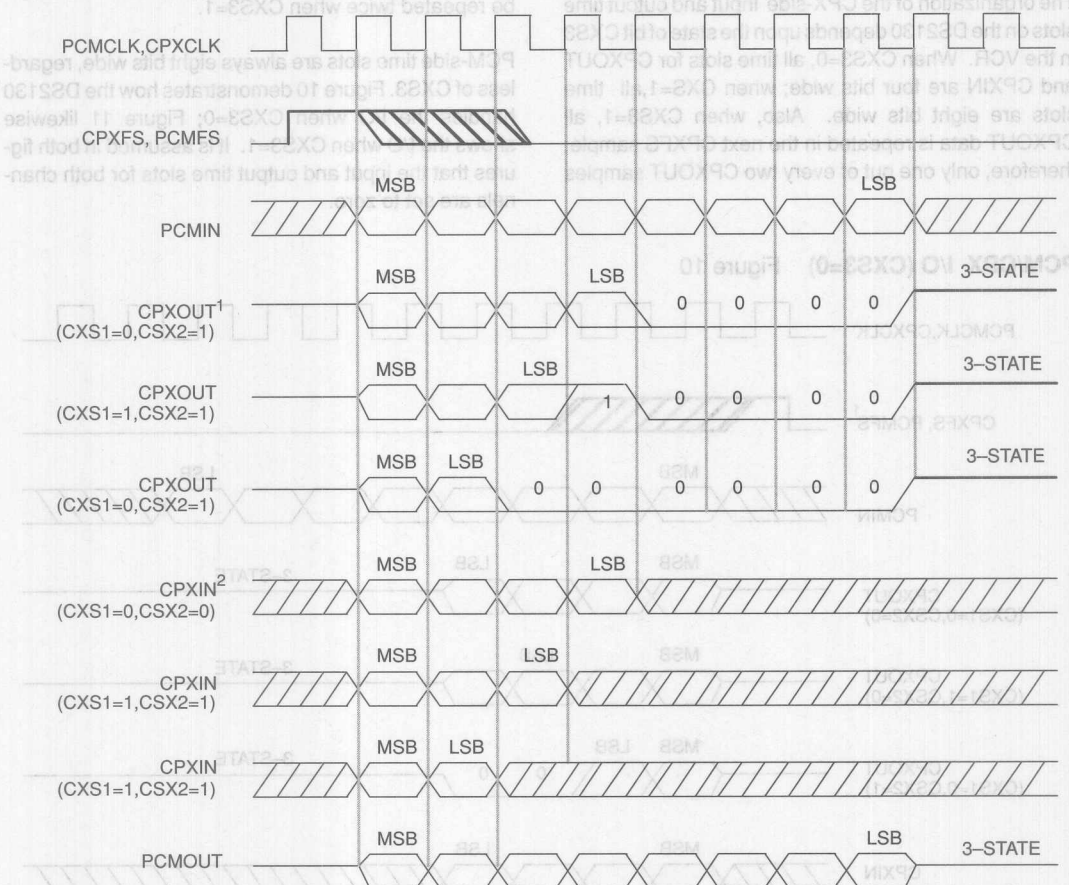
PCM/CPX I/O (CXS3=0) Figure 10



NOTE:

1. The CPXFS and PCMFS frame sync pulses must be at least 1 CPXCLK or PCMCLK high.

PCM/CPX I/O (CXS3=1) Figure 11

**NOTES:**

1. When CXS3=1, all CPX-side time slots are eight bits wide and CPXOUT data samples are repeated in the next CPXFS frame sync during the same time slot. Therefore, only alternate data samples need to actually be used for host processing.
2. When CXS3=1, all CPXIN data must be repeated in next frame sync (CPXFS).

INPUT TO OUTPUT DELAY

With all compression algorithms, the total delay from the time the PCM data sample is captured by the DS2130 to the time it is output is always less than 375 μ s. The exact delay is determined by the input and output time slots selected for each channel.

ON-THE-FLY ALGORITHM SELECTION

The user can switch between the three available algorithms on-the-fly. That is, the DS2130 does not need to

be reset or stopped to make the change from one algorithm to another. However, the CXRST bit in the Voice Control register must be set to a one when making the algorithm change. The DS2130 reads the Control register before it starts to process each PCM or CPX sample. If the user wishes to switch algorithms, then the Voice Control register must be updated via the serial port before the first input sample to be processed with the new algorithm arrives at either PCMIN or CPXIN. PCM and ADPCM outputs will tristate during register updates.

SPECIAL CLOCK REQUIREMENTS

The minimum number of clock transitions at CPXCLK and PCMCLK is nine per every CPXFS and PCMFSP period (one for clocking the frame sync pulse and eight for the PCM or CPX data bits). When using this minimum number, please note that all nine clocks must occur within 1/3 of the total PCMFSP/CPXFS period. For example, if CPXFS=8 KHz, then nine CPXCLK clocks must be received within 41.7 μ s after the rising edge of CPXFS. The CPXCLK pin can remain idle until the next CPXFS rising edge.

When the DS2130 is placed in the power-down mode (CPD1=CPD2=1), the serial port must be subsequently clocked at less than 39 KHz (at SCLK) to write new data. Once the power-down mode is exited, the serial port can be operated at full speed again.

DTMF/ENERGY DETECTION

The DS2130 provides continuous detection of DTMF signals as well as monitoring of signal levels received at PCMIN. The only exception is when CPD1 and CPD2 are both set to one, which disables all DSP activity. The detect outputs, DT0-DT3 as shown in Table 5, indicate when DTMF digits have been detected and when certain energy thresholds have been exceeded. DTMF digits always take precedence over energy monitoring.

For example, if a voice signal is present, only the states 1100 through 1111 are possible since DTMF signals are not present. When a DTMF digit is detected, the code for that digit will appear at DT0-DT3 for the duration of the signal. When the digit is no longer present, DT0-DT3 will return to one of the four possible energy detect states (1100 - 1111). It is recommended that these outputs be scanned at a rate no slower than 30 mS to avoid missing a digit since a DTMF burst may be as short as 50 ms. If the digit is generated only by a keypad depression, then a slower sample rate can be used.

As shown in Figure 1, the energy detector monitors the output of the DTMF low-band filter, which is a low-pass filter with a breakpoint at 1 KHz. The fundamental power spectrum of speech is typically in the range of 500 - 1000 Hz so that the energy detector can be used as an indication of voice level strength. This information can be used to determine if the gain in the analog front-end needs to be increased or when to stop recording. The energy detector integrates the signal over a 10 mS period.

As shown in Figure 9, a Data Valid signal for interrupting a processor can be created by simply ANDing the DT2 and DT3 outputs together. The output of the AND gate will go low whenever a DTMF digit is detected.

DETECT OUTPUT CODING¹ Table 4

DT3-DT0	DESCRIPTION
0000	DTMF digit "0" detected.
0001	DTMF digit "1" detected.
0010	DTMF digit "2" detected.
0011	DTMF digit "3" detected.
0100	DTMF digit "4" detected.
0101	DTMF digit "5" detected.
0110	DTMF digit "6" detected.
0111	DTMF digit "7" detected.
1000	DTMF digit "8" detected.
1001	DTMF digit "9" detected.
1010	DTMF digit "*" detected.
1011	DTMF digit "#" detected.
1100	Vin > -15 dBm0
1101	-15 > Vin > -25 dBm0
1110	-25 > Vin > -40 dBm0
1111	-40 > Vin

1. Zero dBm0 is defined as the PCM signal level, which is 3 dB below the maximum PCM level.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

-1.0V to +7.0V

0°C to 70°C

-55°C to +125°C

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{CC}	4.5		5.5	V	

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		20		mA	1,2
Power-Down Current	I_{DDPD}		1		mA	1,2,3
Input Leakage	I_{ILK}	-1.0		+1.0	μA	
Output Leakage	I_{OLK}	-1.0		+1.0	μA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. PCMCLK = CPXCLK = 2.048 MHz; MCLK = 12 MHz.
2. Outputs open; inputs swinging full supply levels.
3. Control register bits CPD1 = CPD2 = 1.
4. PCMOUT and CPXOUT are tri-stated.

DTMF RECEIVER CHARACTERISTICS (0°C to 70°C; $V_{CC} = +5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Valid Detect Amplitude Range		-40		0	dBm0	1,2
Frequency Deviation Accept		± 1.5			%	3
Frequency Deviation Reject		± 3.5			%	3
Minimum Twist Accept Range		-10		+10	dB	4
Talk Off (Mitel Test Tape #CM7291)			5		Hits	5
Noise Tolerance (Mitel Test Tape #CM7291)			-12		dB	6

NOTES:

1. All DTMF receiver tests performed using test circuit shown in Figure 12.
2. Individual tone level of the DTMF pair.
3. Percent of nominal frequency for the individual tone.
4. Twist = 20 LOG (Hi tone/Lo tone).
5. Talk Off is a measure of the speech immunity of a DTMF receiver; the lower the number of hits, the better the immunity.
6. Three KHz bandlimited white noise, referenced to lowest amplitude tone in the DTMF pair.

DTMF RECEIVER TIMING(0°C to 70°C; $V_{CC} = +5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Tone Duration Accept	t_{TAC}	40			ms	1
Tone Duration Reject	t_{TRJ}			20	ms	
Interdigit Pause Accept	t_{PAC}	40			ms	
Interdigit Pause Reject	t_{PRJ}			20	ms	
Detect Delay (DT0-3)	t_{DTD}	25		45	ms	

NOTE:

1. See Figure 13 for DTMF receiver timing diagrams.

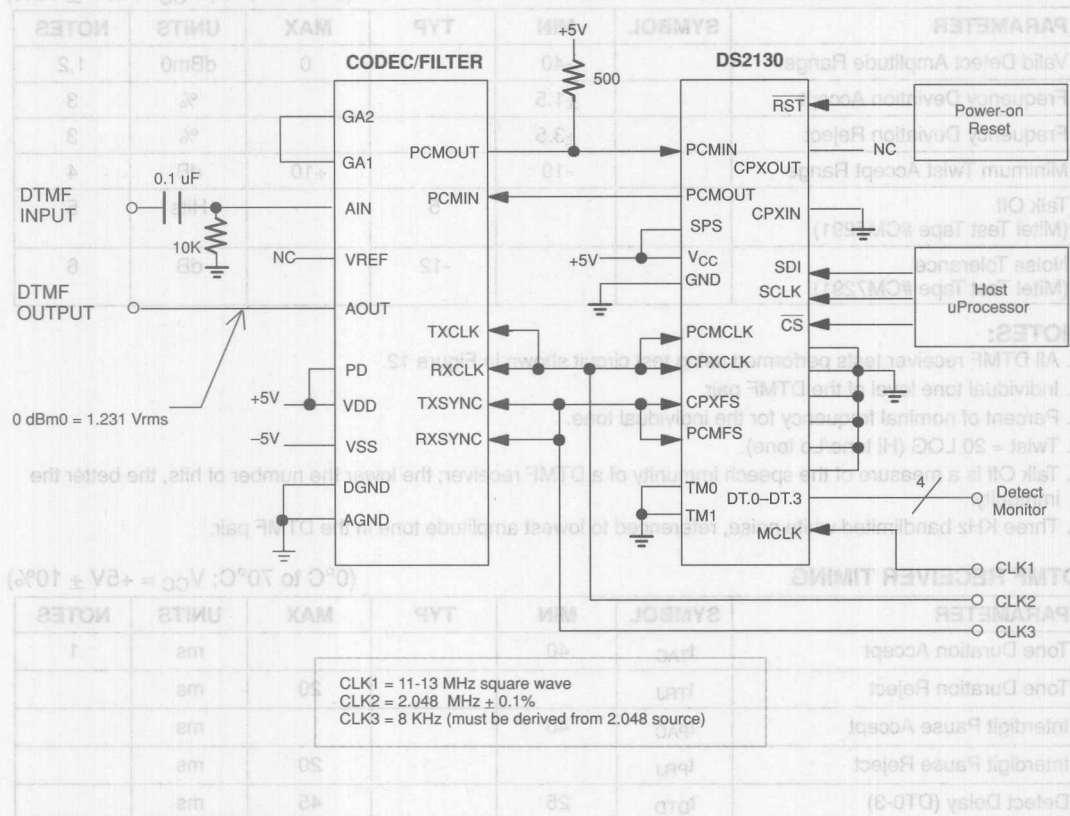
DTMF/TONE GENERATOR CHARACTERISTICS(0°C to 70°C; $V_{CC} = +5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DTMF Frequency Deviation (each tone of the pair)				± 1.0	%	1, 2
DTMF High Tone Level			-6.0		dBm0	
DTMF Low Tone Level			-6.0		dBm0	
Output Twist (DTMF only)			0.0		dB	
1004 Hz Tone Level			0.0		dBm0	
620, 350 Hz Tone Level			-12.0		dBm0	
Output Distortion (single tone)				-25	dB	3

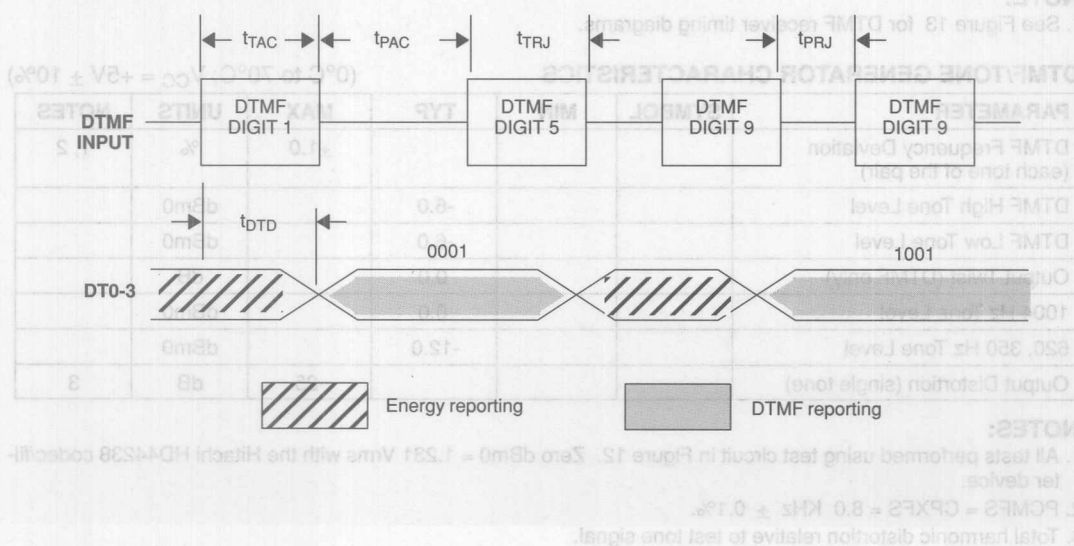
NOTES:

1. All tests performed using test circuit in Figure 12. Zero dBm0 = 1.231 Vrms with the Hitachi HD44238 codec/filter device.
2. PCMFS = CPXFS = 8.0 KHz \pm 0.1%.
3. Total harmonic distortion relative to test tone signal.

DTMF RECEIVER/GENERATOR TEST CIRCUIT Figure 12



DTMF RECEIVER TIMING Figure 13



PCM INTERFACE**AC ELECTRICAL CHARACTERISTICS**(0°C to 70°C; $V_{CC}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PCMCLK, CPXCLK Clock Period	t_p	244		5208	ns	1
PCMCLK, CPXCLK Pulse Width High	t_{WH}	100			ns	
PCMCLK, CPXCLK Rise, Fall Times	t_R t_F	10	20		ns	
Hold Time from PCMCLK, CPXCLK to PCMFS, CPXFS	t_{HOLD}	0			ns	2
Setup Time from PCMFS, CPXFS high to PCMCLK, CPXCLK low	t_{SF}	50			ns	2
Hold Time from PCMCLK, CPXCLK Low to PCMFS, CPXFS Low	t_{HF}	100			ns	2
Setup Time for PCMIN, CPXIN to PCMCLK, CPXCLK Low	t_{SD}	50			ns	2
Hold Time for PCMIN, CPXIN to PCMCLK, CPXCLK Low	t_{HD}	50			ns	2
Delay Time from PCMCLK, CPXCLK to Valid PCMOUT, CPXOUT	t_{DO}	10		150	ns	3
Delay Time from PCMCLK, CPXCLK to PCMOUT, CPXOUT 3-stated	t_{DZ}	20		150	ns	2,3,4

NOTES:

1. At least nine CPXCLK(or PCMCLK) clocks must be received within 1/3 of the CPXFS (or PCMFS) period.
2. Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10 ns maximum rise and fall times.
3. Load = 150 pF + 2 LSTTL loads.
4. For LSB of PCM or CPX word.

MASTER CLOCK/RESET
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	MAX	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	95	t _{PM}	75		95	ns	1
MCLK Duty Cycle (t _{WMH} / t _{WML} + t _{WMH})	55		45		55	%	
MCLK Rise/Fall Times	10	t _{RM} t _{FM}	10		10	ns	
RST Pulse Width		t _{RST}	1	0		ms	

NOTE:

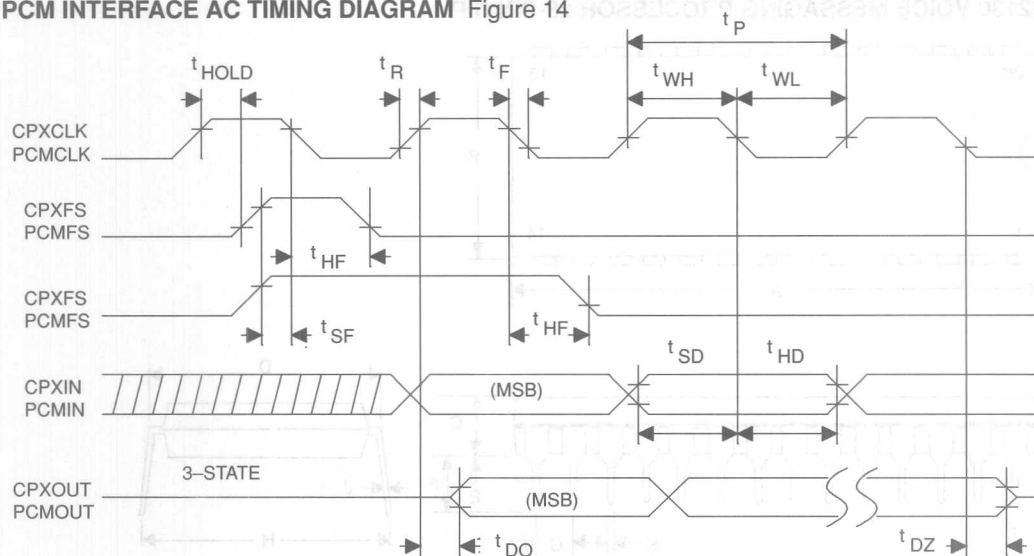
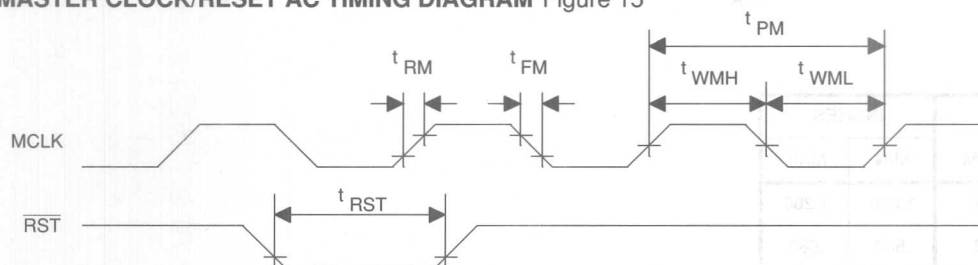
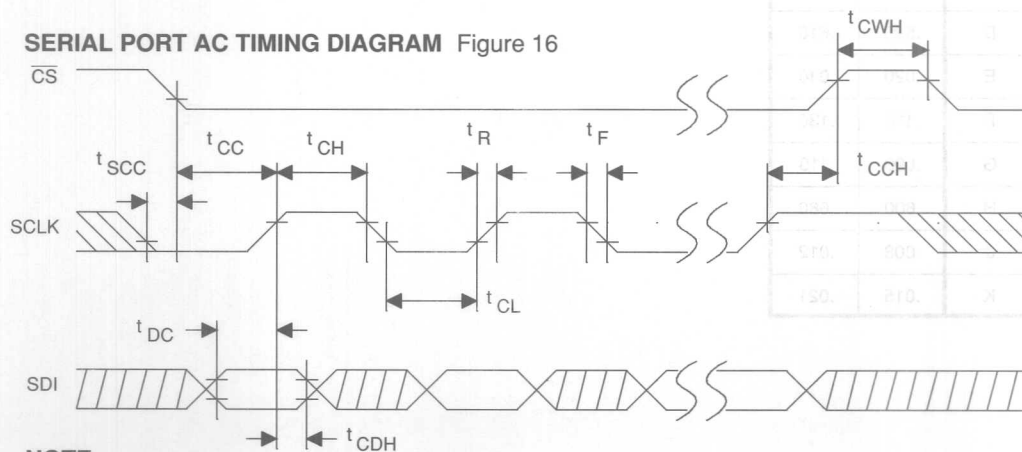
1. MCLK = 10.5 to 12.5 MHz typically.

SERIAL PORT
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t _{DC}	55			ns	1
SCLK to SDI Hold	t _{CDH}	55			ns	1
SCLK Low Time	t _{CL}	250			ns	1
SCLK High Time	t _{CH}	250			ns	1
SCLK Rise and Fall Time	t _R , t _F			100	ns	1
CS to SCLK Setup	t _{CC}	50			ns	1
SCLK to $\overline{\text{CS}}$ Hold	t _{CCH}	250			ns	1
CS Inactive Time	t _{CWH}	250			ns	1
SCLK Setup to $\overline{\text{CS}}$ Falling	t _{SCC}	50			ns	1

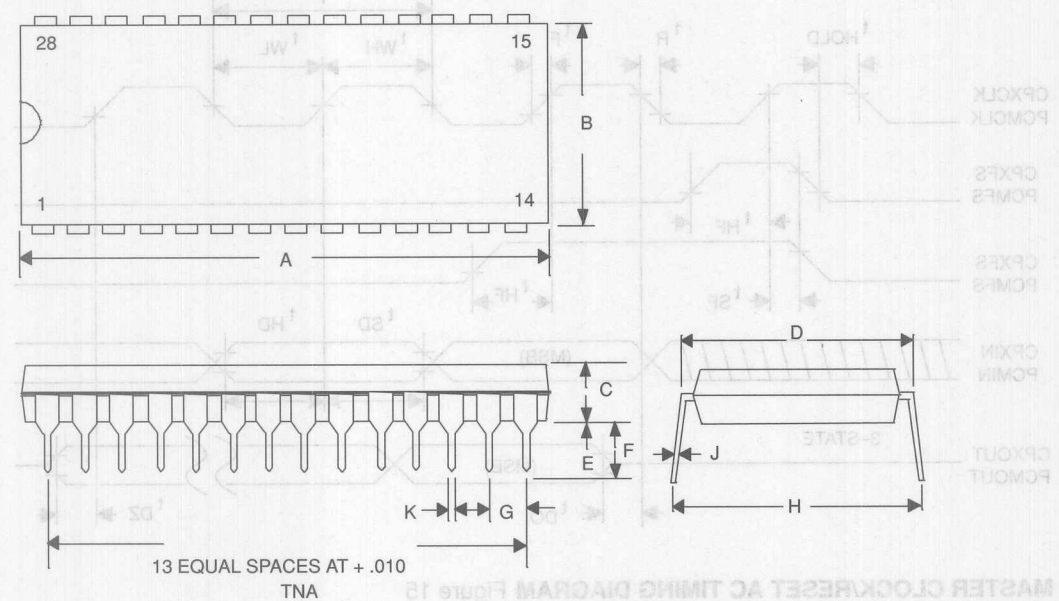
NOTE:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.

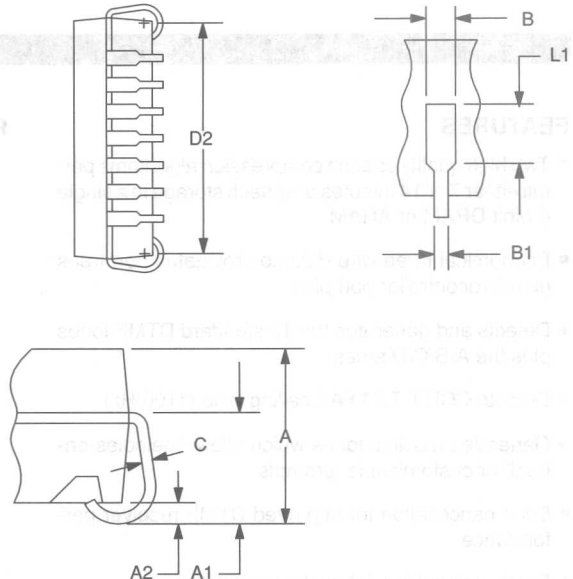
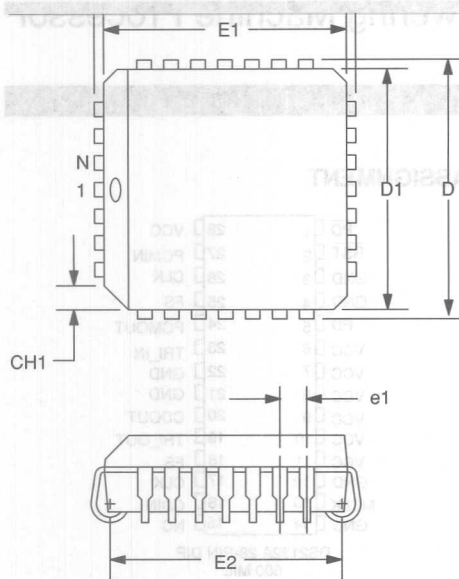
PCM INTERFACE AC TIMING DIAGRAM Figure 14**MASTER CLOCK/RESET AC TIMING DIAGRAM** Figure 15**SERIAL PORT AC TIMING DIAGRAM** Figure 16

NOTE:
SCLK may be either high or low when \overline{CS} is taken low.

DS2130 VOICE MESSAGE PROCESSOR 28-PIN DIP



DIM	INCHES	
	MIN	MAX
A	1.240	1.280
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021



DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	—
N	28	—
e1	0.050 BSC	
CH1	0.042	0.048

DESCRIPTION

The DS2130A Digital Answer Machine Processor is a 2.5Kbit signal processor (LSI) optimized for the compact, low-power, 100-pin quad package. It is designed to interface with the DS2130A compact disc recorder and the DS2130A compact disc player. The DS2130A compact disc recorder and the DS2130A compact disc player are designed to interface with the DS2130A compact disc recorder and the DS2130A compact disc player. The DS2130A compact disc recorder and the DS2130A compact disc player are designed to interface with the DS2130A compact disc recorder and the DS2130A compact disc player.

The DS2130A is ideal for embedded applications such as digital answering machines, voice mail, voice announcements, and other devices that need to maximize space and power efficiency. A single

DALLAS

SEMICONDUCTOR

DS2132A/Q

Digital Answering Machine Processor

FEATURES

- Two high quality speech compression algorithms permit either 7 or 14 minutes of speech storage in a single 4 Mbit DRAM or ARAM
- Economical three-wire data/control/status port frees up microcontroller port pins
- Detects and generates the 12 standard DTMF tones plus the A/B/C/D tones
- Detects CCITT T.30 FAX calling tone (1100 Hz)
- Generates musical tones which allow "melodies-on-hold" or customizable prompts
- Echo cancellation for improved DTMF receiver performance
- Precise signal level detection capability
- Record/Playback gain control
- 28-pin DIP or PLCC (DS2132AQ) packages

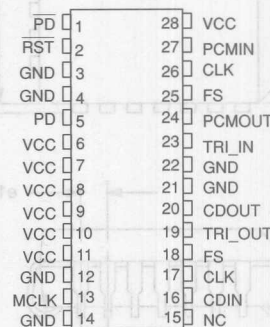
There is a series of Application Notes that accompany this data sheet.

DESCRIPTION

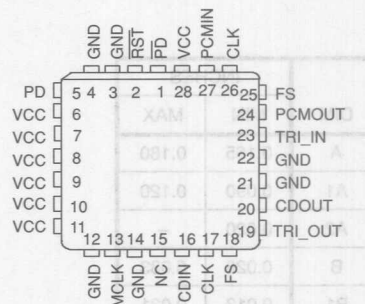
The DS2132A Digital Answering Machine Processor is a Digital Signal Processor (DSP) optimized for the compression/expansion of PCM coded voice to/from an extremely low bit rate. The DS2132A contains two advanced speech compression algorithms that offer outstanding fidelity. The Standard Record/Playback algorithm compresses speech to 9.8Kbps and the Extended Record/Playback algorithm compresses speech to 4.9Kbps.

The DS2132A is ideal for embedded applications such as digital answering machines, voice mail, voice annunciators, and any other device that needs to maximize speech storage in a limited memory space. A simple

PIN ASSIGNMENT



DS2132A 28-PIN DIP
600 MIL



DS2132AQ 28-PIN
PLCC

three wire interface to the embedded microcontroller frees up valuable controller port pins for other uses and simplifies the software needed to transfer speech data, issue commands, and receive DTMF/energy level/status information. The DS2132A detects and generates all 16 DTMF tones and can also generate a wide variety of call progress tones. In addition, the DS2132A provides CCITT Rec. T.30 FAX calling tone detection which enables the answering machine to determine if the incoming call is a voice or FAX transmission. The energy level detector allows the microcontroller to perform call progress detection and automatic gain control functions.

PIN DESCRIPTION Table 1

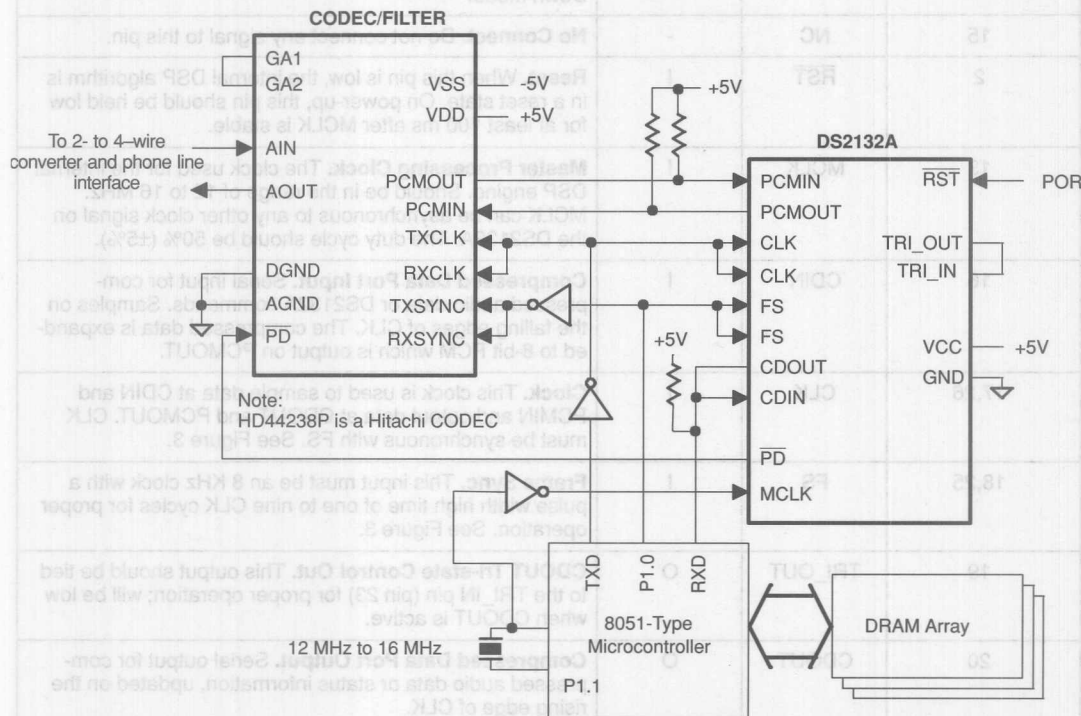
PIN	SYMBOL	TYPE	DESCRIPTION
3,4,12,14,21,22	GND	-	Ground. Tie to system ground.
6,7,8,9,10,11,28	VCC	-	Positive Supply. Tie to system +5 volt supply.
1	PD	O	Power-Down Active Low. Will toggle low during Power-Down mode.
5	PD	O	Power-Down Active High. Will toggle high during Power-Down mode.
15	NC	-	No Connect. Do not connect any signal to this pin.
2	RST	I	Reset. When this pin is low, the internal DSP algorithm is in a reset state. On power-up, this pin should be held low for at least 100 ms after MCLK is stable.
13	MCLK	I	Master Processing Clock. The clock used for the internal DSP engine. Should be in the range of 12 to 16 MHz. MCLK can be asynchronous to any other clock signal on the DS2132A. The duty cycle should be 50% ($\pm 5\%$).
16	CDIN	I	Compressed Data Port Input. Serial input for compressed audio data or DS2132A commands. Samples on the falling edges of CLK. The compressed data is expanded to 8-bit PCM which is output on PCMOUT.
17,26	CLK	I	Clock. This clock is used to sample data at CDIN and PCMIN and output data at CDOOUT and PCMOUT. CLK must be synchronous with FS. See Figure 3.
18,25	FS	I	Frame Sync. This input must be an 8 KHz clock with a pulse width high time of one to nine CLK cycles for proper operation. See Figure 3.
19	TRI_OUT	O	CDOOUT Tri-state Control Out. This output should be tied to the TRI_IN pin (pin 23) for proper operation; will be low when CDOOUT is active.
20	CDOOUT	O	Compressed Data Port Output. Serial output for compressed audio data or status information, updated on the rising edge of CLK.
23	TRI_IN	I	CDOOUT Tri-state Control In. This input should be tied to the TRI_OUT pin (pin 19) for proper operation. If this pin is forced high, CDOOUT will not go active.
24	PCMOUT	O	PCM Port Output. Output for expanded data which is in the standard 8-bit μ -law format. Data is updated on the rising edges of CLK.
27	PCMIN	I	PCM Port Input. Input for the 8-bit serial μ -law PCM data which would normally be supplied by a codec/filter device. Data is sampled on the falling edges of CLK.

FUNCTIONAL DESCRIPTION

A typical digital answering machine using the DS2132A is shown in Figure 1. The system consists of a standard telephone CODEC (Coder-DECoder) device, the DS2132A, a microcontroller, and a bank of DRAM. The implementation shown is with a Hitachi CODEC and a 8051-type microcontroller but a wide variety of

CODECs and microcontrollers can be used with the DS2132A. It is only important that the CODEC have serial digital I/O and have μ -law ("Mu" law) companding. Table 2 lists some CODECs that will work with the DS2132A. There is a separate Application Note that explains how to connect these CODECs to the DS2132A.

TYPICAL DIGITAL ANSWERING SYSTEM Figure 1



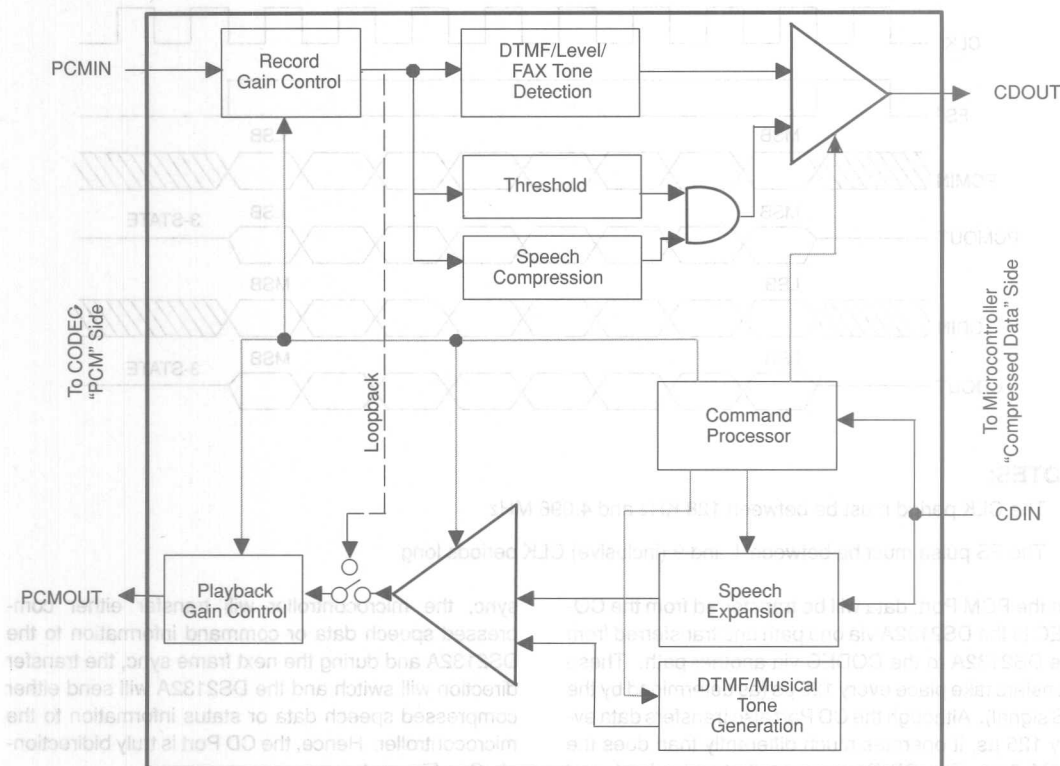
RECOMMENDED DS2132A CODECS Table 2

VENDOR	MODEL(S)
Texas Instruments	TCM29CXX
National Semiconductor	TP3054X
Motorola	MC1455XX
SGS-Thomson	ETC505X
Hitachi	HD44238C

As shown in Figure 1, the microcontroller creates the clock (CLK) and frame sync (FS) that is sent to both the CODEC and the DS2132A. In this manner, the

DS2132A shares the signals necessary to drive the CODEC. To "record" an audio signal, the following occurs. The analog signal applied at the AIN pin of the CODEC is converted to eight bit values and output at PCMOUT every 125 μ s. The DS2132A takes these eight bit samples in at the PCMIN pin and effectively compresses them to either 9.8Kbps or 4.9Kbps. See Figure 2. The compressed data is then passed to the microcontroller via the CDOUT pin (CD stands for Compressed Data). The microcontroller then stores the compressed speech in the DRAM array. The inverse of this process is required to "playback" the message at the AOUT pin of the CODEC.

DS2132A BLOCK DIAGRAM Figure 2

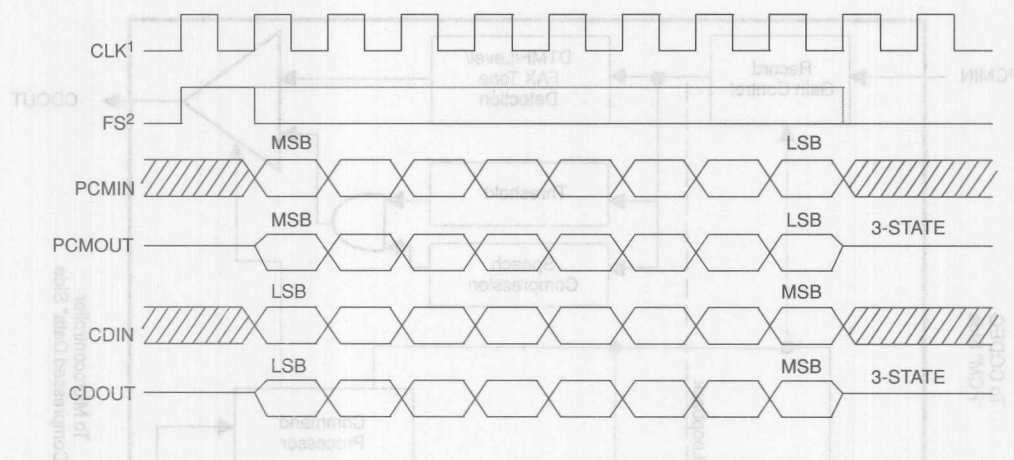


OPERATION OF THE CD AND PCM PORTS

As mentioned earlier, the DS2132A essentially contains two separate serial ports, one for the DS2132A to microcontroller interface (the CD Port) and one for the CODEC to DS2132A interface (the PCM Port). The Compressed Data (CD) Port is used to send compressed speech information from the DS2132A to the microcontroller and vice versa. The CD Port is also used to monitor the current status of the DS2132A and it is used to issue instructions to the DS2132A. The CD Port consists of the CDIN, CDOUT, CLK, and FS pins (the CLK

and FS pins are shared with the CODEC). The PCM Port is used to transfer uncompressed speech data between the DS2132A and the CODEC. It consists of the PCMIN, PCMOUT, CLK, and FS pins. Figure 3 details the DS2132A CD and PCM port signals. All communication begins with the frame sync (FS) signal. It indicates to the DS2132A and the CODEC that a byte of information will follow. Note that the PCM Port operates on a MSB first basis and the CD Port operates on a LSB first basis.

CD AND PCM PORT I/O DIAGRAM Figure 3

**NOTES:**

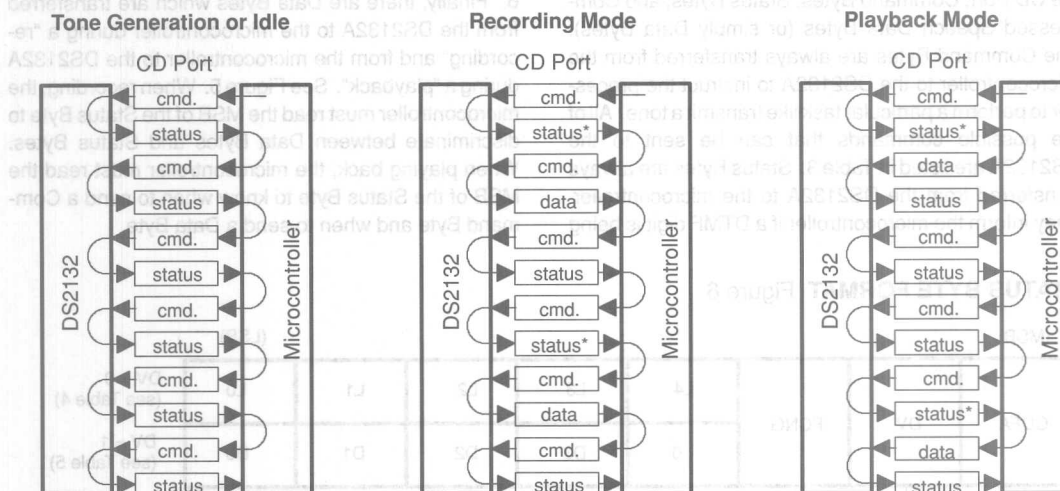
1. The CLK period must be between 128 KHz and 4.096 MHz
2. The FS pulse must be between 1 and 9 (inclusive) CLK periods long

On the PCM Port, data will be transferred from the CODEC to the DS2132A via one path and transferred from the DS2132A to the CODEC via another path. These transfers take place every 125 μ s (as determined by the FS signal). Although the CD Port also transfers data every 125 μ s, it operates much differently than does the PCM Port. The CD Port constantly toggles back and forth in its data transfer direction. During one frame

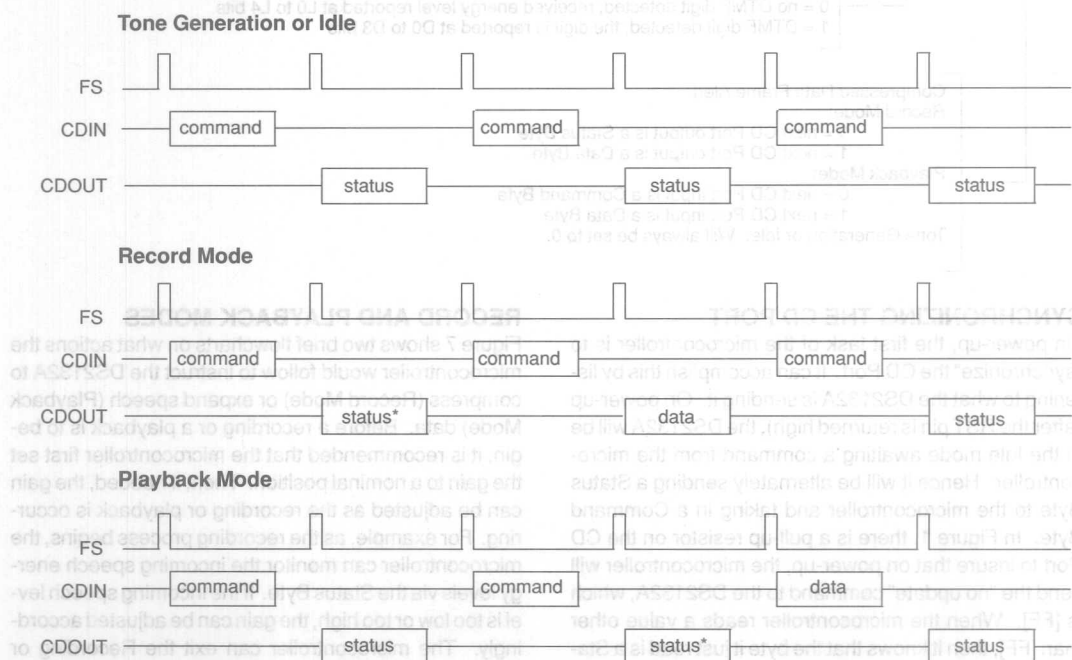
sync, the microcontroller will transfer either compressed speech data or command information to the DS2132A and during the next frame sync, the transfer direction will switch and the DS2132A will send either compressed speech data or status information to the microcontroller. Hence, the CD Port is truly bidirectional. See Figure 4.

As mentioned earlier, the DS2132A essentially contains two separate serial ports, one for the DS2132A to microcontroller interface (the CD Port) and one for the CODEC to DS2132A interface (the PCM Port). The Compressed Data (CD) Port is used to send compressed speech information from the DS2132A to the microcontroller and vice versa. The CD Port is also used to monitor the current status of the DS2132A and it is used to issue instructions to the DS2132A. The CD Port consists of the CDIN, CDOUT, CLK, and FS pins (the CLK

FS pin is shared with the CODEC). The PCM Port is used to transfer uncompressed speech data between the DS2132A and the CODEC. It consists of the PCMIN, PCMOUT, CLK, and FS pins. All communication between the DS2132A and the CODEC takes place every 125 μ s (as determined by the FS signal). It indicates that the PCM Port operates on a byte basis and the CD Port operates on a byte basis.

CD PORT FLOW STRUCTURE Figure 4

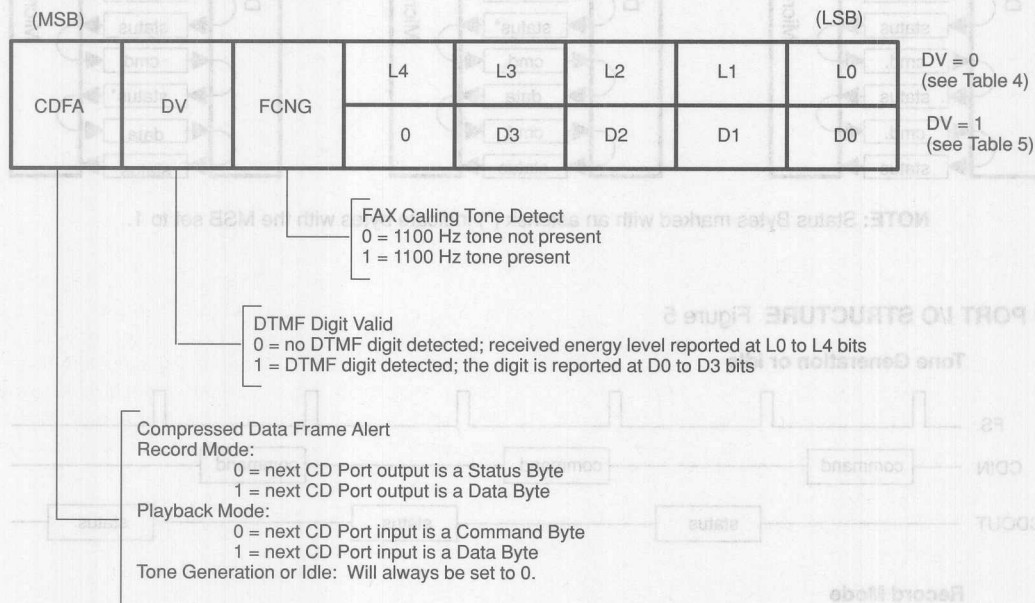
NOTE: Status Bytes marked with an asterisk (*) indicate bytes with the MSB set to 1.

CD PORT I/O STRUCTURE Figure 5

There are three types of bytes that can be transferred on the CD Port; Command Bytes, Status Bytes, and Compressed Speech Data Bytes (or simply Data Bytes). The Command Bytes are always transferred from the microcontroller to the DS2132A to instruct the processor to perform a particular task like transmit a tone. All of the possible commands that can be sent to the DS2132A are listed in Table 3. Status Bytes are always transferred from the DS2132A to the microcontroller. They inform the microcontroller if a DTMF digit is being

received, or what the current energy level is. See Figure 6. Finally, there are Data Bytes which are transferred from the DS2132A to the microcontroller during a "recording" and from the microcontroller to the DS2132A during a "playback". See Figure 5. When recording, the microcontroller must read the MSB of the Status Byte to discriminate between Data Bytes and Status Bytes. When playing back, the microcontroller must read the MSB of the Status Byte to know when to send a Command Byte and when to send a Data Byte.

STATUS BYTE FORMAT Figure 6



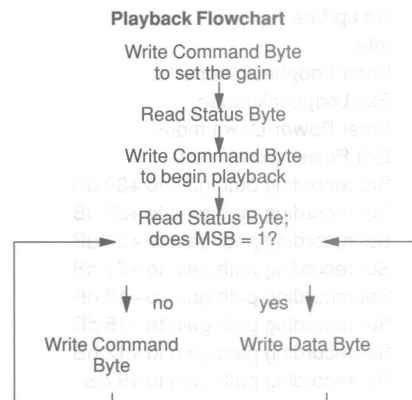
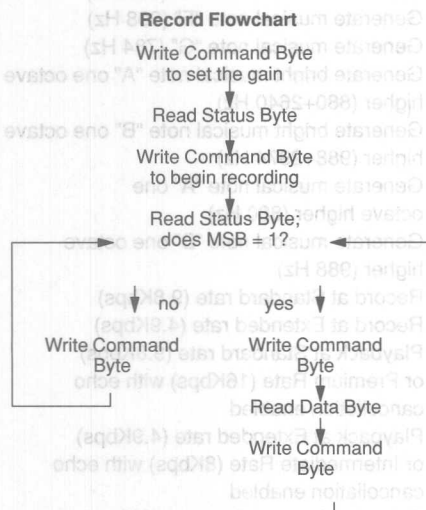
SYNCHRONIZING THE CD PORT

On power-up, the first task of the microcontroller is to "synchronize" the CD Port. It can accomplish this by listening to what the DS2132A is sending it. On power-up (after the $\overline{\text{RST}}$ pin is returned high), the DS2132A will be in the Idle mode awaiting a command from the microcontroller. Hence it will be alternately sending a Status Byte to the microcontroller and taking in a Command Byte. In Figure 1, there is a pull-up resistor on the CD Port to insure that on power-up, the microcontroller will send the "no update" command to the DS2132A, which is [FF]. When the microcontroller reads a value other than [FF], then it knows that the byte it just read is a Status Byte and hence it will then know that the next byte will be a Command Byte and it will be synchronized.

RECORD AND PLAYBACK MODES

Figure 7 shows two brief flowcharts on what actions the microcontroller would follow to instruct the DS2132A to compress (Record Mode) or expand speech (Playback Mode) data. Before a recording or a playback is to begin, it is recommended that the microcontroller first set the gain to a nominal position. Then, if needed, the gain can be adjusted as the recording or playback is occurring. For example, as the recording process begins, the microcontroller can monitor the incoming speech energy levels via the Status Byte. If the incoming speech level is too low or too high, the gain can be adjusted accordingly. The microcontroller can exit the Recording or Playback Modes by sending the Idle command.

RECORD AND PLAYBACK FLOWCHARTS Figure 7



LOOPBACK MODE

The DS2132A contains a Loopback Mode that is useful in debugging the CODEC to DS2132A interface and in adjusting the analog circuits to the proper gain/attenuation levels. In the Loopback Mode, the DS2132A routes the incoming digitized audio signal received at the PCMIN pin, back to the PCMOUT pin after making gain adjustments. See Figure 2. Notice that the route includes the record and playback gain circuits. The Loopback mode can be enabled at any time. When the Loopback is enabled, the generated tones or expanded speech are ignored. See Figure 2. The DS2132A will enter the Loopback mode if a Command Byte of [08] is sent to it by the microcontroller. The Loopback mode will be exited upon receiving the Exit Loopback Mode command.

FAX CALLING TONE DETECT

According to CCITT Recommendation T.30, originating automatic FAX machines should transmit an 1100 Hz tone for 0.5 seconds every 3.5 seconds (on for 0.5's; off for 3.0's). This tone is meant as an indication to the called station that a non-voice instrument is making the call. The Status Byte in the DS2132A reports if a 1100 Hz tone is being received. This detection can be used to determine if a FAX machine has called the answering machine. The answering machine will then know not to record the incoming call and to route the call to a FAX machine.

COMMAND BYTE OPTIONS Table 3

[FF]	No update	[B8]	Generate musical note "E" (659 Hz)
[00]	No update	[B9]	Generate musical note "F" (698 Hz)
[BE]	Idle	[BA]	Generate musical note "G" (784 Hz)
[08]	Enter Loopback mode	[9B]	Generate bright musical note "A" one octave higher (880+2640 Hz)
[09]	Exit Loopback mode	[9C]	Generate bright musical note "B" one octave higher (988+2974 Hz)
[04]	Enter Power-Down mode	[BB]	Generate musical note "A" one octave higher (880 Hz)
[05]	Exit Power-Down mode	[BC]	Generate musical note "B" one octave higher (988 Hz)
[4A]	Set recording path gain to +30 dB	[25]	Record at Standard rate (9.8Kbps)
[49]	Set recording path gain to +27 dB	[27]	Record at Extended rate (4.9Kbps)
[48]	Set recording path gain to +24 dB	[28]	Playback at Standard rate (9.8Kbps) or Premium Rate (16Kbps) with echo cancellation enabled
[47]	Set recording path gain to +21 dB	[2A]	Playback at Extended rate (4.9Kbps) or Intermediate Rate (8Kbps) with echo cancellation enabled
[46]	Set recording path gain to +18 dB	[23]	Record at Intermediate rate (8Kbps)
[45]	Set recording path gain to +15 dB	[21]	Record at Premium rate (16Kbps)
[44]	Set recording path gain to +12 dB	[20]	Playback at Standard rate (9.8 Kbps) or Premium rate [16Kbps] with echo cancellation disabled
[43]	Set recording path gain to +9 dB	[22]	Playback at Extended rate (4.9Kbps) or Intermediate rate (8Kbps) with echo cancellation disabled
[42]	Set recording path gain to +6 dB	[6A]	Set playback path gain to +30 dB
[41]	Set recording path gain to +3 dB	[69]	Set playback path gain to +27 dB
[40]	Set recording path gain to 0 dB	[68]	Set playback path gain to +24 dB
[5F]	Set recording path gain to -3 dB	[67]	Set playback path gain to +21 dB
[5E]	Set recording path gain to -6 dB	[66]	Set playback path gain to +18 dB
[5D]	Set recording path gain to -9 dB	[65]	Set playback path gain to +15 dB
[5C]	Set recording path gain to -12 dB	[64]	Set playback path gain to +12 dB
[5B]	Set recording path gain to -15 dB	[63]	Set playback path gain to +9 dB
[5A]	Set recording path gain to -18 dB	[62]	Set playback path gain to +6 dB
[59]	Set recording path gain to -21 dB	[61]	Set playback path gain to +3 dB
[58]	Set recording path gain to -24 dB	[60]	Set playback path gain to 0 dB
[57]	Set recording path gain to -27 dB	[7F]	Set playback path gain to -3 dB
[56]	Set recording path gain to -30 dB	[7E]	Set playback path gain to -6 dB
[80]	Generate DTMF "0" (941+1336 Hz)	[7D]	Set playback path gain to -9 dB
[81]	Generate DTMF "1" (697+1209 Hz)	[7C]	Set playback path gain to -12 dB
[82]	Generate DTMF "2" (697+1336 Hz)	[7B]	Set playback path gain to -15 dB
[83]	Generate DTMF "3" (697+1477 Hz)	[7A]	Set playback path gain to -18 dB
[84]	Generate DTMF "4" (770+1209 Hz)	[79]	Set playback path gain to -21 dB
[85]	Generate DTMF "5" (770+1336 Hz)	[78]	Set playback path gain to -24 dB
[86]	Generate DTMF "6" (770+1477 Hz)	[77]	Set playback path gain to -27 dB
[87]	Generate DTMF "7" (852+1209 Hz)	[76]	Set playback path gain to -30 dB
[90]	Generate Dial tone (350+440 Hz)	[88]	Generate DTMF "8" (852+1336 Hz)
[91]	Generate Ringing tone (480+440 Hz)	[89]	Generate DTMF "9" (852+1477 Hz)
[94]	Generate bright musical note "A" (440+1320 Hz)		
[95]	Generate bright musical note "B" (494+1482 Hz)		
[96]	Generate bright musical note "C" (523+1569 Hz)		
[97]	Generate bright musical note "D" (587+1761 Hz)		
[97]	Generate bright musical note "D" (587+1761 Hz)		
[98]	Generate bright musical note "E" (659+1977 Hz)		
[99]	Generate bright musical note "F" (698+2094 Hz)		
[9A]	Generate bright musical note "G" (784+2352 Hz)		
[B4]	Generate musical note "A" (440 Hz)		
[B5]	Generate musical note "B" (494 Hz)		
[B6]	Generate musical note "C" (523 Hz)		
[B7]	Generate musical note "D" (587 Hz)		

[13]	Set "off" threshold to -44 dBm
[14]	Set "off" threshold to -42 dBm
[15]	Set "off" threshold to -40 dBm
[16]	Set "off" threshold to -38 dBm
[17]	Set "off" threshold to -35 dBm
[18]	Set "off" threshold to -32 dBm
[19]	Set "off" threshold to -29 dBm
[1A]	Set "off" threshold to -26 dBm
[1B]	Set "off" threshold to -23 dBm
[1C]	Set "off" threshold to -20 dBm
[1D]	Set "off" threshold to -17 dBm
[1E]	Set "off" threshold to -14 dBm
[1F]	Set "off" threshold to -11 dBm

1. All tones are generated at 0 dBm0 except for the high tones of DTMF which are at +3 dBm0.
2. The unit dBm0 represents a digital representation of an analog level; throughout this data sheet, the zero reference point of 0 dBm0 was measured with a Hitachi HD44238P CODEC which produces a 1.231Vrms analog signal when sent a "0 dBm0" digital code.
3. All letters and numbers contained in brackets ([]) represent Hexadecimal values.
4. The above hexadecimal code are sent LSB first.

DEFINITION OF THE L0 TO L4 LEVEL BITS

Table 4

L4	L3	L2	L1	L0	ENERGY LEVEL RECEIVED
0	0	0	0	0	<-48dBm0
0	0	0	1	0	-45dBm0
0	0	1	0	0	-42dBm0
0	0	1	0	1	-39dBm0
0	0	1	1	0	-36dBm0
0	0	1	1	1	-33dBm0
0	1	0	0	0	-30dBm0
0	1	0	0	1	-27dBm0
0	1	0	1	0	-24dBm0
0	1	0	1	1	-21dBm0
0	1	1	0	0	-18dBm0
0	1	1	0	1	-15dBm0
0	1	1	1	0	-12dBm0
0	1	1	1	1	-9dBm0
1	0	0	0	0	-6dBm0
1	0	0	0	1	-3dBm0
1	0	0	1	0	0dBm0
1	0	0	1	1	+3dBm0
1	0	1	0	0	+6dBm0
1	0	1	0	1	+9dBm0

POWER-DOWN MODE

The DS2132A can be placed into a low-power standby condition by sending the enter power-down command [04] to the DS2132A. The DS2132A will power down within 500 μ s after receiving the power-down command. The MCLK signal should still be applied to the DS2132A in the power-down mode. The CLK and FS signals may be either stopped or continued. In the power-down mode, the DS2132A will consume about 1 mA and the $\overline{\text{PD}}$ pin (Pin 1) will be forced low and the PD pin (Pin 5)

DEFINITION OF THE D0 TO D3 DTMF BITS

Table 5

D3	D2	D1	D0	DTMF DIGIT DETECTED
0	0	0	0	DTMF Digit "0"
0	0	0	1	DTMF Digit "1"
0	0	1	0	DTMF Digit "2"
0	0	1	1	DTMF Digit "3"
0	1	0	0	DTMF Digit "4"
0	1	0	1	DTMF Digit "5"
0	1	1	0	DTMF Digit "6"
0	1	1	1	DTMF Digit "7"
1	0	0	0	DTMF Digit "8"
1	0	0	1	DTMF Digit "9"
1	0	1	0	DTMF Digit "A"
1	0	1	1	DTMF Digit "B"
1	1	0	0	DTMF Digit "C"
1	1	0	1	DTMF Digit "D"
1	1	1	0	DTMF Digit "**"
1	1	1	1	DTMF Digit "#"

will be forced high. The $\overline{\text{PD}}$ and PD pins can be used to power-down the CODEC. See Figure 2. To exit the power-down mode, the exit power-down command [05] should be sent to the DS2132A. There is no need to issue a hardware reset via the $\overline{\text{RST}}$ pin; the device will reset itself. The DS2132A will power-up in the Idle mode. The microcontroller should wait 1 ms after issuing the exit power-down command before reinitializing the device.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 0	V_{IL}	-0.3		0.8	V	
Logic 1	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Supply	V_{CC}	4.5		5.5	V	

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		35	40	mA	1,2
Input Leakage	I_{LI}	-1.0		+1.0	μA	
Output Leakage	I_{LO}	-1.0		-1.0	μA	3
Output Current (2.4 V)	I_{OH}	-1.0		-1.0	mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	
Power-Down Current	I_{PD}		1		mA	1,2,4

NOTES:

1. $V_{CC} = 5.5V$; CLK=2.048 MHz; MCLK=16 MHz.
2. Outputs open; inputs swinging full supply levels.
3. PCMOUT and CDOUT are 3-stated.
4. Power-down mode.

DTMF RECEIVER CHARACTERISTICS(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Valid Detect Amplitude Range		-40		0	dBm0	1,2
Frequency Deviation Accept		± 1.5			%	3
Frequency Deviation Reject		± 3.5			%	3
Minimum Twist Accept Range		-10		+10	dB	4
Talk Off (Mitel Tape CM7291)			5		Hits	5
Noise Tolerance (Mitel Test Tape CM7291)			-12		dB	6

NOTES:

- 0 dBm0 = 1.231Vrms when sent through a Hitachi HD44238P CODEC as shown in Figure 1.
- Individual tone level of the DTMF pair with recording path gain set to 0db.
- Percent of nominal frequency for the individual tone; FS = 8 KHz ($\pm 0.1\%$).
- Twist = 20 LOG (High tone/Low tone).
- Talk Off is a measure of the speech immunity of a DTMF receiver; the lower the number of hits, the better the immunity.
- Three KHz bandlimited white noise, referenced to lowest amplitude in the DTMF pair.

DTMF DETECTION TIMING(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Tone Duration Accept		40			ms	
Tone Duration Reject				20	ms	
Interdigit Pause Accept		40			ms	
Interdigit Pause Reject				20	ms	

DTMF TONE GENERATOR CHARACTERISTICS(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DTMF Frequency Deviation (each tone of the pair)				± 1.0	%	1
Output Distortion (single tone)				-25	dB	2
DTMF Tone Level Twist			± 3		dB	3

NOTES:

- FS = 8.0 KHz $\pm 0.1\%$
- Total harmonic distortion relative to test tone signal.
- Twist = 20 LOG (High tone/Low tone).

DATA INPUT/OUTPUT **AC ELECTRICAL CHARACTERISTICS**

(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Clock Period	t_P	244		7813	ns	1,2
CLK Pulse Width High, Low	t_{WH}, t_{WL}	100			ns	2
CLK Rise, Fall Times	t_R, t_F			20	ns	2
Hold Time from CLK to FS	t_{HOLD}	0			ns	2
Setup Time from FS high CLK low	t_{SF}	50			ns	2
Hold Time from CLK low to FS low	t_{HF}	100			ns	2
Setup Time from PCMIN, CDIN to CLK low	t_{SD}	50			ns	2
Hold Time from PCMIN, CDIN to CLK low	t_{HD}	50			ns	2
Delay Time from CLK to Valid PCMOUT, CDOOUT	t_{DO}	10		150	ns	2
Delay Time from CLK to PCMOUT, CDOOUT 3-stated	t_{DZ}	20		150	ns	2

NOTES:

- At least nine CLK clocks must be received within first half of the FS period (62.5 μ s).
- See Figure 8.

MASTER CLOCK/RESET **AC ELECTRICAL CHARACTERISTICS**

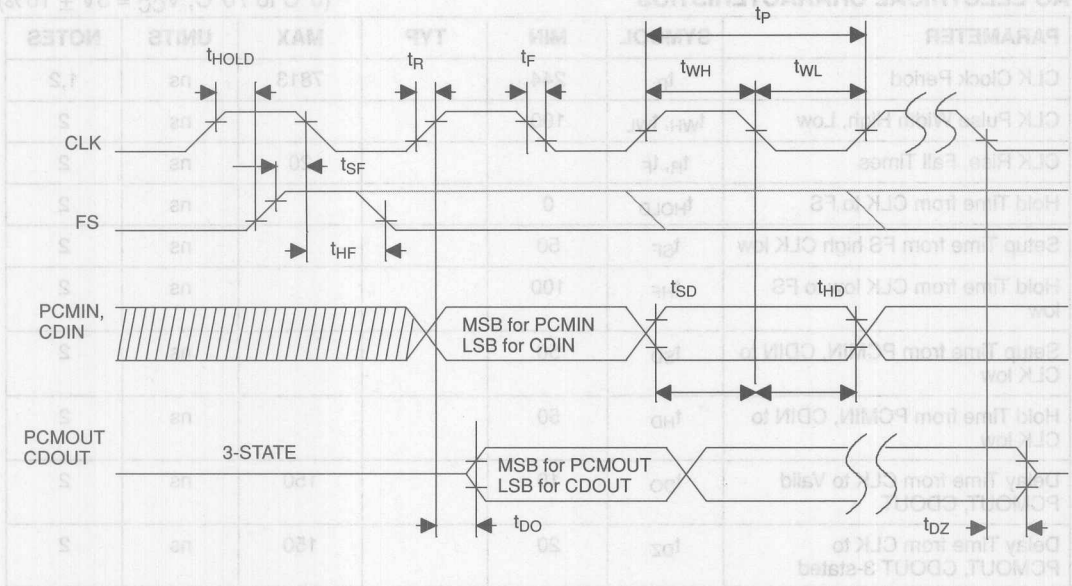
(0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}	62		84	ns	1,2
MCLK Duty Cycle		45		55	%	
MCLK Rise/Fall Times	t_{RM}, t_{FM}			10	ns	2
RST Pulse Width	t_{RST}	100			ms	2

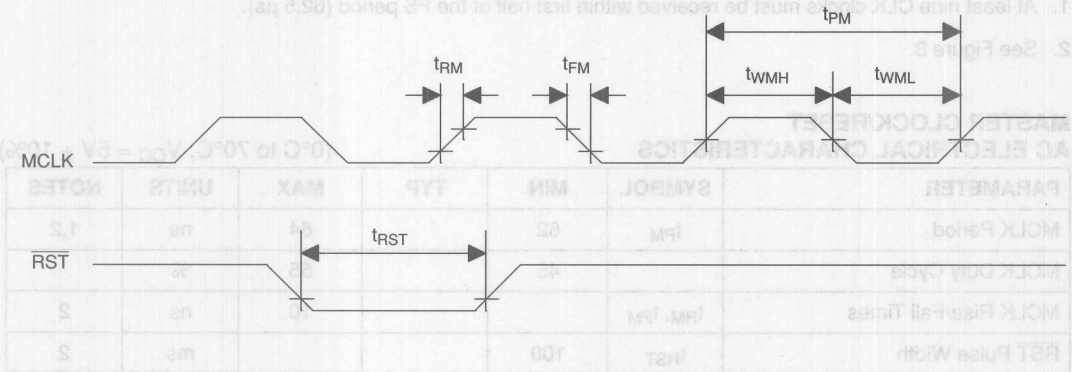
NOTES:

- MCLK = 12 to 16 MHz.
- See Figure 9.

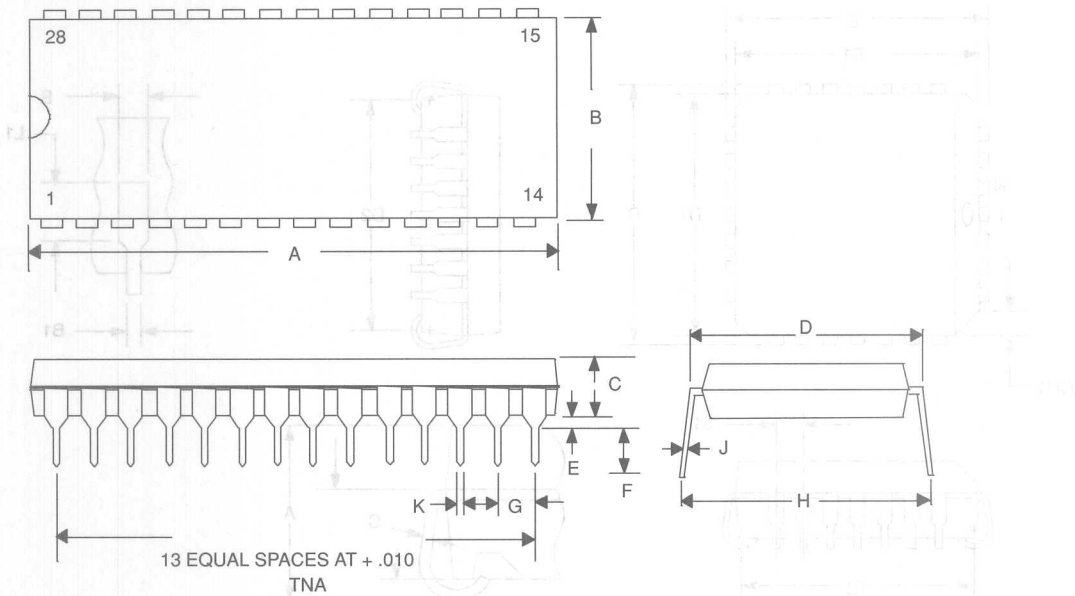
DATA I/O AC TIMING DIAGRAM Figure 8



MASTER CLOCK AND RESET AC TIMING DIAGRAM Figure 9

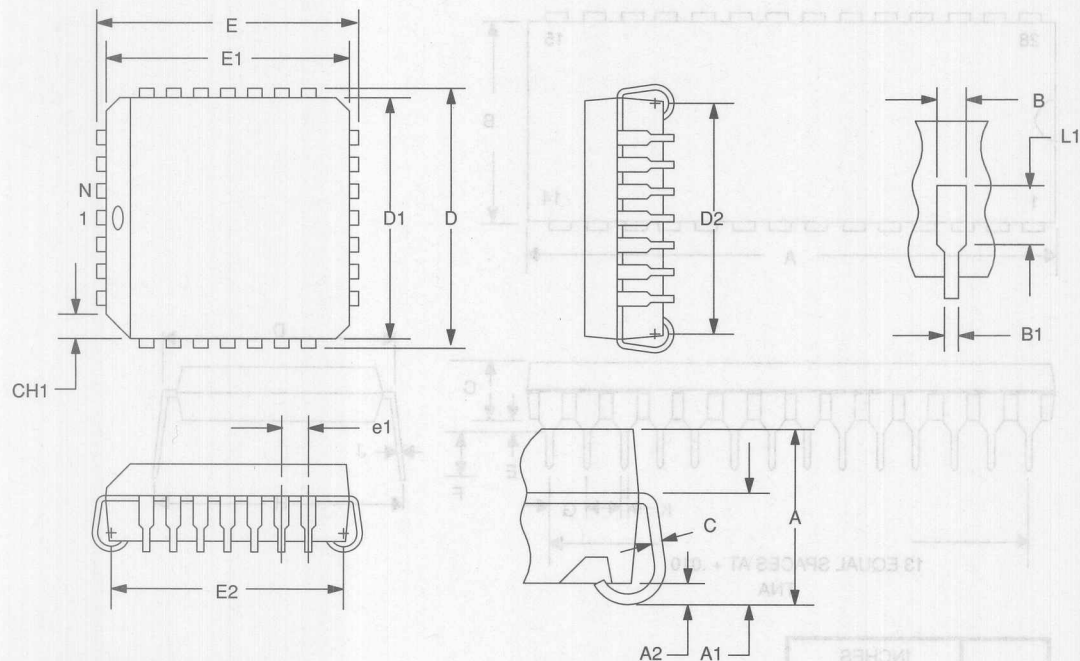


DS2132A DIGITAL ANSWERING MACHINE PROCESSOR



DIM	INCHES	
	MIN	MAX
A	1.445	1.470
B	0.530	0.550
C	0.140	0.160
D	0.600	0.625
E	0.015	0.040
F	0.120	0.145
G	0.090	0.110
H	0.600	0.680
J	0.008	0.012
K	0.015	0.022

DS2132AQ DIGITAL ANSWERING MACHINE PROCESSOR



DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	—
N	28	—
e1	0.050 BSC	
CH1	0.042	0.048

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
B	0.026	0.033
C	0.009	0.012
D	0.485	0.495
E	0.485	0.495
F	0.150	0.165
G	0.110	0.120
H	0.050	0.060
I	0.015	0.020
J	0.015	0.020
K	0.015	0.020

DALLAS SEMICONDUCTOR

DS2164Q G.726 ADPCM Processor

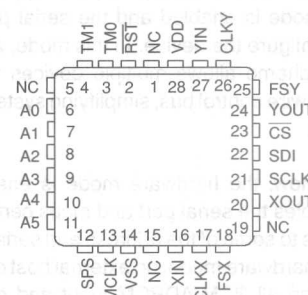
FEATURES

- Compresses/expands 64Kbps PCM voice to/from either 32Kbps, 24Kbps, or 16Kbps as per the CCITT/ITU G.726 specification
- Dual, fully independent channel architecture; device can be programmed to perform either:
 - two expansions
 - two compressions
 - one expansion and one compression
- Interconnects directly to combo-codec devices
- Input to output delay is less than 375 μ s
- Simple serial port used to configure the device
- Onboard Time Slot Assigner Circuit (TSAC) function allows data to be input/output at various time slots
- Supports Channel Associated Signaling
- Each channel can be independently idled or placed into bypass
- Available hardware mode requires no host processor; ideal for voice storage applications
- Backward-compatible with the DS2165 ADPCM Processor Chip
- Single +5V supply; low-power CMOS technology
- Available in 28-pin PLCC

DESCRIPTION

The DS2164Q ADPCM Processor Chip is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 64Kbps voice data down to (up from) either 32Kbps, 24Kbps, or 16Kbps. The compression follows the algorithm specified by CCITT Recommendation G.726. The DS2164Q can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

PIN ASSIGNMENT



28-Pin PLCC

OVERVIEW

The DS2164Q contains three major functional blocks: a high performance (10 MIPS) DSP engine, two independent PCM interfaces (X and Y) which connect directly to serial Time Division Multiplexed (TDM) backplanes, and a serial port that can configure the device on-the-fly via an external controller. A 10 MHz master clock is required by the DSP engine. The DS2164Q can be configured to perform either two expansions, two compressions, or one expansion and one compression. The PCM/ADPCM data interfaces support data rates from 256 KHz to 4.096 MHz. Typically, the PCM data rates

will be 1.544 MHz for μ -law and 2.048 MHz for A-law. Each channel on the device samples the serial input PCM or ADPCM bit stream during a user-programmed input time slot, processes the data and outputs the result during a user-programmed output time slot.

Each PCM interface has a control register which specifies functional characteristics (compress, expand, bypass, and idle), data format (μ -law or A-law), and algorithm reset control. With the SPS pin strapped high, the software mode is enabled and the serial port can be used to configure the device. In this mode, a novel addressing scheme allows multiple devices to share a common 3-wire control bus, simplifying system-level interconnect.

With SPS low, the hardware mode is enabled. This mode disables the serial port and maps certain control register bits to some of the address and serial port pins. Under the hardware mode, no external host controller is required and all PCM/ADPCM input and output time slots default to time slot 0.

HARDWARE RESET

RST allows the user to reset both channel algorithms and the contents of the internal registers. This pin must be held low for at least 1 ms on system power-up after the master clock is stable to ensure that the device has initialized properly. $\overline{\text{RST}}$ should also be asserted when changing to or from the hardware mode. $\overline{\text{RST}}$ clears all bits of the Control Register for both channels except the IPD bits; the IPD bits for both channels are set to 1.

SOFTWARE MODE

Tying SPS high enables the software mode. In this mode, an external host controller writes configuration

data to the DS2164Q via the serial port through inputs SCLK, SDI, and $\overline{\text{CS}}$. (See Figure 2.) Each write to the DS2164Q is either a 2-byte write or a 4-byte write. A 2-byte write consists of the Address/Command Byte (ACB), followed by a byte to configure the Control Register (CR) for either the X or Y channel. The 4-byte write consists of the ACB, followed by a byte to configure the CR, and then one byte to set the input time slot and another byte to set the output time slot.

ADDRESS/COMMAND BYTE

In the software mode, the address/command byte is the first byte written to the serial port; it identifies which of the 64 possible ADPCM processors sharing the port wiring is to be updated. Address data must match that at inputs A0 to A5. If no match occurs, the device ignores the following configuration data. If an address match occurs, the next three bytes written are accepted as control, input and output time slot data. Bit ACB.6 determines which side (X or Y) of the device is to be updated. The PCM and ADPCM outputs are tristated during register updates.

CONTROL REGISTER

The control register establishes idle, algorithm reset, bypass, data format and channel coding for the selected channel.

The X and Y side PCM interfaces can be independently disabled (output 3-stated) via IPD. When IPD is set for both channels, the device enters a low-power standby mode. In this mode, the serial port must not be operated faster than 39 KHz.

ALRST resets the algorithm coefficients for the selected channel to their initial values. ALRST will be cleared by the device when the algorithm reset is complete.

OVERVIEW
The DS2164Q contains three major functional blocks: a high performance (10 MIPS) DSP engine, two independent PCM interfaces (X and Y) which connect directly to serial time division multiplexed (TDM) backplanes, and a serial port that can configure the device on-the-fly via an external controller. A 10 MHz master clock is required by the DSP engine. The DS2164Q can be configured to perform either two expansions, two compressions, or one expansion and one compression. The PCM/ADPCM data interfaces support data rates from 256 KHz to 4.096 MHz. Typically, the PCM data rates

DESCRIPTION
The DS2164Q ADPCM Processor Chip is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 8-KHz voice data down to (up from) either 3.2-KHz, 2.4-KHz, or 1.8-KHz. The compression follows the algorithm specified by CCITT Recommendation G.726. The DS2164Q can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
2	RST	I	Reset. A high-low-high transition resets the algorithm. The device should be reset on power up and when changing to or from the hardware mode.
3 4	TM0 TM1	I	Test Modes 0 and 1. Tie to V _{SS} for normal operation.
6 7 8 9 10 11	A0 A1 A2 A3 A4 A5	I	Address Select. A0 = LSB; A5 = MSB Must match address/command word to enable the serial port.
12	SPS	I	Serial Port Select. Tie to V _{DD} to select the serial port; tie to V _{SS} to select the hardware mode.
13	MCLK	I	Master Clock. 10 MHz clock for the ADPCM processing engine; may be asynchronous to SCLK, CLKX, and CLKY.
14	V _{SS}	—	Signal Ground. 0.0 volts.
16	XIN	I	X Data In. Sampled on falling edge of CLKX during selected time slots.
17	CLKX	I	X Data Clock. Data clock for the X side PCM interface; must be synchronous with FSX.
18	FSX	I	X Frame Sync. 8 KHz frame sync for the X side PCM interface.
20	XOUT	O	X Data Output. Updated on rising edge of CLKX during selected time slots.
21	SCLK	I	Serial Data Clock. Used to write to the serial port registers.
22	SDI	I	Serial Data In. Data for onboard control registers; sampled on the rising edge of SCLK. LSB sent first.
23	$\overline{\text{CS}}$	I	Chip Select. Must be low to write to the serial port.
24	YOUT	O	Y Data Output. Updated on rising edge of CLKY during selected time slots.
25	FSY	I	Y Frame Sync. 8 KHz frame sync for the Y side PCM interface.
26	CLKY	I	Y Data Clock. Data clock for the Y side PCM interface; must be synchronous with FSY.
27	YIN	I	Y Data In. Sampled on falling edge of CLKY during selected time slots.
28	V _{DD}	—	Positive Supply. 5.0 volts.

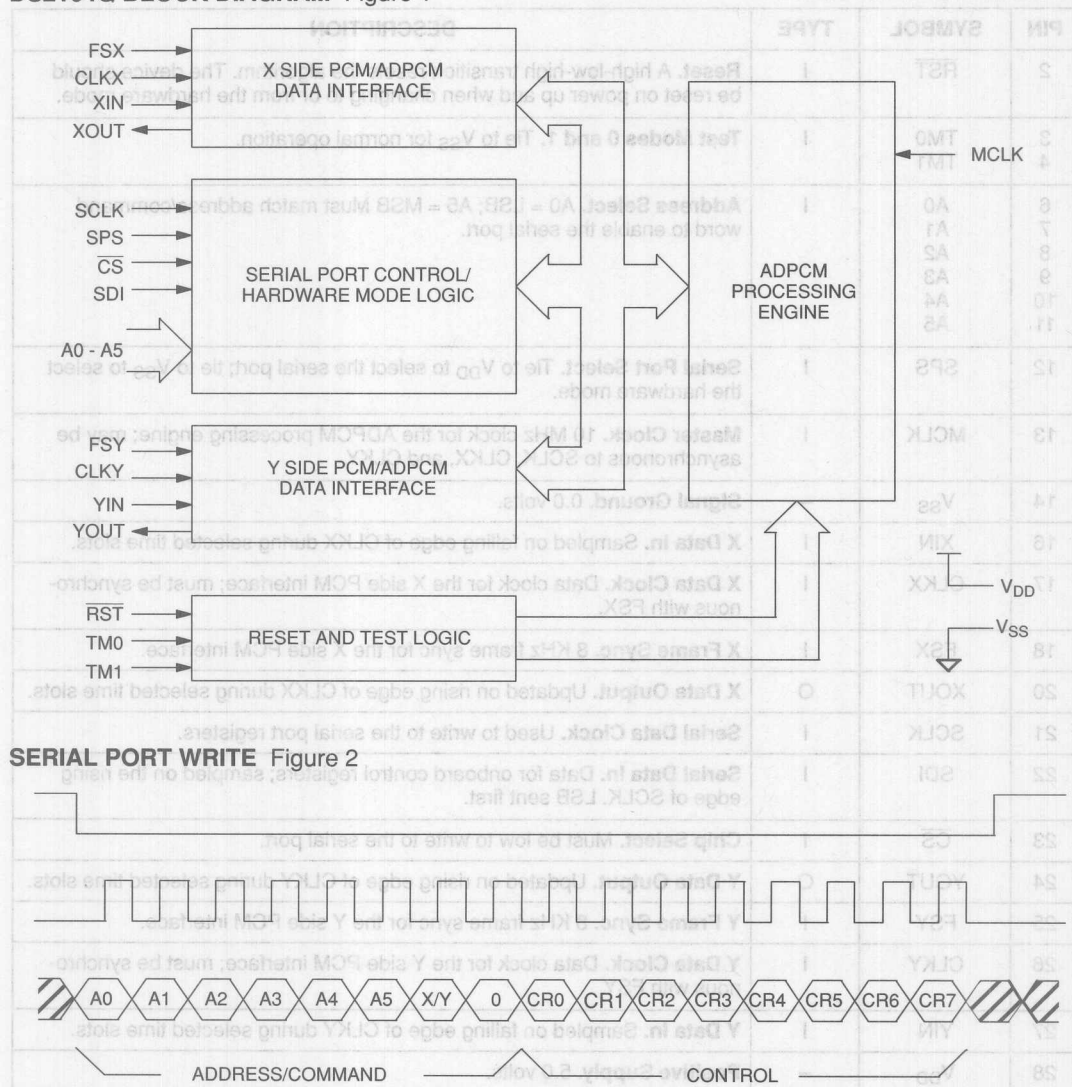
NOTE:

1. Pin 28 is shown.

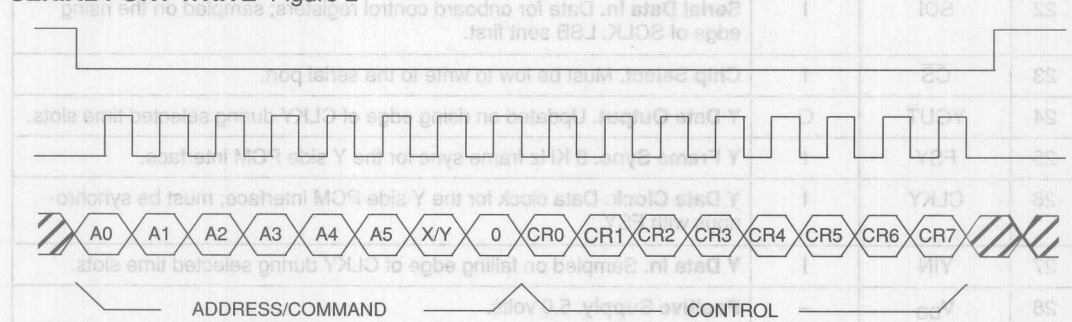
A test (UIA = 0) and a test (UIA = 1) PCM coding is indicated. During bypass, no expansion or compression occurs. Bypass operates on byte-wide (8 bits) slots when CPREX is set and on nibble-wide (4 bits) slots when CPREX is cleared.

The device is enabled when BYP is set and IPD is cleared. During bypass, no expansion or compression occurs. Bypass operates on byte-wide (8 bits) slots when CPREX is set and on nibble-wide (4 bits) slots when CPREX is cleared.

DS2164Q BLOCK DIAGRAM Figure 1



SERIAL PORT WRITE Figure 2

**NOTE:**

1. A 2-byte write is shown.

The bypass feature is enabled when BYP is set and IPD is cleared. During bypass, no expansion or compression occurs. Bypass operates on byte-wide (8 bits) slots when CP/EX is set and on nibble-wide (4 bits) slots when CP/EX is cleared.

A-law ($U/\bar{A} = 0$) and μ -law ($U/\bar{A} = 1$) PCM coding is independently selected for the X and Y channels via CR.2. If BYP and IPD are cleared, then CP/EX determines if the input data is to be compressed or expanded.

ADDRESS/COMMAND BYTE Figure 3

(MSB)	12A	A5	A4	A3	A2	A1	(LSB)
—	X/Y	A5	A4	A3	A2	A1	A0
SYMBOL	POSITION	NAME AND DESCRIPTION					
—	ACB.7	Reserved; must be 0 for proper operation					
X/Y	ACB.6	X/Y Channel Select 0 = update channel Y characteristics 1 = update channel X characteristics					
A5	ACB.5	MSB of Device Address					
A4	ACB.4						
A3	ACB.3						
A2	ACB.2						
A1	ACB.1						
A0	ACB.0	LSB of Device Address					

CONTROL REGISTER Figure 4

(MSB)	AS0	AS1	IPD	ALRST	BYP	U/A	AS2	(LSB)
SYMBOL	POSITION	NAME AND DESCRIPTION						
AS0	CR.7	Algorithm Select 0. See Table 2.						
AS1	CR.6	Algorithm Select 1. See Table 2.						
IPD	CR.5	Idle and Power Down. 0 = channel enabled 1 = channel disabled (output 3-stated)						
ALRST	CR.4	Algorithm Reset. 0 = normal operation 1 = reset algorithm for selected channel						
BYP	CR.3	Bypass. 0 = normal operation 1 = bypass selected channel						
U/A	CR.2	Data Format. 0 = A-law 1 = μ -law						
AS2	CR.1	Algorithm Select 2. See Table 2.						
CP/EX	CR.0	Channel Coding. 0 = expand (decode) selected channel 1 = compress (encode) selected channel						

ALGORITHM SELECT BITS Table 2

ALGORITHM SELECTED		AS2	AS1	AS0
DA	64Kbps to/from 32Kbps	0	0	0
	64Kbps to/from 24Kbps	1	1	1
	64Kbps to/from 16Kbps	1	0	1

INPUT TIME SLOT REGISTER Figure 5

(MSB)			(LSB)				
—	—	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
—	ITR.7	Reserved; must be 0 for proper operation.
—	ITR.6	Reserved; must be 0 for proper operation.
D5	ITR.5	MSB of input time slot register.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input time slot register.

OUTPUT TIME SLOT REGISTER Figure 6

(MSB)			(LSB)				
—	—	D5	D4	D3	D2	D1	D0

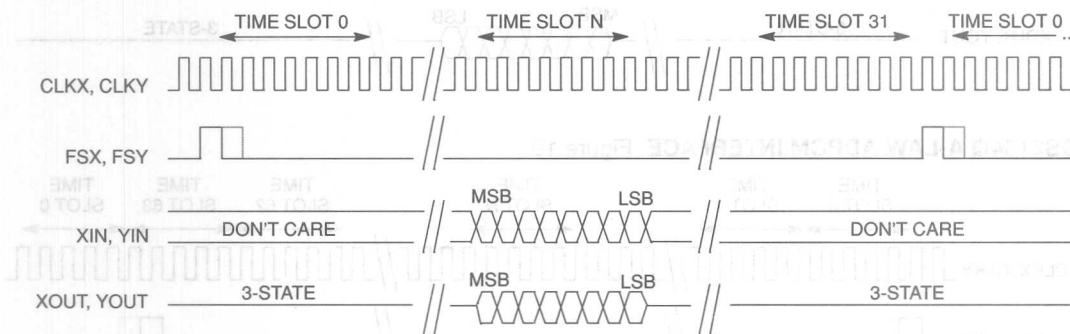
SYMBOL	POSITION	NAME AND DESCRIPTION
—	OTR.7	Reserved; must be 0 for proper operation.
—	OTR.6	Reserved; must be 0 for proper operation.
D5	OTR.5	MSB of output time slot register.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output time slot register.

TIME SLOT ASSIGNMENT/ORGANIZATION

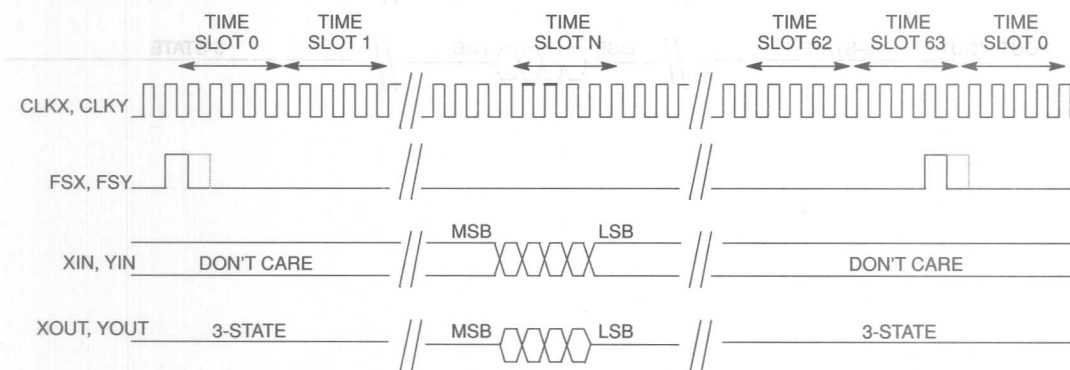
Onboard counters establish when PCM and ADPCM I/O occurs. The counters are programmed via the time slot registers. Time slot size (number of bits wide) is determined by the state of CP/\overline{EX} . The number of time slots available is determined by both the state of CP/\overline{EX} and U/\overline{A} . (See Figures 7 through 10.) For example, if the X channel is set to compress ($CP/\overline{EX} = 1$) and it is set to

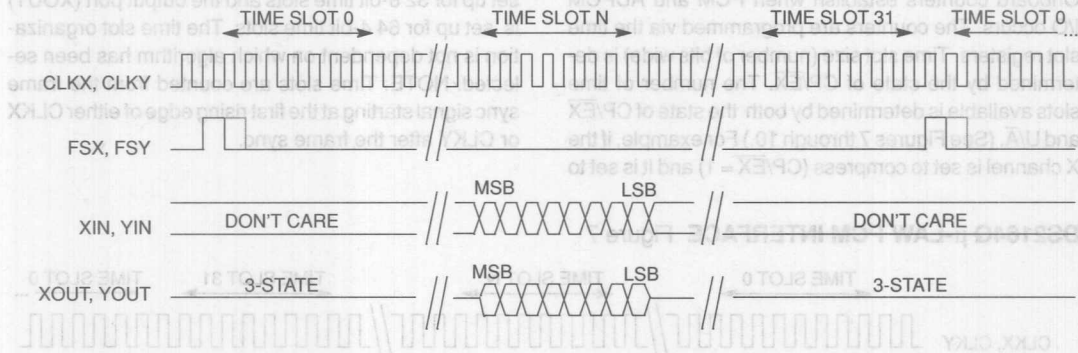
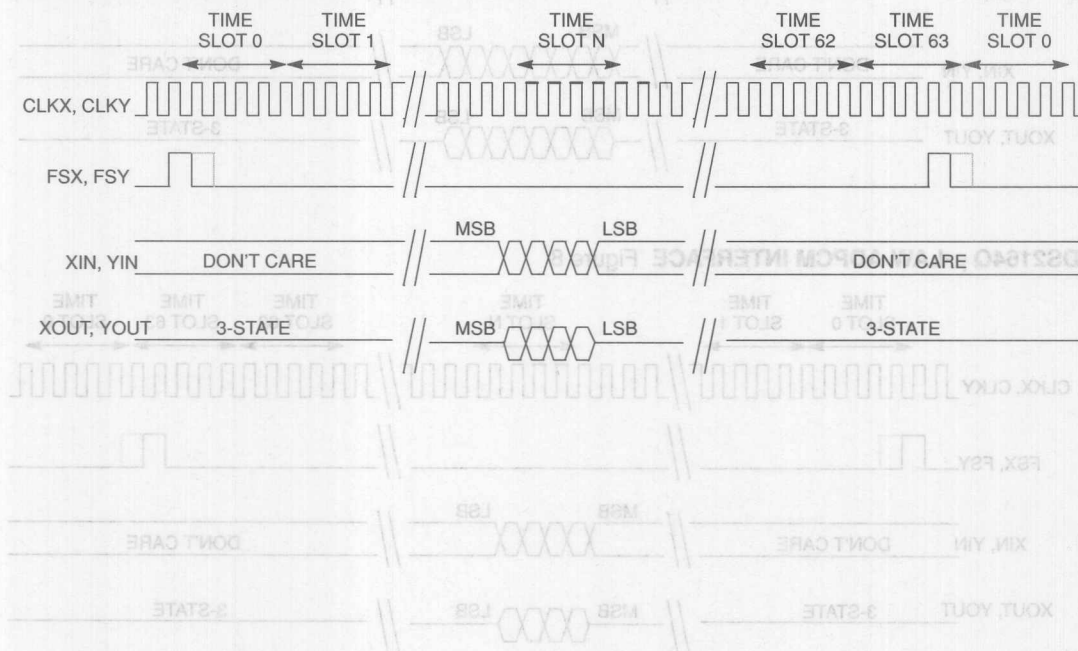
expect μ -law data ($U/\overline{A} = 1$), then the input port (XIN) is set up for 32 8-bit time slots and the output port (XOUT) is set up for 64 4-bit time slots. The time slot organization is not dependent on which algorithm has been selected. NOTE: Time slots are counted from the frame sync signal starting at the first rising edge of either CLKX or CLKY after the frame sync.

DS2164Q μ -LAW PCM INTERFACE Figure 7



DS2164Q μ -LAW ADPCM INTERFACE Figure 8



DS2164Q A-LAW PCM INTERFACE Figure 9**DS2164Q A-LAW ADPCM INTERFACE** Figure 10

HARDWARE MODE

The hardware mode is intended for applications that do not have an external controller available or do not require the extended features offered by the serial port. Tying the SPS pin to V_{SS} disables the serial port, clears

all internal register bits and maps the IPD, U/\bar{A} , and CP/EX bits for both channels to external bits. (See Table 3.) In the hardware mode, both the input and output time slots default to time slot 0.

HARDWARE MODE Table 3

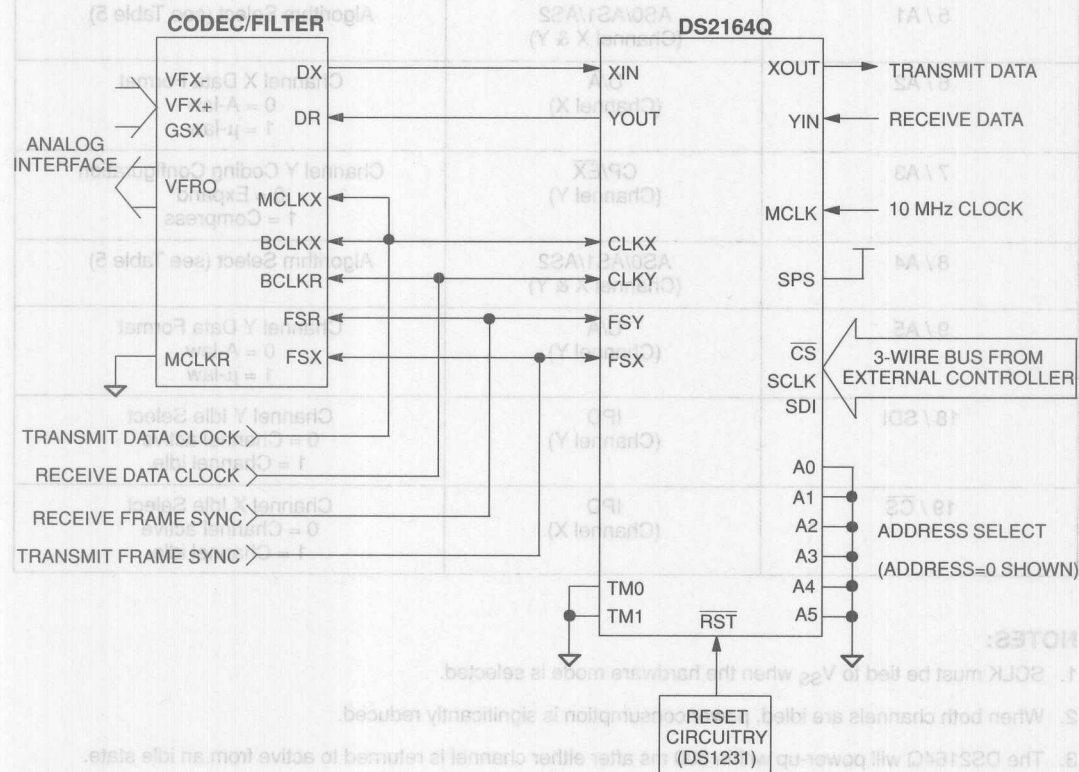
PIN # / NAME	REG. LOCATION	NAME AND DESCRIPTION
4 / A0	CP/EX (Channel X)	Channel X Coding Configuration 0 = Expand 1 = Compress
5 / A1	AS0/AS1/AS2 (Channel X & Y)	Algorithm Select (see Table 5)
6 / A2	U/\bar{A} (Channel X)	Channel X Data Format 0 = A-law 1 = μ -law
7 / A3	CP/EX (Channel Y)	Channel Y Coding Configuration 0 = Expand 1 = Compress
8 / A4	AS0/AS1/AS2 (Channel X & Y)	Algorithm Select (see Table 5)
9 / A5	U/\bar{A} (Channel Y)	Channel Y Data Format 0 = A-law 1 = μ -law
18 / SDI	IPD (Channel Y)	Channel Y Idle Select 0 = Channel active 1 = Channel idle
19 / \overline{CS}	IPD (Channel X)	Channel X Idle Select 0 = Channel active 1 = Channel idle

NOTES:

1. SCLK must be tied to V_{SS} when the hardware mode is selected.
2. When both channels are idled, power consumption is significantly reduced.
3. The DS2164Q will power-up within 800 ms after either channel is returned to active from an idle state.

ALGORITHM SELECT FOR HARDWARE MODE Table 4

ALGORITHM	CONFIGURATION OF A1 AND A4
64Kbps to/from 32Kbps	Tie both A1 and A4 to V_{SS} .
64Kbps to/from 24Kbps	Hold A1 and A4 low during a hardware reset; take both A1 and A4 high after the RST pin has returned high (allow 3 μ s after RST returns high before taking A1 and A4 high).
64Kbps to/from 16Kbps	Tie both A1 and A4 to V_{DD} .

DS2164Q CONNECTION TO CODEC/FILTER Figure 11**NOTE:****Suggested Codec/Filters**

TP305X	National Semiconductor
ETC505X	SGS-Thomson Microelectronics
MC1455XX	Motorola
TCM29CXX	Texas Instruments
HD44238C	Hitachi

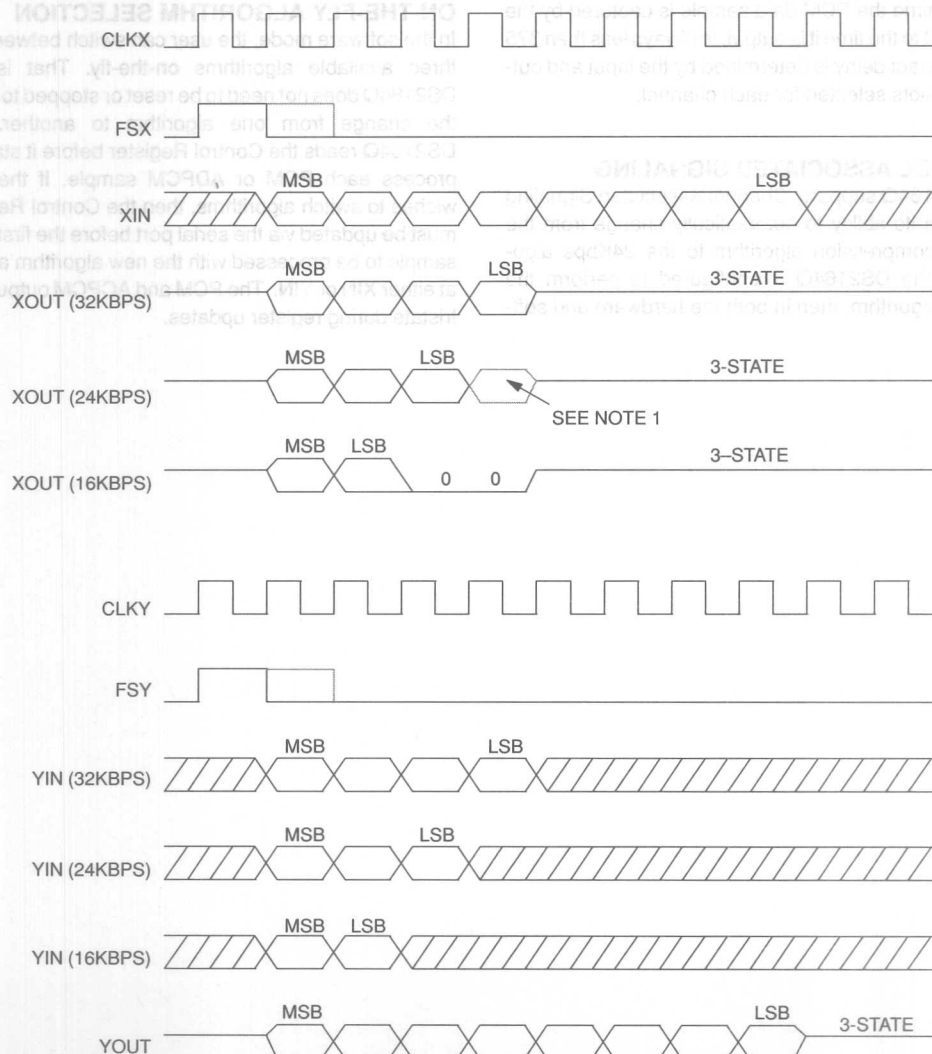
*other generic Codec/Filter devices can be substituted.

PCM AND ADPCM INPUT/OUTPUT

Since the organization of the input and output time slots on the DS2164Q does not depend on the algorithm selected, it always assumes that PCM input and output will be in 8-bit bytes and that ADPCM input and output will be in 4-bit bytes. Figure 12 demonstrates how the DS2164Q handles the I/O for the three different algo-

rithms. In the figure, it is assumed that channel X is in the compression mode ($CP/\overline{EX} = 1$) and channel Y is in the expansion mode ($CP/\overline{EX} = 0$). Also, it is assumed that both the input and output time slots for both channels are set to 0.

PCM AND ADPCM I/O EXAMPLE Figure 12



NOTE:

1. The bit after the LSB in the 24Kbps ADPCM output will only be a 1 when the DS2164Q is operated in the software mode and is programmed to perform 24Kbps compression; in all other configurations, it will be a 0.

TIME SLOT RESTRICTIONS

Under certain conditions, the DS2164Q does contain some restrictions on the output time slots that are available. These restrictions are covered in detail in a separate application note. No restrictions occur if the DS2164Q is operated in the hardware mode.

INPUT TO OUTPUT DELAY

With all three compressions algorithms, the total delay, from the time the PCM data sample is captured by the DS2164Q to the time it is output, is always less than 375 μ s. The exact delay is determined by the input and output time slots selected for each channel.

CHANNEL ASSOCIATED SIGNALING

The DS2164Q supports Channel Associated Signaling (CAS) via its ability to automatically change from the 32Kbps compression algorithm to the 24Kbps algorithm. If the DS2164Q is configured to perform the 32Kbps algorithm, then in both the hardware and soft-

ware mode, it will sense the frame sync inputs (FSX and FSY) for a double wide frame sync pulse. Whenever the DS2164Q receives a double wide pulse, it will automatically switch from the 32Kbps algorithm to the 24Kbps algorithm. Switching to the 24Kbps algorithm allows the user to insert signaling data into the LSB bit position of the ADPCM output because this bit does not contain any useful speech information.

ON-THE-FLY ALGORITHM SELECTION

In the software mode, the user can switch between the three available algorithms on-the-fly. That is, the DS2164Q does not need to be reset or stopped to make the change from one algorithm to another. The DS2164Q reads the Control Register before it starts to process each PCM or ADPCM sample. If the user wishes to switch algorithms, then the Control Register must be updated via the serial port before the first input sample to be processed with the new algorithm arrives at either XIN or YIN. The PCM and ADPCM outputs will tristate during register updates.



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground

-1.0V to +7.0V

Operating Temperature

0°C to 70°C

Storage Temperature

-55°C to +125°C

Soldering Temperature

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		20		mA	1,2
Idle Supply Current	I_{DDPD}		1		mA	1,2,3
Input Leakage	I_I	-1.0		+1.0	μA	
Output Leakage	I_O	-1.0		+1.0	μA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. CLKX = CLKY = 1.544 MHz; MCLK = 10 MHz.
2. Outputs open; inputs swinging full supply levels.
3. Both channels in idle mode.
4. XOUT and YOUT are 3-stated.

PCM INTERFACE**AC ELECTRICAL CHARACTERISTICS**(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLKX, CLKY Period	t_{PXY}	244		3906	ns	1
CLKX, CLKY Pulse Width	t_{WXYL} t_{WXYH}	100			ns	
CLKX, CLKY Rise/Fall Times	t_{RXY} t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	2
Setup Time from FSX, FSY high to CLKX, CLKY low	t_{SF}	50			ns	2
Hold Time from CLKX, CLKY low to FSX, FSY low	t_{HF}	100			ns	2
Setup Time for XIN, YIN to CLKX, CLKY low	t_{SD}	50			ns	2
Hold Time for XIN, YIN to CLKX, CLKY low	t_{HD}	50			ns	2
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	3
Delay Time from CLKX, CLKY to XOUT, YOUT 3-stated	t_{DXYZ}	20		150	ns	2,3,4

NOTES:

- Maximum width of FSX and FSY is one CLKX or CLKY period (except for signaling frames).
- Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10 ns maximum rise and fall times.
- Load = 150 pF + 2 LSTTL loads.
- For LSB of PCM or ADPCM byte.

MASTER CLOCK / RESET**AC ELECTRICAL CHARACTERISTICS**(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	1
MCLK Pulse Width	t_{WMH} , t_{WML}	45	50	55	ns	
MCLK Rise/Fall Times	t_{RM} , t_{FM}			10	ns	
RST Pulse Width	t_{RST}	1			ms	

NOTE:

- MCLK = 10 MHz \pm 500 ppm

SERIAL PORT AC ELECTRICAL CHARACTERISTICS

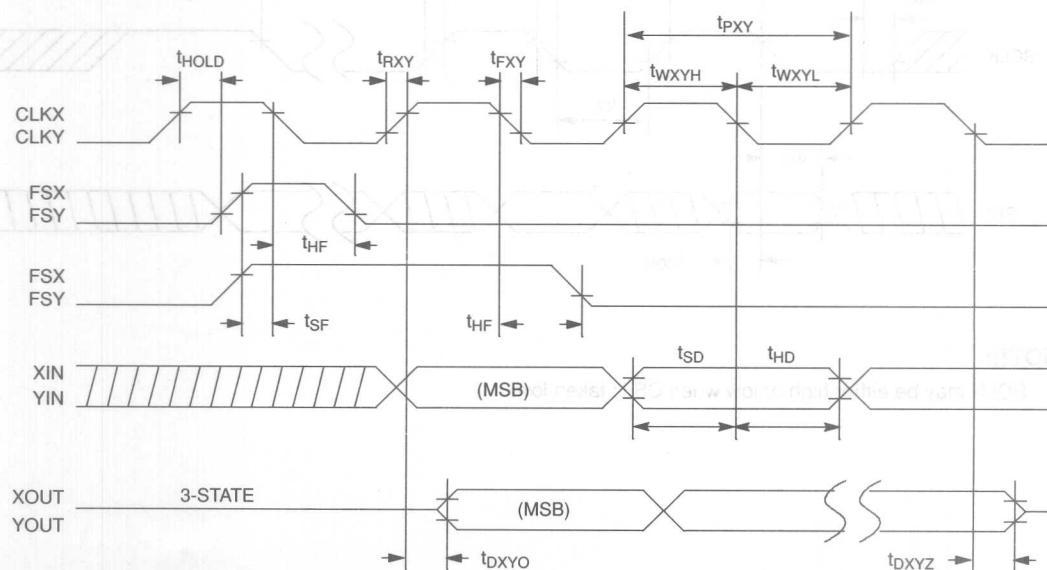
(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Time	t_R, t_F			100	ns	1
CS to SCLK Setup	t_{CC}	50			ns	1
SCLK to \overline{CS} Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to \overline{CS} Falling	t_{SCC}	50			ns	1

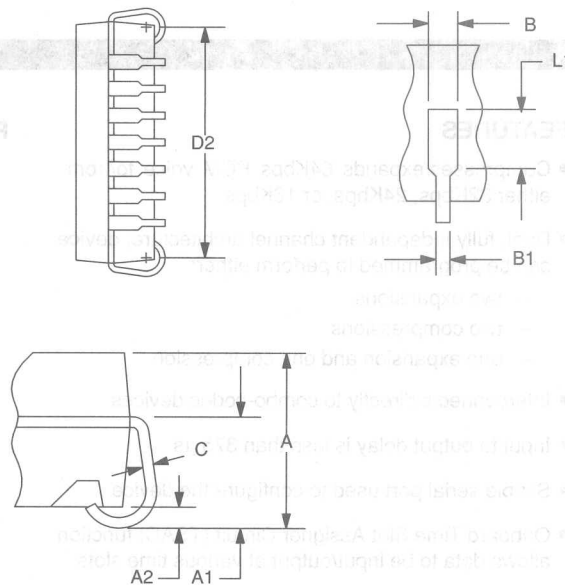
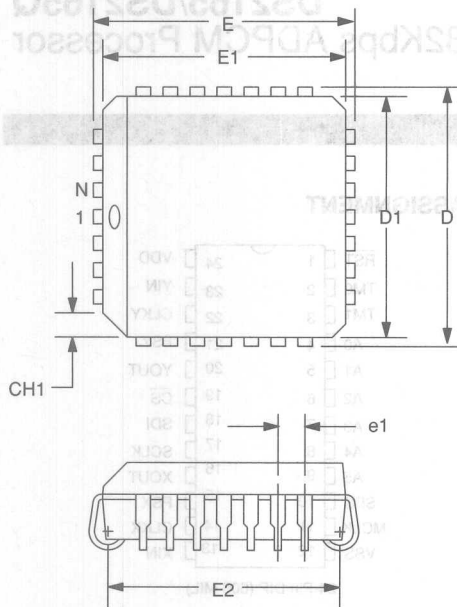
NOTE:

1. Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10ns maximum rise and fall times.

PCM INTERFACE AC TIMING DIAGRAM Figure 13



DS2164Q G.726 ADPCM PROCESSOR 28-PIN PLCC



DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	—
N	28	—
e1	0.050 BSC	
CH1	0.042	0.048

The DS2164Q ADPCM Processor is a dedicated digital signal processor (DSP) chip that has been optimized for use in a variety of applications. It is a 28-pin PLCC package that is compatible with the DS2164Q processor. The chip is designed to process audio signals and is capable of handling up to 16Kbps of data. It is a 28-pin PLCC package that is compatible with the DS2164Q processor. The chip is designed to process audio signals and is capable of handling up to 16Kbps of data. It is a 28-pin PLCC package that is compatible with the DS2164Q processor. The chip is designed to process audio signals and is capable of handling up to 16Kbps of data.

DALLAS

SEMICONDUCTOR

DS2165/DS2165Q

16/24/32Kbps ADPCM Processor

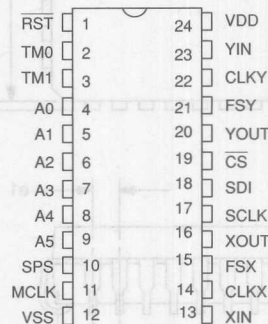
FEATURES

- Compresses/expands 64Kbps PCM voice to/from either 32Kbps, 24Kbps, or 16Kbps
- Dual, fully independent channel architecture; device can be programmed to perform either:
 - two expansions
 - two compressions
 - one expansion and one compression
- Interconnects directly to combo-codec devices
- Input to output delay is less than 375 μ s
- Simple serial port used to configure the device
- Onboard Time Slot Assigner Circuit (TSAC) function allows data to be input/output at various time slots
- Supports Channel Associated Signaling
- Each channel can be independently idled or placed into bypass
- Available hardware mode requires no host processor; ideal for voice storage applications
- Backward-compatible with the DS2167 ADPCM Processor Chip
- Single +5V supply; low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC

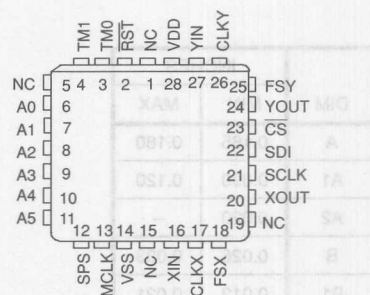
DESCRIPTION

The DS2165 ADPCM Processor Chip is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 64Kbps voice data down to (up from) either 32Kbps, 24Kbps, or 16Kbps. The compression to 32Kbps follows the algorithm specified by CCITT Recommendation G.721 (July 1986) and ANSI document

PIN ASSIGNMENT



24-Pin DIP (600 MIL)



28-Pin PLCC

A 3-volt Operation Version
is Available (DS2165QL)

T1.301 (April 1987). The compression to 24Kbps follows ANSI document T1.303. The compression to 16Kbps follows a proprietary algorithm developed by Dallas Semiconductor. The DS2165 can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

OVERVIEW

The DS2165 contains three major functional blocks: a high performance (10 MIPS) DSP engine, two independent PCM interfaces (X and Y) which connect directly to serial Time Division Multiplexed (TDM) backplanes, and a serial port that can configure the device on-the-fly via an external controller. A 10 MHz master clock is required by the DSP engine. The DS2165 can be configured to perform either two expansions, two compressions, or one expansion and one compression. The PCM/ADPCM data interfaces support data rates from 256 KHz to 4.096 MHz. Typically, the PCM data rates will be 1.544 MHz for μ -law and 2.048 MHz for A-law. Each channel on the device samples the serial input PCM or ADPCM bit stream during a user-programmed input time slot, processes the data and outputs the result during a user-programmed output time slot.

Each PCM interface has a control register which specifies functional characteristics (compress, expand, bypass, and idle), data format (μ -law or A-law), and algorithm reset control. With the SPS pin strapped high, the software mode is enabled and the serial port can be used to configure the device. In this mode, a novel addressing scheme allows multiple devices to share a common 3-wire control bus, simplifying system-level interconnect.

With SPS low, the hardware mode is enabled. This mode disables the serial port and maps certain control register bits to some of the address and serial port pins. Under the hardware mode, no external host controller is required and all PCM/ADPCM input and output time slots default to time slot 0.

HARDWARE RESET

RST allows the user to reset both channel algorithms and the contents of the internal registers. This pin must be held low for at least 1 ms on system power-up after the master clock is stable to ensure that the device has initialized properly. RST should also be asserted when changing to or from the hardware mode. RST clears all bits of the Control Register for both channels

except the IPD bits; the IPD bits for both channels are set to 1.

SOFTWARE MODE

Tying SPS high enables the software mode. In this mode, an external host controller writes configuration data to the DS2165 via the serial port through inputs SCLK, SDI, and \overline{CS} . (See Figure 2.) Each write to the DS2165 is either a 2-byte write or a 4-byte write. A 2-byte write consists of the Address/Command Byte (ACB), followed by a byte to configure the Control Register (CR) for either the X or Y channel. The 4-byte write consists of the ACB, followed by a byte to configure the CR, and then one byte to set the input time slot and another byte to set the output time slot.

ADDRESS/COMMAND BYTE

In the software mode, the address/command byte is the first byte written to the serial port; it identifies which of the 64 possible ADPCM processors sharing the port wiring is to be updated. Address data must match that at inputs A0 to A5. If no match occurs, the device ignores the following configuration data. If an address match occurs, the next three bytes written are accepted as control, input and output time slot data. Bit ACB.6 determines which side (X or Y) of the device is to be updated. The PCM and ADPCM outputs are tristated during register updates.

CONTROL REGISTER

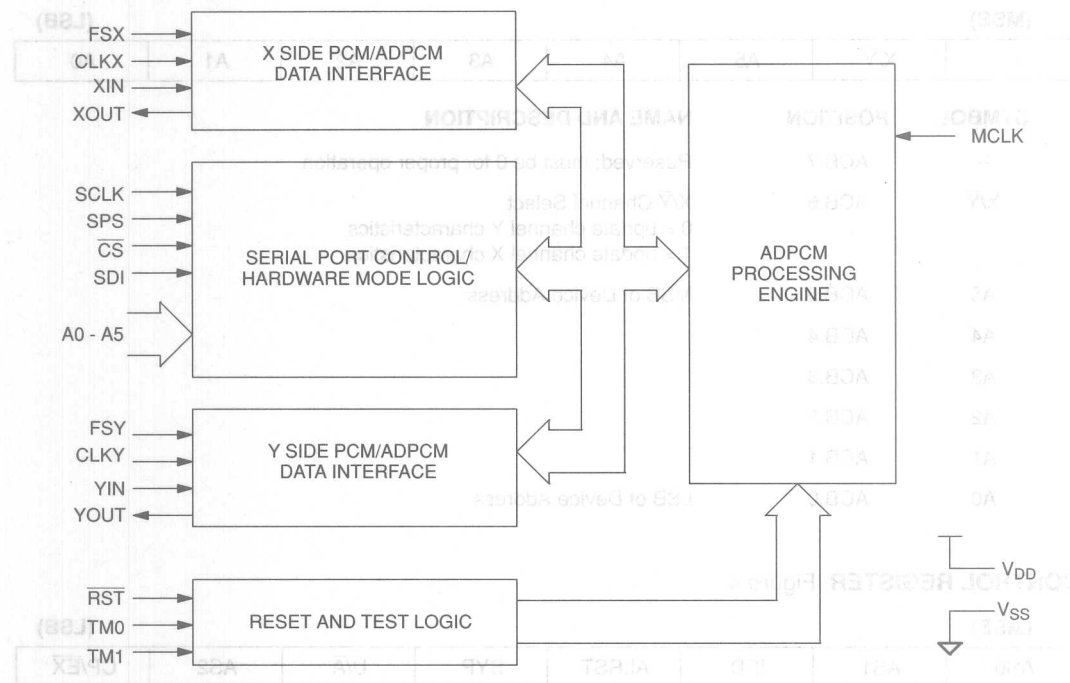
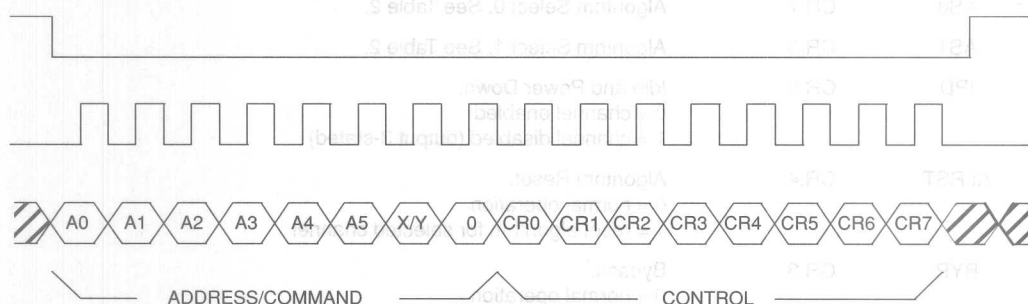
The control register establishes idle, algorithm reset, bypass, data format and channel coding for the selected channel.

The X and Y side PCM interfaces can be independently disabled (output 3-stated) via IPD. When IPD is set for both channels, the device enters a low-power standby mode. In this mode, the serial port must not be operated faster than 39 KHz.

ALRST resets the algorithm coefficients for the selected channel to their initial values. ALRST will be cleared by the device when the algorithm reset is complete.

PIN DESCRIPTION Table 11

PIN	SYMBOL	TYPE	DESCRIPTION
1	RST	I	Reset. A high-low-high transition resets the algorithm. The device should be reset on power up and when changing to or from the hardware mode.
2	TM0	I	Test Modes 0 and 1. Tie to V _{SS} for normal operation.
3	TM1	I	
4	A0	I	
5	A1	I	Address Select. A0 = LSB; A5 = MSB Must match address/command word to enable the serial port.
6	A2	I	
7	A3	I	
8	A4	I	
9	A5	I	
10	SPS	I	Serial Port Select. Tie to V _{DD} to select the serial port; tie to V _{SS} to select the hardware mode.
11	MCLK	I	Master Clock. 10 MHz clock for the ADPCM processing engine; may be asynchronous to SCLK, CLKX, and CLKY.
12	V _{SS}	—	Signal Ground. 0.0 volts.
13	XIN	I	X Data In. Sampled on falling edge of CLKX during selected time slots.
14	CLKX	I	X Data Clock. Data clock for the X side PCM interface; must be synchronous with FSX.
15	FSX	I	X Frame Sync. 8 KHz frame sync for the X side PCM interface.
16	XOUT	O	X Data Output. Updated on rising edge of CLKX during selected time slots.
17	SCLK	I	Serial Data Clock. Used to write to the serial port registers.
18	SDI	I	Serial Data In. Data for onboard control registers; sampled on the rising edge of SCLK. LSB sent first.
19	CS	I	Chip Select. Must be low to write to the serial port.
20	YOUT	O	Y Data Output. Updated on rising edge of CLKY during selected time slots.
21	FSY	I	Y Frame Sync. 8 KHz frame sync for the Y side PCM interface.
22	CLKY	I	Y Data Clock. Data clock for the Y side PCM interface; must be synchronous with FSY.
23	YIN	I	Y Data In. Sampled on falling edge of CLKY during selected time slots.
24	V _{DD}	—	Positive Supply. 5.0 volts (or 3.0 volts for DS2165QL).

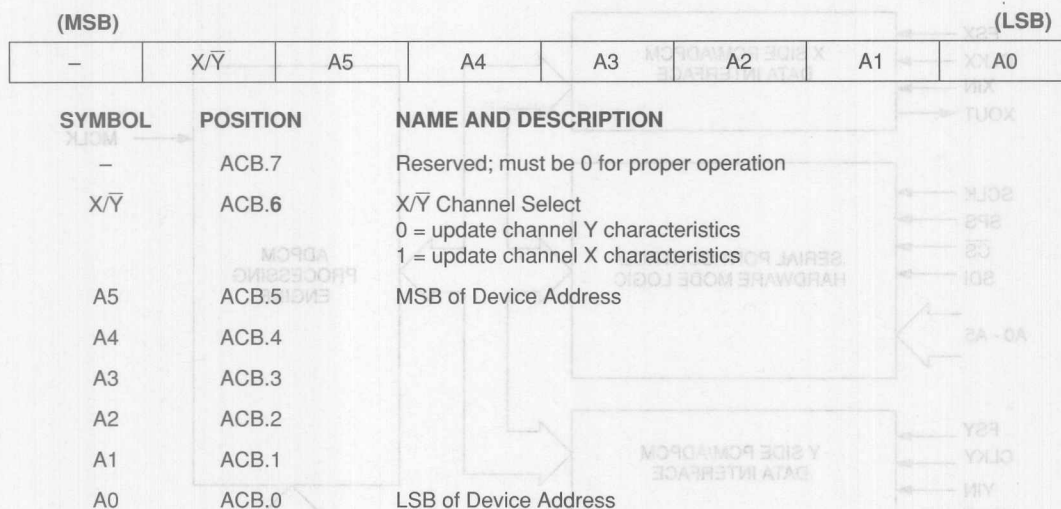
DS2165 BLOCK DIAGRAM Figure 1**SERIAL PORT WRITE** Figure 2**NOTE:**

1. A 2-byte write is shown.

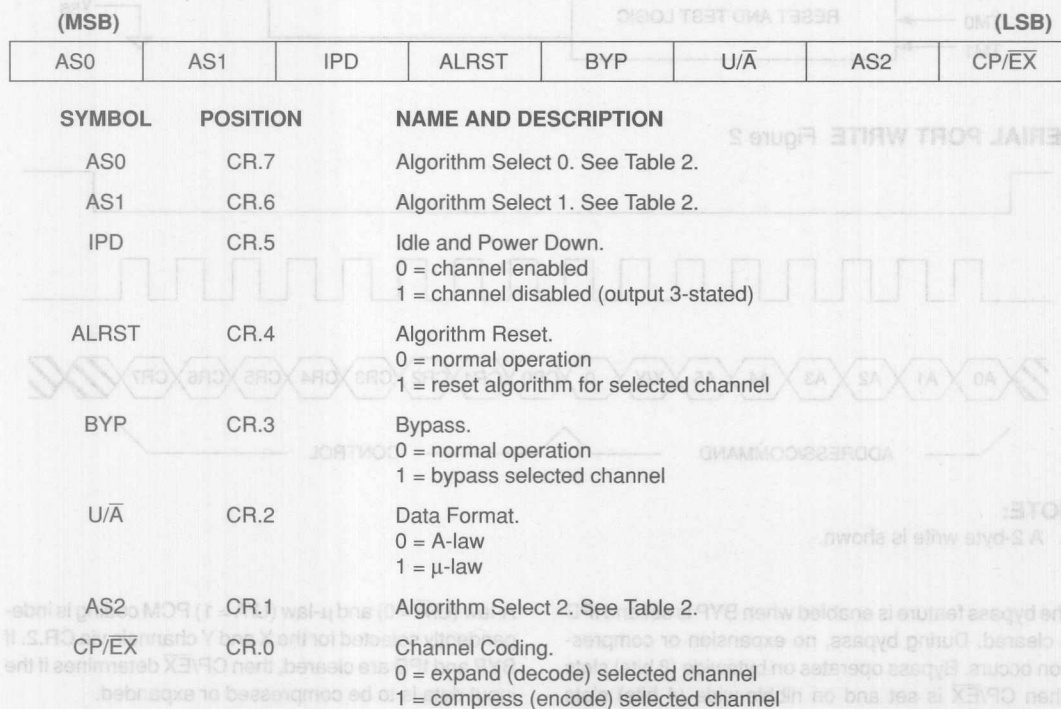
The bypass feature is enabled when BYP is set and IPD is cleared. During bypass, no expansion or compression occurs. Bypass operates on byte-wide (8 bits) slots when CP/EX is set and on nibble-wide (4 bits) slots when CP/EX is cleared.

A-law ($U/\bar{A} = 0$) and μ -law ($U/\bar{A} = 1$) PCM coding is independently selected for the X and Y channels via CR.2. If BYP and IPD are cleared, then CP/EX determines if the input data is to be compressed or expanded.

ADDRESS/COMMAND BYTE Figure 3



CONTROL REGISTER Figure 4



ALGORITHM SELECT BITS Table 2

ALGORITHM SELECTED	AS2	AS1	AS0
64Kbps to/from 32Kbps	0	0	0
64Kbps to/from 24Kbps	1	1	1
64Kbps to/from 16Kbps	1	0	1

INPUT TIME SLOT REGISTER Figure 5

(MSB)							(LSB)
—	—	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	ITR.7	Reserved; must be 0 for proper operation.
-	ITR.6	Reserved; must be 0 for proper operation.
D5	ITR.5	MSB of input time slot register.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input time slot register.

OUTPUT TIME SLOT REGISTER Figure 6

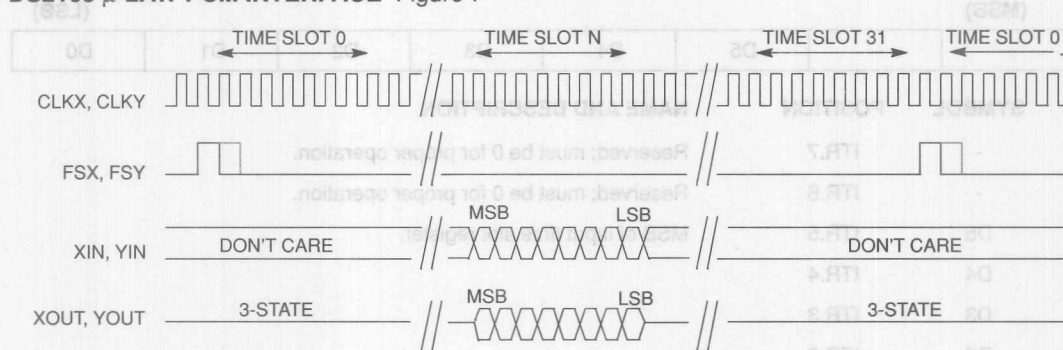
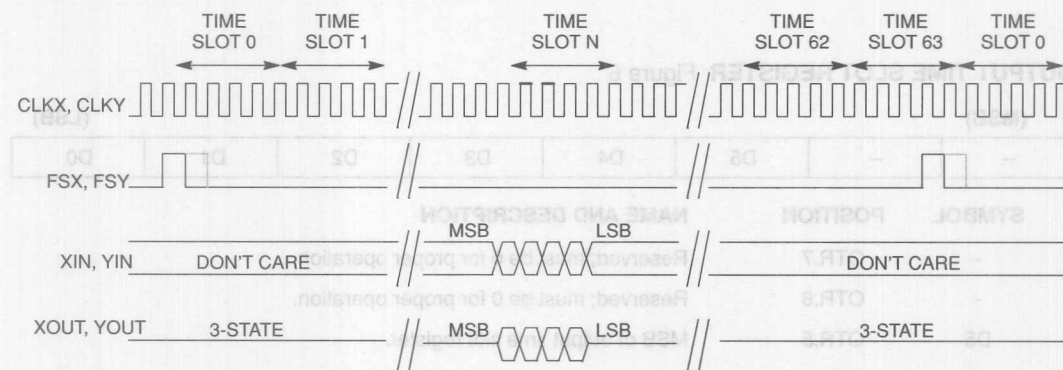
(MSB)							(LSB)
—	—	D5	D4	D3	D2	D1	D0

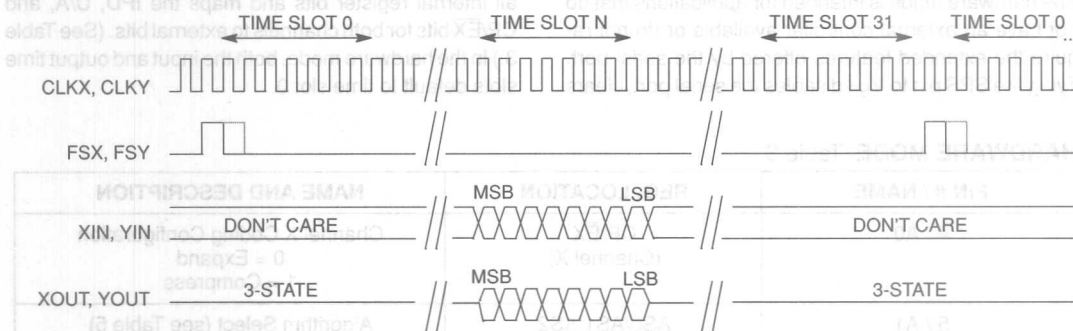
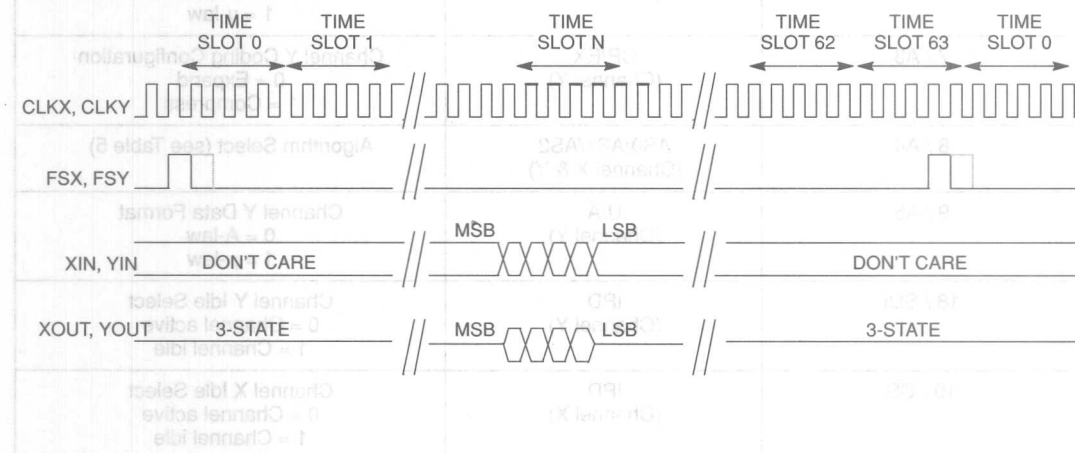
SYMBOL	POSITION	NAME AND DESCRIPTION
-	OTR.7	Reserved; must be 0 for proper operation.
-	OTR.6	Reserved; must be 0 for proper operation.
D5	OTR.5	MSB of output time slot register.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output time slot register.

TIME SLOT ASSIGNMENT/ORGANIZATION

Onboard counters establish when PCM and ADPCM I/O occurs. The counters are programmed via the time slot registers. Time slot size (number of bits wide) is determined by the state of CP/\overline{EX} . The number of time slots available is determined by both the state of CP/\overline{EX} and U/\overline{A} . (See Figures 7 through 10.) For example, if the X channel is set to compress ($CP/\overline{EX} = 1$) and it is set to

expect μ -law data ($U/\overline{A} = 1$), then the input port (XIN) is set up for 32 8-bit time slots and the output port (XOUT) is set up for 64 4-bit time slots. The time slot organization is not dependent on which algorithm has been selected. NOTE: Time slots are counted from the frame sync signal starting at the first rising edge of either CLKX or CLKY after the frame sync.

DS2165 μ -LAW PCM INTERFACE Figure 7**DS2165 μ -LAW ADPCM INTERFACE** Figure 8

DS2165 A-LAW PCM INTERFACE Figure 9**DS2165 A-LAW ADPCM INTERFACE** Figure 10**ALGORITHM SELECT FOR HARDWARE MODE** Table 4

ALGORITHM	CONFIGURATION OF A1 AND A4
8-kbps full-rate 8-kbps	The both A1 and A4 to V _{DD}
8-kbps full-rate 4-kbps	Hold A1 and A4 low during a hardware reset; take both A1 and A4 high after the RST pin has returned high (allow 3 μ s after RST returns high before taking A1 and A4 high)
4-kbps full-rate 4-kbps	The both A1 and A4 to V _{DD}

HARDWARE MODE

The hardware mode is intended for applications that do not have an external controller available or do not require the extended features offered by the serial port. Tying the SPS pin to V_{SS} disables the serial port, clears

all internal register bits and maps the IPD, U/\bar{A} , and CP/ $\bar{E}X$ bits for both channels to external bits. (See Table 3.) In the hardware mode, both the input and output time slots default to time slot 0.

HARDWARE MODE Table 3

PIN # / NAME	REG. LOCATION	NAME AND DESCRIPTION
4 / A0	CP/ $\bar{E}X$ (Channel X)	Channel X Coding Configuration 0 = Expand 1 = Compress
5 / A1	AS0/AS1/AS2 (Channel X & Y)	Algorithm Select (see Table 5)
6 / A2	U/\bar{A} (Channel X)	Channel X Data Format 0 = A-law 1 = μ -law
7 / A3	CP/ $\bar{E}X$ (Channel Y)	Channel Y Coding Configuration 0 = Expand 1 = Compress
8 / A4	AS0/AS1/AS2 (Channel X & Y)	Algorithm Select (see Table 5)
9 / A5	U/\bar{A} (Channel Y)	Channel Y Data Format 0 = A-law 1 = μ -law
18 / SDI	IPD (Channel Y)	Channel Y Idle Select 0 = Channel active 1 = Channel idle
19 / \bar{CS}	IPD (Channel X)	Channel X Idle Select 0 = Channel active 1 = Channel idle

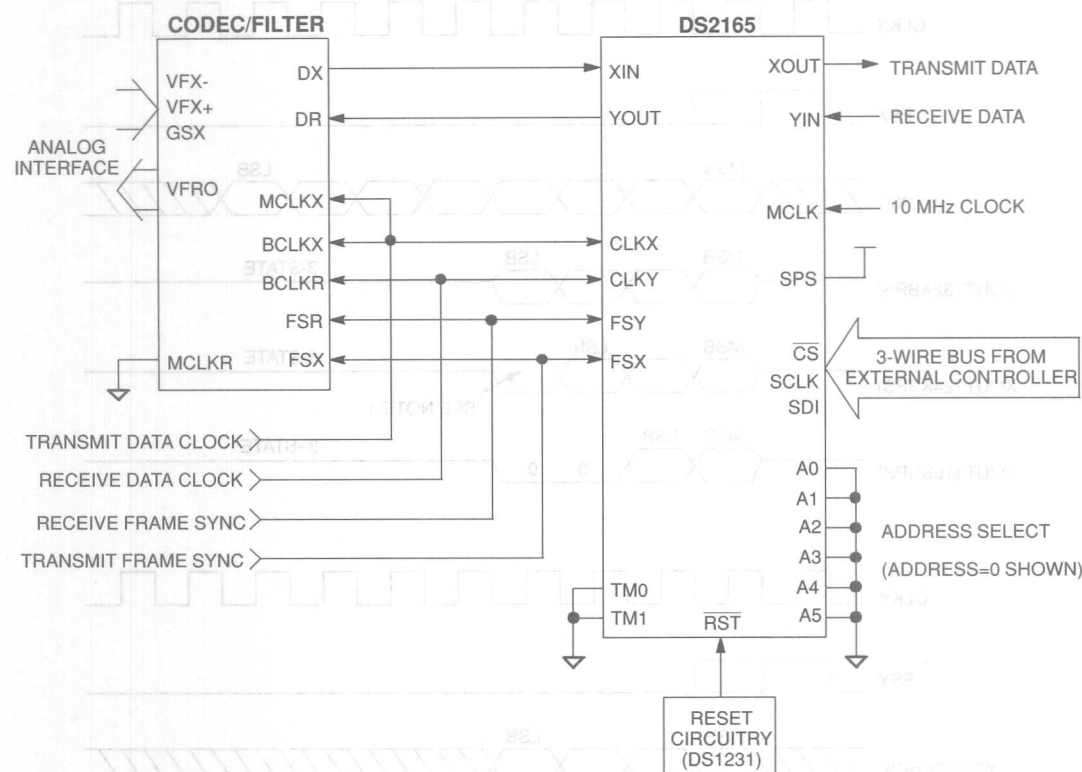
NOTES:

1. SCLK must be tied to V_{SS} when the hardware mode is selected.
2. When both channels are idled, power consumption is significantly reduced.
3. The DS2165 will power-up within 800 ms after either channel is returned to active from an idle state.

ALGORITHM SELECT FOR HARDWARE MODE Table 4

ALGORITHM	CONFIGURATION OF A1 AND A4
64Kbps to/from 32Kbps	Tie both A1 and A4 to V_{SS} .
64Kbps to/from 24Kbps	Hold A1 and A4 low during a hardware reset; take both A1 and A4 high after the \bar{RST} pin has returned high (allow 3 μs after \bar{RST} returns high before taking A1 and A4 high).
64Kbps to/from 16Kbps	Tie both A1 and A4 to V_{DD} .

DS2165 CONNECTION TO CODEC/FILTER Figure 11

**NOTE:****Suggested Codec/Filters**

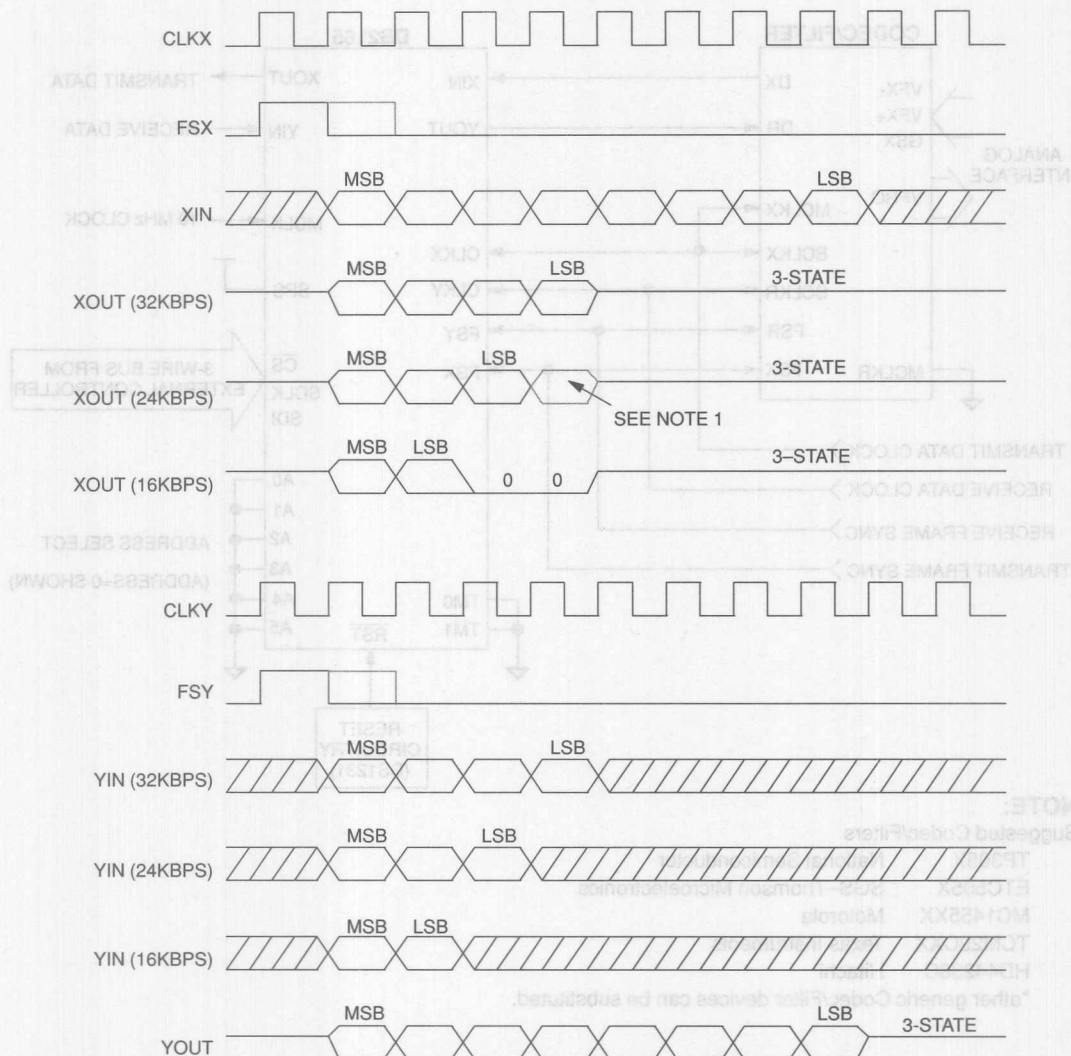
TP305X	National Semiconductor
ETC505X	SGS-Thomson Microelectronics
MC1455XX	Motorola
TCM29CXX	Texas Instruments
HD44238C	Hitachi

*other generic Codec/Filter devices can be substituted.

PCM AND ADPCM INPUT/OUTPUT

Since the organization of the input and output time slots on the DS2165 does not depend on the algorithm selected, it always assumes that PCM input and output will be in 8-bit bytes and that ADPCM input and output will be in 4-bit bytes. Figure 12 demonstrates how the DS2165 handles the I/O for the three different algo-

rithms. In the figure, it is assumed that channel X is in the compression mode ($CP/\overline{EX} = 1$) and channel Y is in the expansion mode ($CP/\overline{EX} = 0$). Also, it is assumed that both the input and output time slots for both channels are set to 0.

PCM AND ADPCM I/O EXAMPLE Figure 12**NOTE:**

1. The bit after the LSB in the 24Kbps ADPCM output will only be a 1 when the DS2165 is operated in the software mode and is programmed to perform 24Kbps compression; in all other configurations, it will be a 0.

TIME SLOT RESTRICTIONS

Under certain conditions, the DS2165 does contain some restrictions on the output time slots that are available. These restrictions are covered in detail in a separate application note. No restrictions occur if the DS2165 is operated in the hardware mode.

INPUT TO OUTPUT DELAY

With all three compressions algorithms, the total delay, from the time the PCM data sample is captured by the DS2165 to the time it is output, is always less than 375 μ s. The exact delay is determined by the input and output time slots selected for each channel.

CHANNEL ASSOCIATED SIGNALING

The DS2165 supports Channel Associated Signaling (CAS) via its ability to automatically change from the 32Kbps compression algorithm to the 24Kbps algorithm. If the DS2165 is configured to perform the 32Kbps algorithm, then in both the hardware and software

mode, it will sense the frame sync inputs (FSX and FSY) for a double wide frame sync pulse. Whenever the DS2165 receives a double wide pulse, it will automatically switch from the 32Kbps algorithm to the 24Kbps algorithm. Switching to the 24Kbps algorithm allows the user to insert signaling data into the LSB bit position of the ADPCM output because this bit does not contain any useful speech information.

ON-THE-FLY ALGORITHM SELECTION

In the software mode, the user can switch between the three available algorithms on-the-fly. That is, the DS2165 does not need to be reset or stopped to make the change from one algorithm to another. The DS2165 reads the Control Register before it starts to process each PCM or ADPCM sample. If the user wishes to switch algorithms, then the Control Register must be updated via the serial port before the first input sample to be processed with the new algorithm arrives at either XIN or YIN. The PCM and ADPCM outputs will tristate during register updates.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			8	pF	
Output Capacitance	C_{OUT}			10	pF	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		20		mA	1, 2, 3
Active Supply Current	I_{DDA}		12		mA	1, 2, 3
Idle Supply Current	I_{DDI}		1		mA	1, 2, 3
Input Leakage	I_{IL}	-1.0		0.1	μ A	
Output Leakage	I_{OL}	-1.0		0.1	μ A	4
Output Current (2.4V)	$I_{O2.4}$	-1.0			mA	5
Output Current (1.0V)	$I_{O1.0}$	-4.0			mA	5
Output Current (2.5V)	$I_{O2.5}$	-0.3			mA	6
Output Current (0.4V)	$I_{O0.4}$	-2.0			mA	6

NOTES:

1. $I_{DDA} = \text{CLKV} = 1.241 \text{ MHz}$; $\text{MCLK} = 10 \text{ MHz}$.
2. Input is open; inputs switching full supply levels.
3. All channels in idle mode.
4. XOUT and YOUT are 3-state.
5. Applies only to 8V device.
6. Applies only to 8V device (DS2165Q).

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

-1.0V to +7.0V

0°C to 70°C

-55°C to +125°C

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V _{IH}	2.0		V _{CC} +0.3	V	5
Logic 0	V _{IL}	-0.3		+0.8	V	5
Supply	V _{DD}	4.5		5.5	V	5
Logic 1	V _{IH}	2.2		V _{CC} +0.3	V	6
Logic 0	V _{IL}	-0.3		+0.4	V	6
Supply	V _{DD}	2.7		3.6	V	6

CAPACITANCE(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C _{IN}			5	pF	
Output Capacitance	C _{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 10%)
(V_{DD}=3.0V + 20% – 10% for DS2165QL)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I _{DDA}		20		mA	1, 2, 5
Active Supply Current	I _{DDA}		12		mA	1, 2, 6
Idle Supply Current	I _{DDPD}		1		mA	1, 2, 3
Input Leakage	I _I	-1.0		+1.0	μA	
Output Leakage	I _O	-1.0		+1.0	μA	4
Output Current (2.4V)	I _{OH}	-1.0			mA	5
Output Current (0.4V)	I _{OL}	+4.0			mA	5
Output Current (2.2V)	I _{OH}	-0.5			mA	6
Output Current (0.4V)	I _{OL}	+2.0			mA	6

NOTES:

1. CLKX = CLKY = 1.544 MHz; MCLK = 10 MHz.
2. Outputs open; inputs swinging full supply levels.
3. Both channels in idle mode.
4. XOUT and YOUT are 3-stated.
5. Applies only to 5V device.
6. Applies only to 3V device (DS2165QL).

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLKX, CLKY Period	t_{PXY}	244		3906	ns	1
CLKX, CLKY Pulse Width	t_{WXYL} t_{WXYH}	100			ns	
CLKX, CLKY Rise/Fall Times	t_{RXY} t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	2
Setup Time from FSX, FSY high to CLKX, CLKY low	t_{SF}	50			ns	2
Hold Time from CLKX, CLKY low to FSX, FSY low	t_{HF}	100			ns	2
Setup Time for XIN, YIN to CLKX, CLKY low	t_{SD}	50			ns	2
Hold Time for XIN, YIN to CLKX, CLKY low	t_{HD}	50			ns	2
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	3
Delay Time from CLKX, CLKY to XOUT, YOUT 3-stated	t_{DXYZ}	20		150	ns	2,3,4

NOTES:

1. Maximum width of FSX and FSY is one CLKX or CLKY period (except for signaling frames).
2. Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10 ns maximum rise and fall times.
3. Load = 150 pF + 2 LSTTL loads.
4. For LSB of PCM or ADPCM byte.

MASTER CLOCK/RESET**AC ELECTRICAL CHARACTERISTICS**

(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)
 ($V_{DD} = 3.0V + 20\% - 10\%$ for DS2165QL)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	1
MCLK Pulse Width	t_{WMH} t_{WML}	45	50	55	ns	
MCLK Rise/Fall Times	t_{RM} , t_{FM}			10	ns	
RST Pulse Width	t_{RST}	1			ms	

NOTE:

1. MCLK = 10 MHz \pm 500 ppm

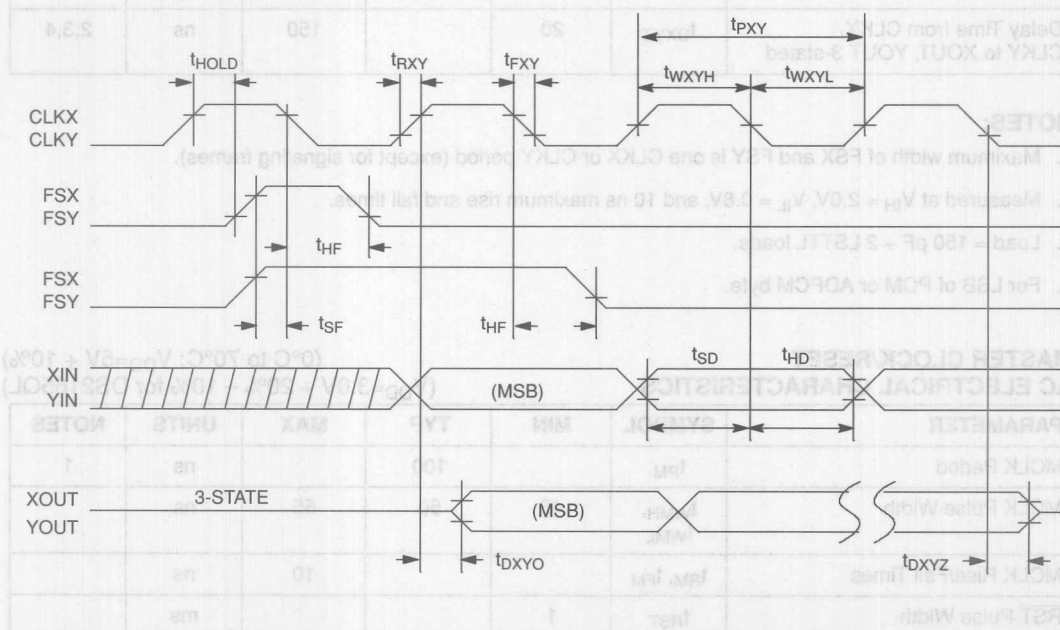
**SERIAL PORT
AC ELECTRICAL CHARACTERISTICS**

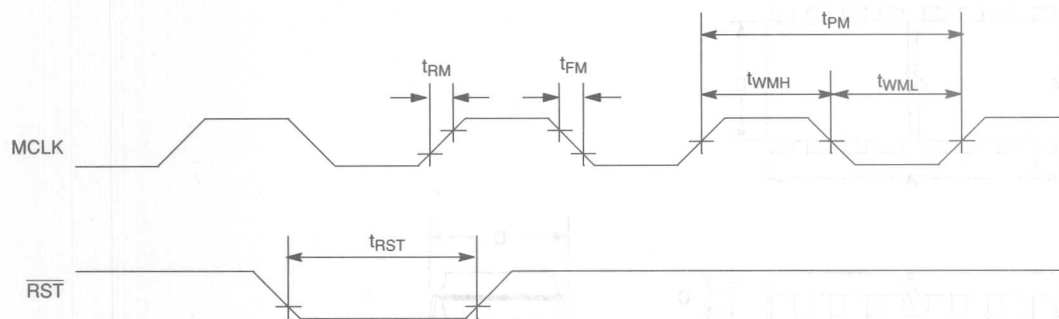
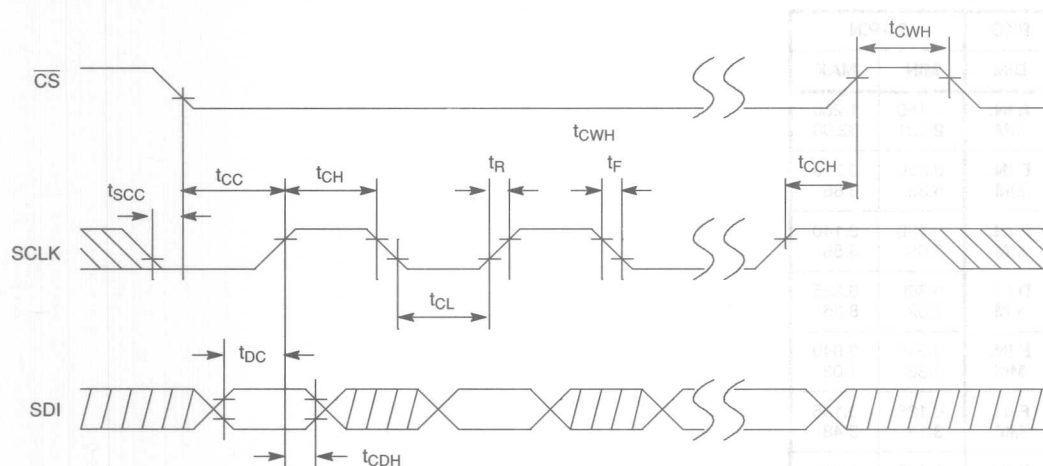
 (0°C to 70°C; $V_{DD}=5V \pm 10\%$)
 ($V_{DD}=3.0V \pm 20\% - 10\%$ for DS2165QL)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Time	t_R, t_F			100	ns	1
CS to SCLK Setup	t_{CC}	50			ns	1
SCLK to \overline{CS} Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to CS Falling	t_{SCC}	50			ns	1

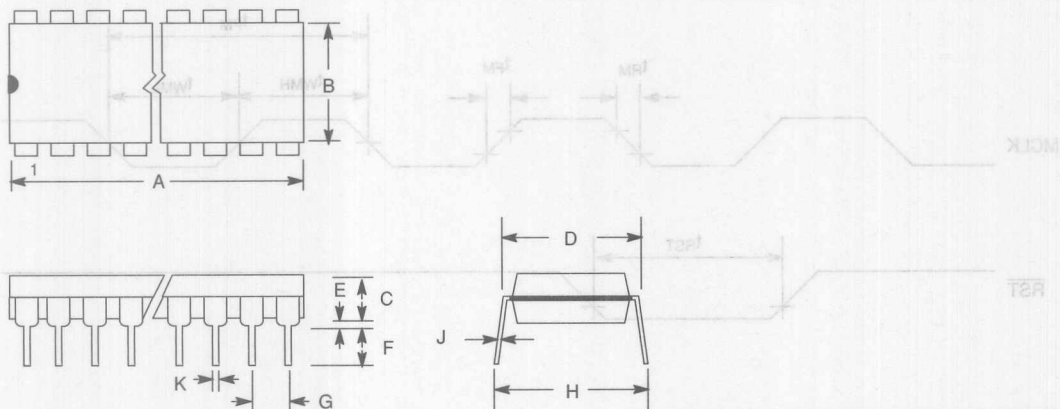
NOTE:

1. Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10ns maximum rise and fall times.

PCM INTERFACE AC TIMING DIAGRAM Figure 13


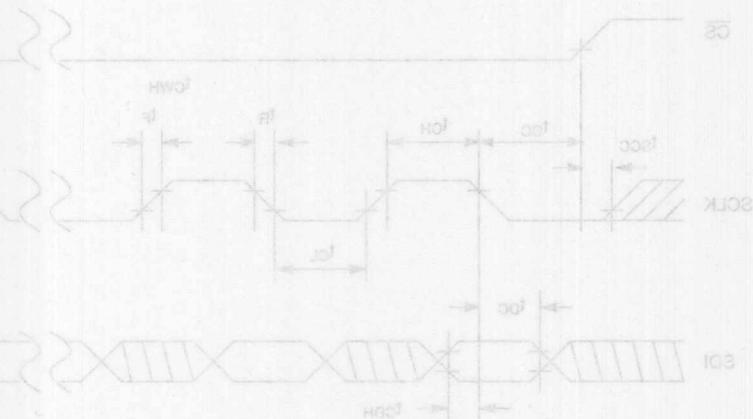
MASTER CLOCK/RESET AC TIMING DIAGRAM Figure 14**SERIAL PORT AC TIMING DIAGRAM** Figure 15**NOTE:**

1. SCLK may be either high or low when \overline{CS} is taken low.



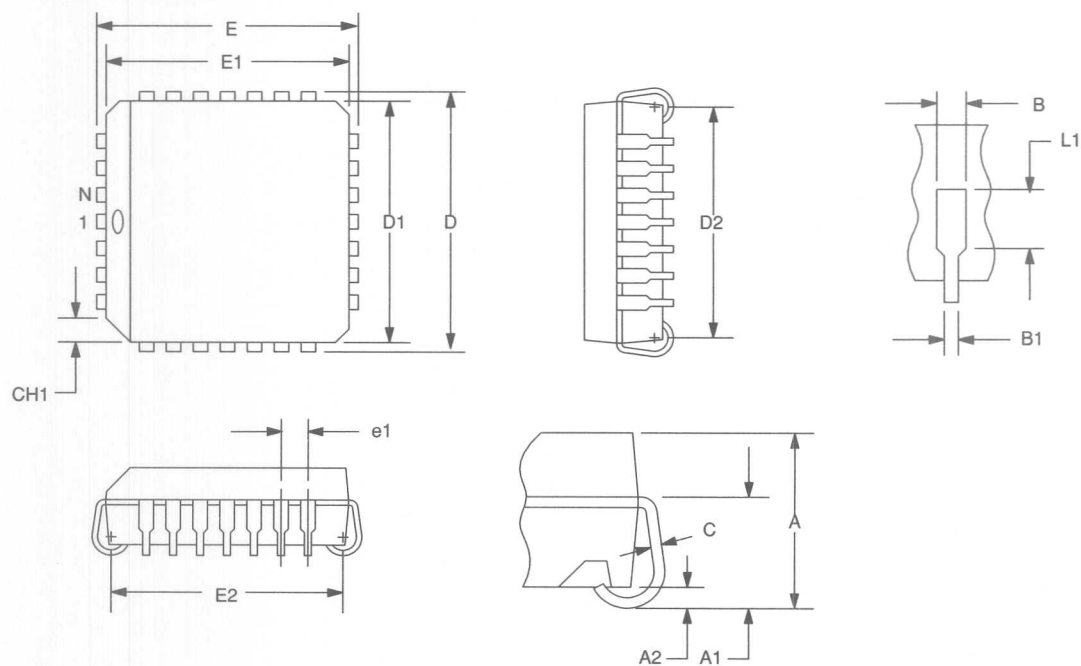
SERIAL PORT AC TIMING DIAGRAM Figure 15

PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.150 29.21	1.260 32.00
B IN. MM	0.250 6.35	0.270 6.86
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.125 3.18	0.135 3.48
G IN. MM	0.090 2.23	0.110 2.79
H IN. MM	0.320 8.13	0.370 9.40
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56



NOTE:
1. SCLK may be either high or low when CS is taken low.

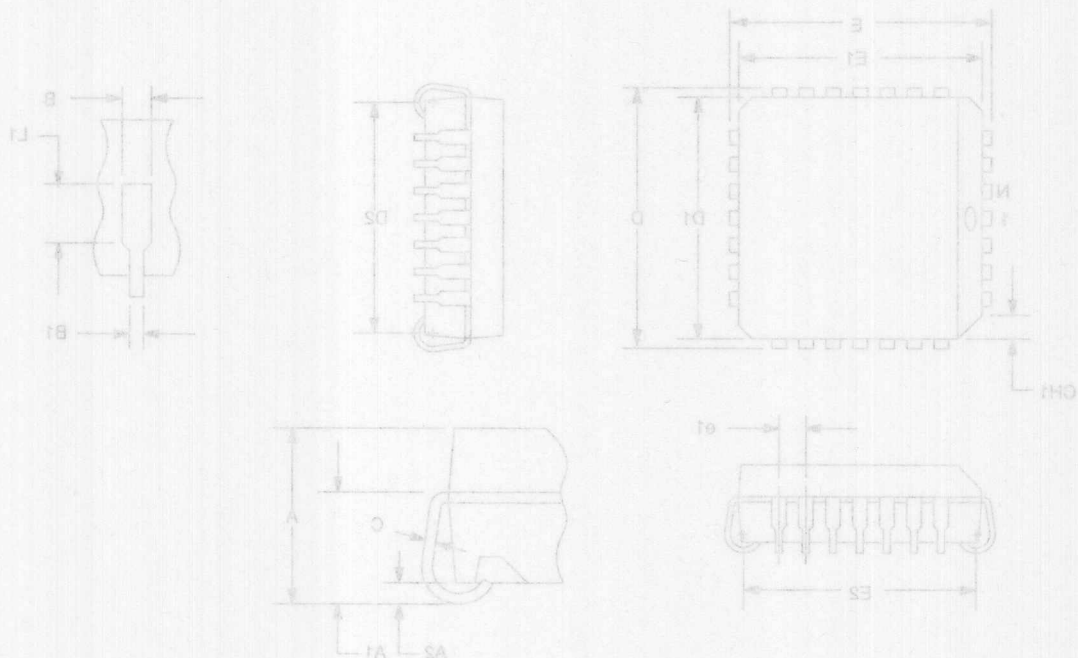
DS2165Q 16/24/32KBPS ADPCM PROCESSOR 28-PIN PLCC



This drawing controlled by drawing number 56-G4001-001.

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	—
N	28	—
e1	0.050 BSC	
CH1	0.042	0.048

025185G 162433KEPS ADPCM PROCESSOR 38-PIN PLCC



This drawing controlled by drawing number 38-G4001-001.

DIM	INCHES	
	MIN	MAX
A	0.182	0.180
A1	0.090	0.120
AS	0.050	—
B	0.058	0.033
B1	0.013	0.021
C	0.008	0.015
D	0.482	0.482
D1	0.450	0.458
D5	0.380	0.490
E	0.482	0.482
E1	0.450	0.458
E5	0.380	0.430
F1	0.090	—
N	38	—
e1	0.020 BSC	
GH1	0.042	0.048

DALLAS

SEMICONDUCTOR

DS2141A

T1 Controller

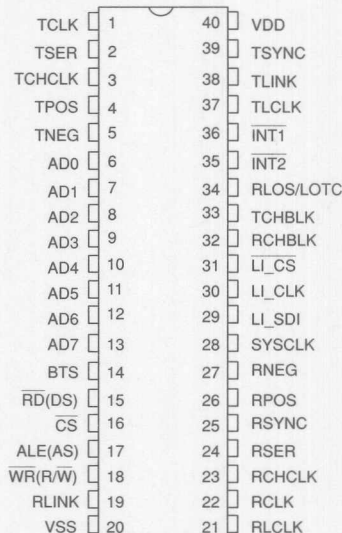
FEATURES

- DS1/ISDN-PRI framing transceiver
- Frames to D4, ESF, and SLC-96 formats
- Parallel control port
- Onboard, dual two-frame elastic store slip buffers
- Extracts and inserts robbed-bit signaling
- Programmable output clocks
- Onboard FDL support circuitry
- 5V supply; low-power CMOS
- Available in 40-pin DIP and 44-pin PLCC (DS2141Q)
- Compatible with DS2186 Transmit Line Interface, DS2187 Receive Line Interface, DS2188 Jitter Attenuator, DS2290 T1 Isolation Stik, and DS2291 T1 Long Loop Stik.

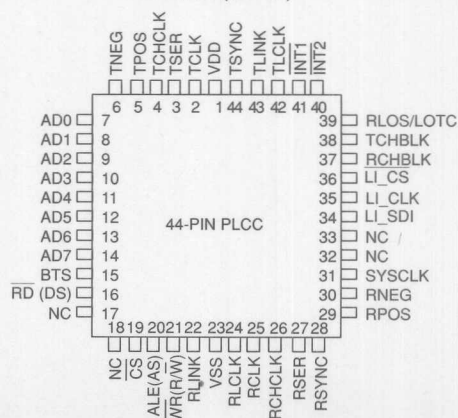
DESCRIPTION

The DS2141A is a comprehensive, software-driven T1 framer. It is meant to act as a slave or coprocessor to a microcontroller or microprocessor. Quick access via the parallel control port allows a single micro to handle many T1 lines. The DS2141A is very flexible and can be configured into numerous orientations via software. The software orientation of the device allows the user to modify their design to conform to future T1 specification changes. The controller contains a set of 62 8-bit internal registers which the user can access. These internal registers are used to configure the device and obtain information from the T1 link. The device fully meets all of the latest T1 specifications including ANSI T1.403-1989, AT&T TR 62411 (12-90), and CCITT G.704 and G.706.

PIN ASSIGNMENT



40-Pin DIP (600 MIL)



44-PIN PLCC

1.0 INTRODUCTION

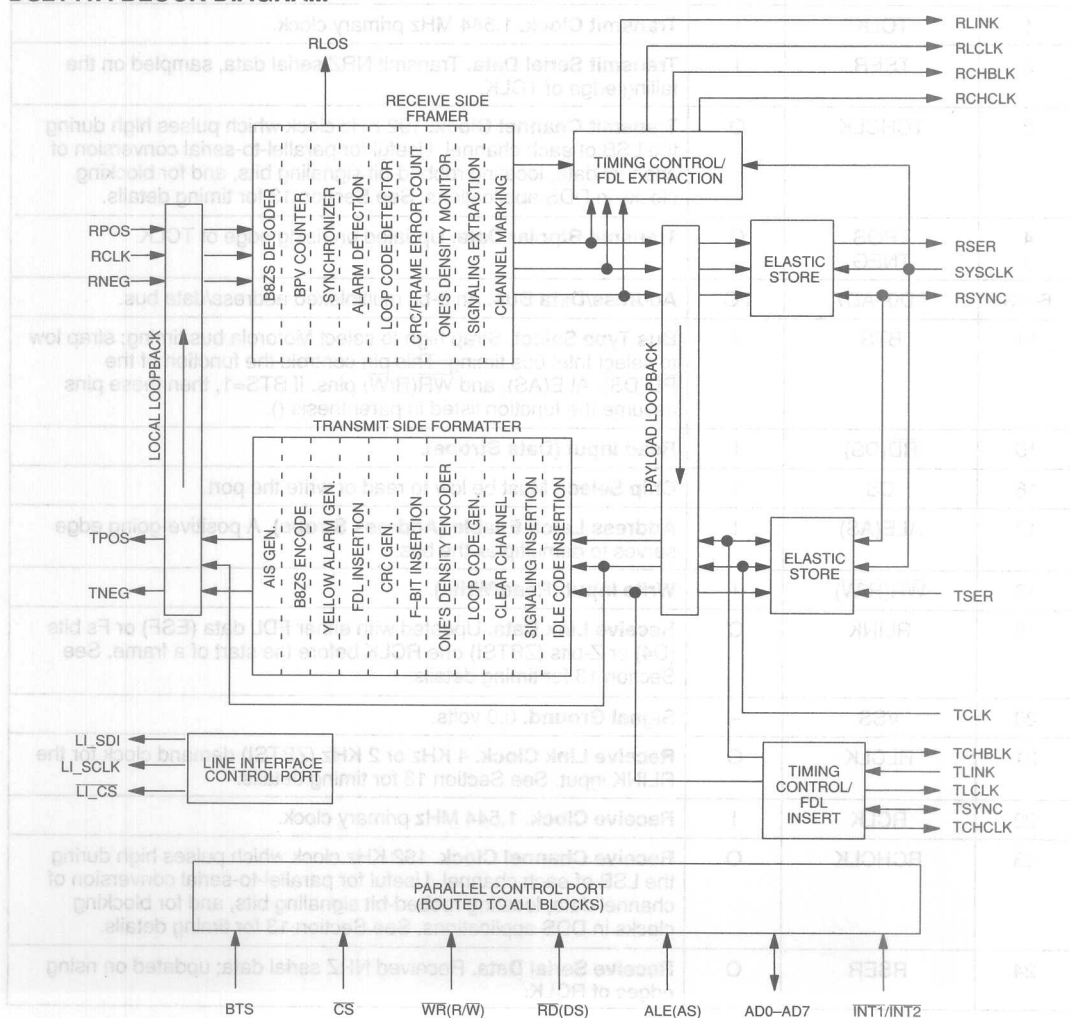
The DS2141A T1 Controller has four main sections: the receive side, the transmit side, the line interface controller, and the parallel control port. See the block diagram below. On the receive side, the device will clock in the serial T1 stream via the RPOS and RNEG pins. The synchronizer will locate the frame and multiframe patterns and establish their respective positions. This information will be used by the rest of the receive side circuitry.

The DS2141A is an "off-line" framer, which means that all of the T1 serial stream that goes into the device will

come out of it unchanged. Once the T1 data has been framed to, the robbed-bit signaling data and FDL can be extracted. The 2-frame elastic stores can either be enabled or bypassed.

The transmit side clocks in the unframed T1 stream at TSER and adds in the framing pattern, the robbed-bit signaling, and the FDL. The line interface control port will update line interface devices that contain a serial port. The parallel control port contains a multiplexed address and data structure which can be connected to either a microcontroller or microprocessor.

DS2141A BLOCK DIAGRAM



DS2141A FEATURES

- parallel control port
- large error counters
- onboard dual 2-frame elastic store
- FDL support circuitry
- robbed-bit signaling extraction and insertion
- programmable output clocks
- fully independent transmit and receive sections
- frame sync generation
- error-tolerant yellow and blue alarm detection
- output pin test mode
- payload loopback capability
- SLC-96 support
- remote loop up/down code detection
- loss of transmit clock detection
- loss of receive clock detection
- 1's density violation detection

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TCLK	I	Transmit Clock. 1.544 MHz primary clock.
2	TSER	I	Transmit Serial Data. Transmit NRZ serial data, sampled on the falling edge of TCLK.
3	TCHCLK	O	Transmit Channel Clock. 192 KHz clock which pulses high during the LSB of each channel. Useful for parallel-to-serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 13 for timing details.
4 5	TPOS TNEG	O	Transmit Bipolar Data. Updated on rising edge of TCLK.
6–13	AD0–AD7	I/O	Address/Data Bus. An 8-bit multiplexed address/data bus.
14	BTS	I	Bus Type Select. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD(DS), ALE(AS), and WR(R/W) pins. If BTS=1, then these pins assume the function listed in parenthesis ().
15	RD(DS)	I	Read Input (Data Strobe).
16	CS	I	Chip Select. Must be low to read or write the port.
17	ALE(AS)	I	Address Latch Enable (Address Strobe). A positive-going edge serves to demultiplex the bus.
18	WR(R/W)	I	Write Input (Read/Write).
19	RLINK	O	Receive Link Data. Updated with either FDL data (ESF) or Fs bits (D4) or Z-bits (ZBTSI) one RCLK before the start of a frame. See Section 13 for timing details.
20	VSS	—	Signal Ground. 0.0 volts.
21	RLCLK	O	Receive Link Clock. 4 KHz or 2 KHz (ZBTSI) demand clock for the RLINK input. See Section 13 for timing details.
22	RCLK	I	Receive Clock. 1.544 MHz primary clock.
23	RCHCLK	O	Receive Channel Clock. 192 KHz clock which pulses high during the LSB of each channel. Useful for parallel-to-serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 13 for timing details.
24	RSER	O	Receive Serial Data. Received NRZ serial data; updated on rising edges of RCLK.

PIN	SYMBOL	TYPE	DESCRIPTION
25	RSYNC	I/O	Receive Sync. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4=0) or multiframe boundaries (RCR2.4=1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the elastic store is enabled via the CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame boundary pulse is applied. See Section 13 for timing details.
26 27	RPOS RNEG	I	Receive Bipolar Data Inputs. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
28	SYSCLK	I	System Clock. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled via the CCR. Should be tied low in applications that do not use the elastic store.
29	LI_SDI	O	Serial Port Data for the Line Interface. Connects directly to the SDI input pin on the line interface.
30	LI_CLK	O	Serial Port Clock for the Line Interface. Connects directly to the SCLK input pin on the line interface.
31	LI_CS	O	Serial Port Chip Select for the Line Interface. Connects directly to the CS input pin on the line interface.
32 33	RCHBLK TCHBLK	O	Receive/Transmit Channel Block. A user-programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in application where not all T1 channels are used such as Fractional T1, 384 Kbps service, 768 Kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 13 for timing details.
34	RLOS/LOTC	O	Receive Loss of Sync/Loss of Transmit Clock. A dual function output. If CCR1.6=0, then this pin will toggle high when the synchronizer is searching for the T1 frame and multiframe. If CCR1.6=1, then this pin will toggle high when the TCLK pin has not been toggled for 5 μ s.
35	INT2	O	Receive Alarm Interrupt 2. Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
36	INT1	O	Receive Alarm Interrupt 1. Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
37	TLCLK	O	Transmit Link Clock. 4 KHz or 2 KHz (ZBTSI) demand clock for the TLINK input. See Section 13 for timing details.
38	TLINK	I	Transmit Link Data. If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 13 for timing details.
39	TSYNC	I/O	Transmit Sync. A pulse at this pin will establish either frame or multiframe boundaries for the DS2141A. Via TCR2.2, the DS2141A can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 13 for timing details.
40	VDD	—	Positive Supply. 5.0 volts.

DS2141A REGISTER MAP

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
20	R/W	Status Register 1.	3F	R/W	Transmit Idle Definition Register.
21	R/W	Status Register 2.	60	R	Receive Signaling Register 1.
22	R/W	Receive Information Register.	61	R	Receive Signaling Register 2.
23	R	Bipolar Violation/ESF Error Event Count Register 1.	62	R	Receive Signaling Register 3.
24	R	Bipolar Violation/ESF Error Event Count Register 2.	63	R	Receive Signaling Register 4.
25	R	CRC6 Count Register 1.	64	R	Receive Signaling Register 5.
26	R	CRC6 Count Register 2.	65	R	Receive Signaling Register 6.
27	R	Frame Error Count Register.	66	R	Receive Signaling Register 7.
28	R	Receive FDL Register.	67	R	Receive Signaling Register 8.
29	R/W	Receive FDL Match Register 1.	68	R	Receive Signaling Register 9.
2A	R/W	Receive FDL Match Register 2.	69	R	Receive Signaling Register 10.
2B	R/W	Receive Control Register 1.	6A	R	Receive Signaling Register 11.
2C	R/W	Receive Control Register 2.	6B	R	Receive Signaling Register 12.
2D	R/W	Receive Mark Register 1.	6C	R/W	Receive Channel Blocking Register 1.
2E	R/W	Receive Mark Register 2.	6D	R/W	Receive Channel Blocking Register 2.
2F	R/W	Receive Mark Register 3.	6E	R/W	Receive Channel Blocking Register 3.
30		Not Assigned.	6F	R/W	Interrupt Mask Register 2.
31		Not Assigned.	70	R/W	Transmit Signaling Register 1.
32	R/W	Transmit Channel Blocking Register 1.	71	R/W	Transmit Signaling Register 2.
33	R/W	Transmit Channel Blocking Register 2.	72	R/W	Transmit Signaling Register 3.
34	R/W	Transmit Channel Blocking Register 3.	73	R/W	Transmit Signaling Register 4.
35	R/W	Transmit Control Register 1.	74	R/W	Transmit Signaling Register 5.
36	R/W	Transmit Control Register 2.	75	R/W	Transmit Signaling Register 6.
37	R/W	Common Control Register 1.	76	R/W	Transmit Signaling Register 7.
38	R/W	Common Control Register 2.	77	R/W	Transmit Signaling Register 8.
39	R/W	Transmit Transparency Register 1.	78	R/W	Transmit Signaling Register 9.
3A	R/W	Transmit Transparency Register 2.	79	R/W	Transmit Signaling Register 10.
3B	R/W	Transmit Transparency Register 3.	7A	R/W	Transmit Signaling Register 11.
3C	R/W	Transmit Idle Register 1.	7B	R/W	Transmit Signaling Register 12.
3D	R/W	Transmit Idle Register 2.	7C	R/W	LI Control Register Byte 1.
3E	R/W	Transmit Idle Register 3.	7D	R/W	LI Control Register Byte 2.
			7E	R/W	Transmit FDL Register.
			7F	R/W	Interrupt Mask Register 1.

Note: All values indicated within the Address column are hexadecimal.

2.0 PARALLEL PORT

The DS2141A is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2141A can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the AC Electrical Characteristics for more details. The multiplexed bus on the DS2141A saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the DS2141A latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or WR

pulses. In a read cycle, the DS2141A outputs a byte of data during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as \overline{RD} transitions high in Intel timing or as DS transitions low in Motorola timing.

3.0 CONTROL REGISTERS

The operation of the DS2141A is configured via a set of six registers. Typically, the control registers are only accessed when the system is first powered up. Once, the DS2141A has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and two Common Control Registers (CCR1 and CCR2). Each of the six registers is described below.

RCR1: RECEIVE CONTROL REGISTER 1 (2Bh)

(MSB)								(LSB)
—	ARC	OOF1	OOF2	SYNCC	SYNCT	SYNCE	RESYNC	
SYMBOL	POSITION	NAME AND DESCRIPTION						
—	RCR1.7	Not Assigned. Should be set to 0 when written to.						
ARC	RCR1.6	Auto Resync Criteria. 0 = Resync on OOF or RCL event. 1 = Resync on OOF only.						
OOF1	RCR1.5	Out Of Frame Select 1. 0 = 2/4 frame bits in error. 1 = 2/5 frame bits in error.						
OOF2	RCR1.4	Out Of Frame Select 2. 0 = follow RCR1.5. 1 = 2/6 frame bits in error.						
SYNCC	RCR1.3	Sync Criteria. In D4 Framing Mode. 0 = search for Ft pattern, then search for Fs pattern. 1 = cross couple Ft and Fs pattern. In ESF Framing Mode. 0 = search for FPS pattern only. 1 = search for FPS and verify with CRC6.						
SYNCT	RCR1.2	Sync Time. 0 = qualify 10 bits. 1 = qualify 24 bits.						
SYNCE	RCR1.1	Sync Enable. 0 = auto resync enabled. 1 = auto resync disabled.						
RESYNC	RCR1.0	Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.						

RCR2: RECEIVE CONTROL REGISTER 2 (2Ch)

(MSB)								(LSB)	
RCS	RZBTSI	RSDW	RSM	RSIO	RD4YM	FSBE	BPVCRS		
SYMBOL	POSITION	NAME AND DESCRIPTION							
RCS	RCR2.7	Receive Code Select. 0 = idle code (7F Hex). 1 = digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex).							
RZBTSI	RCR2.6	Receive Side ZBTSI Enable. 0 = ZBTSI disabled. 1 = ZBTSI enabled.							
RSDW	RCR2.5	RSYNC Double-Wide. 0 = do not pulse double-wide in signaling frames. 1 = do pulse double-wide in signaling frames. (note: this bit must be set to 0 when RCR2.4 = 1 or when RCR2.3 = 1)							
RSM	RCR2.4	RSYNC Mode Select. 0 = frame mode (see the timing in Section 13). 1 = multiframe mode (see the timing in Section 13).							
RSIO	RCR2.3	RSYNC I/O Select. 0 = RSYNC is an output. 1 = RSYNC is an input (only valid if elastic store enabled). (note: this bit must be set to 0 when CCR1.2 = 0).							
RD4YM	RCR2.2	Receive Side D4 Yellow Alarm Select. 0 = 0 in bit 2 of all channels. 1 = a 1 in the S-bit position of frame 12.							
FSBE	RCR2.1	Fs Bit Error Report Enable. 0 = do not report bit errors in the Fs bit position in FECR. 1 = report bit errors in the Fs bit position in FECR.							
BPVCRS	RCR2.0	BPVCRS Function Select. 0 = counts bipolar violations. 1 = counts ESF error events (CRC6 or'ed with RLOS).							

TCR1: TRANSMIT CONTROL REGISTER 1 (35h)

(MSB)

(LSB)

ODF	TFPT	TCPT	RBSE	GB7S	TLINK	TBL	TYEL
-----	------	------	------	------	-------	-----	------

SYMBOL	POSITION	NAME AND DESCRIPTION
--------	----------	----------------------

ODF	TCR1.7	Output Data Format. 0 = bipolar data at TPOS and TNEG. 1 = NRZ data at TPOS; TNEG = 0.
TFPT	TCR1.6	Transmit Framing Pass Through. 0 = Ft or FPS bits sourced internally. 1 = Ft or FPS bits sampled at TSER during F-bit time.
TCPT	TCR1.5	Transmit CRC Pass Through. 0 = source CRC6 bits internally. 1 = CRC6 bits sampled at TSER during F-bit time.
RBSE	TCR1.4	Robbed Bit Signaling Enable. 0 = no signaling is inserted in any channel. 1 = signaling is inserted in all channels (the TTR registers can be used to block insertion on a channel by channel basis).
GB7S	TCR1.3	Global Bit 7 Stuffing. 0 = allow the TTR registers to determine which channels containing all zeros are to be bit 7 stuffed. 1 = force bit 7 stuffing in all zero byte channels regardless of how the TTR registers are programmed.
TLINK	TCR1.2	TLINK Select. 0 = source FDL or Fs bits from TFDL register. 1 = source FDL or Fs bits from the TLINK pin.
TBL	TCR1.1	Transmit Blue Alarm. 0 = transmit data normally. 1 = transmit an unframed all 1's code at TPOS and TNEG.
TYEL	TCR1.0	Transmit Yellow Alarm. 0 = do not transmit yellow alarm. 1 = transmit yellow alarm.

TCR2: TRANSMIT CONTROL REGISTER 2 (36h)

(MSB)

(LSB)

TESTM	TESTIO	TZBTSI	TSDW	TSM	TSIO	TD4YM	B7ZS
-------	--------	--------	------	-----	------	-------	------

SYMBOL	POSITION	NAME AND DESCRIPTION
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TESTM	TCR2.7	Test Mode Select. Set this bit to a 1 to force all outputs (including I/O pins) either high (TCR2.6 = 1) or low (TCR2.6 = 0).
TESTIO	TCR2.6	Test I/O Pins. 0 = force all output (and I/O) pins to a logic 0. 1 = force all output (and I/O) pins to a logic 1.
TZBTSI	TCR2.5	Transmit Side ZBTSI Enable. 0 = ZBTSI disabled. 1 = ZBTSI enabled.

TSDW	TCR2.4	TSYNC Double-Wide. 0 = do not pulse double-wide in signaling frames. 1 = do pulse double-wide in signaling frames. (note: this bit must be set to 0 when TCR2.3 = 1 or when TCR2.2 = 0).
TSM	TCR2.3	TSYNC Mode Select. 0 = frame mode (see the timing in Section 13). 1 = multiframe mode (see the timing in Section 13).
TSIO	TCR2.2	TSYNC I/O Select. 0 = TSYNC is an input. 1 = TSYNC is an output.
TD4YM	TCR2.1	Transmit Side D4 Yellow Alarm Select. 0 = 0s in bit 2 of all channels. 1 = a 1 in the S-bit position of frame 12.
B7ZS	TCR2.0	Bit 7 Zero Suppression Enable. 0 = no stuffing occurs. 1 = Bit 7 forced to a 1 in channels with all 0s.

CCR1: COMMON CONTROL REGISTER 1 (37h)

(MSB)							(LSB)
TESE	P34F	RSOA	—	SCLKM	RESE	PLB	LLB
SYMBOL	POSITION	NAME AND DESCRIPTION					
TESE	CCR1.7	Transmit Elastic Store Enable. 0 = elastic store is bypassed. 1 = elastic store is enabled.					
P34F	CCR1.6	Function of Pin 34. 0 = Receive Loss of Sync (RLOS). 1 = Loss of Transmit Clock (LOTC).					
RSOA	CCR1.5	Receive Signaling All 1's. 0 = allow robbed signaling bits to appear at RSER. 1 = force all robbed signaling bits at RSER to 1.					
—	CCR1.4	Not Assigned. Should be set to 0 when written to.					
SCLKM	CCR1.3	SYSCLK Mode Select. 0 = if SYSCLK is 1.544 MHz. 1 = if SYSCLK is 2.048 MHz.					
RESE	CCR1.2	Receive Elastic Store Enable. 0 = elastic store is bypassed. 1 = elastic store is enabled.					
PLB	CCR1.1	Payload Loopback. 0 = loopback disabled. 1 = loopback enabled.					
LLB	CCR1.0	Local Loopback. 0 = loopback disabled. 1 = loopback enabled.					

PAYLOAD LOOPBACK

When CCR1.1 is set to a 1, the DS2141A will be forced into Payload LoopBack (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS2141A will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS2141A. When PLB is enabled, the following will occur:

1. Data will be transmitted from the TPOS and TNEG pins synchronous with RCLK instead of TCLK.
2. All of the receive side signals will continue to operate normally.
3. The TCHCLK and TCHBLK signals are forced low.
4. Data at the TSER pin is ignored.

5. The TLCLK signal will become synchronous with RCLK instead of TCLK.

LOCAL LOOPBACK

When CCR1.0 is set to a 1, the DS2141A will enter a Local LoopBack (LLB) mode. This loopback is useful in testing and debugging applications. In LLB, the DS2141A will loop data from the transmit side back to the receive side. This loopback is synonymous with replacing the RCLK input with the TCLK signal, and the RPOS/RNEG inputs with the TPOS/TNEG outputs. When LLB is enabled, the following will occur:

1. The TPOS and TNEG pins will transmit an unframed all 1's
2. Data at RPOS and RNEG will be ignored
3. All receive side signals will take on timing synchronous with TCLK instead of RCLK.

CCR2: COMMON CONTROL REGISTER 2 (38h)

(MSB)				(LSB)			
TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL
SYMBOL	POSITION	NAME AND DESCRIPTION					
TFM	CCR2.7	Transmit Frame Mode Select. 0 = D4 framing mode. 1 = ESF framing mode.					
TB8ZS	CCR2.6	Transmit B8ZS Enable. 0 = B8ZS disabled. 1 = B8ZS enabled.					
TSLC96	CCR2.5	Transmit SLC-96/Fs Bit Insertion Enable. 0 = SLC-96 disabled. 1 = SLC-96 enabled.					
TFDL	CCR2.4	Transmit Zero Stuffer Enable. 0 = zero stuffer disabled. 1 = zero stuffer enabled.					
RFM	CCR2.3	Receive Frame Mode Select. 0 = D4 framing mode. 1 = ESF framing mode.					
RB8ZS	CCR2.2	Receive B8ZS Enable. 0 = B8ZS disabled. 1 = B8ZS enabled.					

CCR2.1 Receive SLC-96 Enable.

0 = SLC-96 disabled.

1 = SLC-96 enabled.

RFDL**CCR2.0****Receive Zero Destuffer Enable.**

0 = zero destuffer disabled.

1 = zero destuffer enabled.

4.0 STATUS AND INFORMATION REGISTERS

There is a set of three registers that contain information on the current real time status of the DS2141A: Status Register 1 (SR1), Status Register 2 (SR2), and the Receive Information Register (RIR). When a particular event has occurred (or is occurring), the appropriate bit in one of these three registers will be set to a 1. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again (or in the case of RLOS, if loss of sync is still present).

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS2141A which bits the user wishes to read and have cleared. The user will write a byte to one of these three registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated

with current value and it will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2141A with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the INT1 and INT2 pins respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

RIR: RECEIVE INFORMATION REGISTER (22h)

(MSB)								(LSB)
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE	
SYMBOL	POSITION	NAME AND DESCRIPTION						
COFA	RIR.7	Change of Frame Alignment. Set when the last resync resulted in a change of frame or multiframe alignment.						
8ZD	RIR.6	Eight Zero Detect. Set when a string of eight consecutive 0s has been received at RPOS and RNEG.						
16ZD	RIR.5	Sixteen Zero Detect. Set when a string of sixteen consecutive 0s has been received at RPOS and RNEG.						
RESF	RIR.4	Receive Elastic Store Full. Set when the elastic store buffer fills and a frame is deleted.						
RESE	RIR.3	Receive Elastic Store Empty. Set when the elastic store buffer empties and a frame is repeated.						

SEFE	RIR.2	Severely Errored Framing Event. Set when 2 out of 6 framing bits are received in error.
B8ZS	RIR.1	B8ZS Code Word Detect. Set when a B8ZS code word is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.2.
FBE	RIR.0	Frame Bit Error. Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

Note: If the transmit elastic store slips, both RIR.4 and RIR.3 will be set.

SR1: STATUS REGISTER 1 (20h)

(MSB)							(LSB)
LUP	LDN	LOT	SLIP	RBL	RYEL	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	SR1.7	Loop Up Code Detected. Set when the repeating ...00001... loop up code is being received.
LDN	SR1.6	Loop Down Code Detected. Set when the repeating ...001... loop down code is being received.
LOT	SR1.5	Loss of Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 5.2 μ s). Will force pin 34 high if enabled via CCR1.6. Based on RCLK.
SLIP	SR1.4	Elastic Store Slip Occurrence. Set when the elastic store has either repeated or deleted a frame of data.
RBL	SR1.3	Receive Blue Alarm. Set when an all 1's code is received at RPOS and RNEG.
RYEL	SR1.2	Receive Yellow Alarm. Set when a yellow alarm is received at RPOS and RNEG.
RCL	SR1.1	Receive Carrier Loss. Set when 192 consecutive 0s have been detected at RPOS and RNEG.
RLOS	SR1.0	Receive Loss of Sync. Set when the device is not synchronized to the receive T1 stream.

LOOP UP/DOWN CODE DETECTION

Bits SR1.7 and SR1.6 will indicate when either the standard "loop up" or "loop down" codes are being received by the DS2141A. When a loop up code has been received for 5 seconds, the CPE is expected to loop the recovered data (without correcting BPVs) back to the source. The loop down code indicates that the loopback should be discontinued. See the AT&T publication TR 62411 for more details. The DS2141A will detect the loop up/down codes in both framed and unframed cir-

cumstances with bit error rates as high as 10^{-2} . The loop code detector has a nominal integration period of 48 ms. Hence, after about 48 ms of receiving either code, the proper status bit will be set to a 1. After this initial indication, it is recommended that the software poll the DS2141A every 100 ms to 500 ms until five seconds has elapsed to insure that the code is continuously present. Once 5 seconds has passed, the line interface should be taken into or out of loopback.

SR2: STATUS REGISTER 2 (21h)**(MSB)****(LSB)**

RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	LORC
SYMBOL	POSITION	NAME AND DESCRIPTION					
RMF	SR2.7	Receive Multiframe. Set on receive multiframe boundaries.					
TMF	SR2.6	Transmit Multiframe. Set on transmit multiframe boundaries.					
SEC	SR2.5	One Second Timer. Set on increments of one second based on RCLK; will be set in increments of 999 ms, 999 ms, and 1002 ms every 3 seconds.					
RFDL	SR2.4	Receive FDL Buffer Full. Set when the receive FDL buffer (RFDL) fills to capacity (8 bits).					
TFDL	SR2.3	Transmit FDL Buffer Empty. Set when the transmit FDL buffer (TFDL) empties.					
RMTCH	SR2.2	Receive FDL Match Occurrence. Set when the RFDL matches either RFDLM1 or RFDLM2.					
RAF	SR2.1	Receive FDL Abort. Set when eight consecutive 1's are received in the FDL.					
LORC	SR2.0	Loss of Receive Clock. Set when the RCLK pin has not transitioned for at least 2 μ s (3 μ s \pm 1 μ s).					

IMR1: INTERRUPT MASK REGISTER 1 (7Fh)**(MSB)****(LSB)**

LUP	LDN	LOT	SLIP	RBL	RYEL	RCL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION					
LUP	IMR1.7	Loop Up Code Detected. 0 = interrupt masked. 1 = interrupt enabled.					
LDN	IMR1.6	Loop Down Code Detected. 0 = interrupt masked. 1 = interrupt enabled.					
LOT	IMR1.5	Loss of Transmit Clock. 0 = interrupt masked. 1 = interrupt enabled.					
SLIP	IMR1.4	Elastic Store Slip Occurrence. 0 = interrupt masked. 1 = interrupt enabled.					
RBL	IMR1.3	Receive Blue Alarm. 0 = interrupt masked. 1 = interrupt enabled.					
RYEL	IMR1.2	Receive Yellow Alarm. 0 = interrupt masked. 1 = interrupt enabled.					

RCL IMR1.1 **Receive Carrier Loss.**
0 = interrupt masked.
1 = interrupt enabled.

RLOS IMR1.0 **Receive Loss of Sync.**
0 = interrupt masked.
1 = interrupt enabled.

IMR2: INTERRUPT MASK REGISTER 2 (6Fh)

(MSB)				(LSB)			
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	LORC
SYMBOL	POSITION	NAME AND DESCRIPTION					
RMF	IMR2.7	Receive Multiframe. 0 = interrupt masked. 1 = interrupt enabled.					
TMF	IMR2.6	Transmit Multiframe. 0 = interrupt masked. 1 = interrupt enabled.					
SEC	IMR2.5	One Second Timer. 0 = interrupt masked. 1 = interrupt enabled.					
RFDL	IMR2.4	Receive FDL Buffer Full. 0 = interrupt masked. 1 = interrupt enabled.					
TFDL	IMR2.3	Transmit FDL Buffer Empty. 0 = interrupt masked. 1 = interrupt enabled.					
RMTCH	IMR2.2	Receive FDL Match Occurrence. 0 = interrupt masked. 1 = interrupt enabled.					
RAF	IMR2.1	Receive FDL Abort. 0 = interrupt masked. 1 = interrupt enabled.					
LORC	IMR2.0	Loss of Receive Clock. 0 = interrupt masked. 1 = interrupt enabled.					

5.0 ERROR COUNT REGISTERS

There is a set of three counters in the DS2141A that record bipolar violations, errors in the CRC6 code words, and frame bit errors. Each of these three counters is automatically updated on one-second boundaries as determined by the one-second timer in Status Register 2

(SR2.5). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the one-second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost.

BPVCR1: BIPOLAR VIOLATION COUNT REGISTER 1 (23h)
BPVCR2: BIPOLAR VIOLATION COUNT REGISTER 2 (24h)

(MSB)				(LSB)				
BV15	BV14	BV13	BV12	BV11	BV10	BV9	BV8	BPVCR1
BV7	BV6	BV5	BV4	BV3	BV2	BV1	BV0	BPVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
BV15	BPVCR1.7	MSB of the bipolar violation count.
BV0	BPVCR2.0	LSB of the bipolar violation count.

Bipolar Violation Count Register 1 (BPVCR1) is the most significant word and BPVCR2 is the least significant word of a 16-bit counter that records bipolar violations (BPVs). If the B8ZS mode is set for the receive side via CCR2.2, then B8ZS code words are not counted. This counter increments at all times and is not

disabled by loss of sync conditions. The counter saturates at 65,535 and will not roll over. If the DS2141A is programmed to record ESF error events (RCR2.0=1), then the BPVCR will increment for each ESF multiframe that contains either an error in the CRC6 word or an out-of-frame occurrence (loss of sync).

CRCCR1: CRC6 COUNT REGISTER 1 (25h)
CRCCR2: CRC6 COUNT REGISTER 2 (26h)

(MSB)				(LSB)				
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR1
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC7	CRCCR1.7	MSB of the CRC6 count.
CRC0	CRCCR2.0	LSB of the CRC6 count.

CRC6 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 16-bit counter that records word errors in the Cyclic Redundancy Check 6 (CRC6) when the DS2141A is oper-

ated in the ESF framing mode (CCR2.3 = 1). This counter saturates at 65,535 and will not roll over. The counter is disabled during loss of sync conditions.

FECR: FRAME ERROR COUNT REGISTER (27h)

(MSB)				(LSB)			
FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
SYMBOL	POSITION	NAME AND DESCRIPTION					
FE7	FECR.7	MSB of the Frame Error count.					
FE0	FECR.0	LSB of the Frame Error count.					

The Frame Error Count Register (FECR) is a 8-bit counter that records either errors in the framing pattern. The FECR will count individual bit errors in the ESF framing pattern (...001011...) if the device is set into the ESF framing mode (CCR2.3 = 1) and it will count individual bit errors in the Ft framing pattern (...101010...) in the D4 framing mode (CCR2.3 = 0). If RCR2.1 = 1, then the FECR will also record individual bit errors in the Fs framing pattern (...001110...) when it is in the D4 framing mode. This counter saturates at 255 and will not roll over. The counter is disabled during loss of sync conditions.

6.0 FDL/FS EXTRACTION AND INSERTION

The DS2141A has the ability to extract/insert data from/into the Facility Data Link (FDL) in the ESF framing mode and from/into Fs bit position in the D4 framing mode. Since SLC-96 utilizes the Fs bit position, this capability can also be used in SLC-96 applications. The operation of the receive and transmit sections will be discussed separately.

6.1 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up

every 2 ms (8 x 250 μs). The DS2141A will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the INT2 pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2 ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR2.2 bit will be set to a 1 and the INT2 pin will toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The DS2141A also contains a zero destuffer which is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follow a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.0, the DS2141A will automatically look for five 1s in a row, followed by a 0. If it finds such a pattern, it will automatically remove the 0. If the 0 destuffer sees six or more 1s in a row followed by a 0, the 0 is not removed. The CCR2.0 bit should always be set to a 1 when the DS2141A is extracting the FDL. More on how to use the DS2141A in FDL applications is covered in a separate Application Note.

RFDL: RECEIVE FDL REGISTER (28h)

(MSB)				(LSB)			
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0
SYMBOL	POSITION	NAME AND DESCRIPTION					
RFDL7	RFDL.7	MSB of the Received FDL Code.					
RFDL0	RFDL.0	LSB of the Received FDL Code.					

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RFDLM1: RECEIVE FDL MATCH REGISTER 1 (29h)
RFDLM2: RECEIVE FDL MATCH REGISTER 2 (2Ah)

(MSB)				(LSB)			
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0
SYMBOL	POSITION	NAME AND DESCRIPTION					
RFDL7	RFDL.7	MSB of the FDL Match Code.					
RFDL0	RFDL.0	LSB of the FDL Match Code.					

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RFDLM1/RFDLM2), RSR2.2 will be set to a 1 and the INT2 will go active if enabled via IMR2.2.

6.2 TRANSMIT SECTION

The transmit section will shift out either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL) into the T1 data stream. When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full eight bits have been shifted out, the DS2141A will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to a 1. The INT2 will also toggle low if enabled via IMR2.3. The user has 2 ms (1.5 ms in SLC-96 ap-

plications) to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again.

The DS2141A also contains a zero stuffer which is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the DS2141A will automatically look for five 1s in a row. If it finds such a pattern, it will automatically insert a 0 after the five 1s. The CCR2.0 bit should always be set to a 1 when the DS2141A is inserting the FDL. More on how to use the DS2141A in FDL applications is covered in a separate Application Note.

TFDL: TRANSMIT FDL REGISTER (7Eh)

(MSB)				(LSB)			
TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0
SYMBOL		POSITION		NAME AND DESCRIPTION			
TFDL7		TFDL.7		MSB of the FDL code to be transmitted.			
TFDL0		TFDL.0		LSB of the FDL code to be transmitted.			

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first.

is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to 0, then the robbed signaling bits will appear at RSER in their proper position as they are received. If CCR1.5 is set to a 1, then the robbed signaling bit positions will be forced to a 1 at RSER.

7.0 SIGNALING OPERATION

The robbed bit signaling bits in embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2141A. There

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (60h to 6Bh)

(MSB)				(LSB)				
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)
C(8)	C(7)	C(6)	C(5)	C(4)	C(3)	C(2)	C(1)	RS7 (66)
C(16)	C(15)	C(14)	C(13)	C(12)	C(11)	C(10)	C(9)	RS8 (67)
C(24)	C(23)	C(22)	C(21)	C(20)	C(19)	C(18)	C(17)	RS9 (68)
D(8)	D(7)	D(6)	D(5)	D(4)	D(3)	D(2)	D(1)	RS10 (69)
D(16)	D(15)	D(14)	D(13)	D(12)	D(11)	D(10)	D(9)	RS11 (6A)
D(24)	D(23)	D(22)	D(21)	D(20)	D(19)	D(18)	D(17)	RS12 (6B)
SYMBOL		POSITION		NAME AND DESCRIPTION				
D(24)		RS12.7		Signaling Bit D in Channel 24.				
A(1)		RS1.0		Signaling Bit A in Channel 1.				

Each Receive Signaling Register (RS1 to RS12) reports the incoming robbed bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two framing bits per channel (A and B). In the D4 framing mode, the DS2141A will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the DS2141A is operated in either framing

mode, the user needs only to retrieve the signaling bits every 3 ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0 = 1). They will contain the most recent signaling information before the "OOF" occurred.

TS1 TO TS12: TRANSMIT SIGNALING REGISTERS (70h to 7Bh)

(MSB)				(LSB)				
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	TS1 (70)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	TS2 (71)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	TS3 (71)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	TS4 (73)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	TS5 (74)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	TS6 (75)
C(8)	C(7)	C(6)	C(5)	C(4)	C(3)	C(2)	C(1)	TS7 (76)
C(16)	C(15)	C(14)	C(13)	C(12)	C(11)	C(10)	C(9)	TS8 (77)
C(24)	C(23)	C(22)	C(21)	C(20)	C(19)	C(18)	C(17)	TS9 (78)
D(8)	D(7)	D(6)	D(5)	D(4)	D(3)	D(2)	D(1)	TS10 (79)
D(16)	D(15)	D(14)	D(13)	D(12)	D(11)	D(10)	D(9)	TS11 (7A)
D(24)	D(23)	D(22)	D(21)	D(20)	D(19)	D(18)	D(17)	TS12 (7B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	Signaling Bit D in Channel 24.
A(1)	TS1.0	Signaling Bit A in Channel 1.

Each Transmit Signaling Register (TS1 to TS12) contains the Robbed Bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two framing bits per channel (A and B). On multiframe boundaries, the DS2141A will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits.

8.0 SPECIAL TRANSMIT SIDE REGISTERS

There is a set of seven registers in the DS2141A that can be used to custom tailor the data that is to be transmitted onto the T1 line, on a channel by channel basis. Each of the 24 T1 channels can be either forced to be transparent or to have a user defined idle code inserted into them. Each of these special registers is defined below.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTERS (39h to 3Bh)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (39)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	Transmit Transparency Registers. 0 = this DS0 channel is not transparent. 1 = this DS0 channel is transparent.
CH1	TTR1.0	

Each of the bit positions in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel is transparent (or clear). If a DS0 is programmed to be clear, no robbed bit signaling

will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, bit 2 will be overwritten by a 0 when a Yellow Alarm is transmitted.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (3Ch to 3Eh)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	Transmit Idle Registers. 0 = do not insert the Idle Code into this DS0 channel. 1 = insert the Idle Code into this channel.
CH1	TIR1.0	

TIDR: TRANSMIT IDLE DEFINITION REGISTER (3Fh)

(MSB)				(LSB)			
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code.
TIDR0	TIDR.0	LSB of the Idle Code.

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel will transmit the Idle Code contained

in the Transmit Idle Definition Register (TIDR). Robbed bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3) control the RCHBLK and TCHCLK pins respectively. The RCHBLK and TCHCLK pins are user-programmable outputs that can be forced either high or low during indi-

vidual channels. These outputs can be used to block clocks to a USART or LAPD controller in Fractional T1, E1 to T1, or ISDN-PRI applications. When the appropriate bits are set to a 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 13 for an example.

RCBR1/RCBR2/RCBR3: RECEIVE CHANNEL BLOCKING REGISTERS (6Ch to 6Eh)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)

SYMBOL POSITION

CH24 RCBR3.7
CH1 RCBR1.0

NAME AND DESCRIPTION

Receive Channel Blocking Registers.

0 = force the RCHBLK pin to remain low during this channel time.

1 = force the RCHBLK pin high during this channel time.

TCBR1/TCBR2/TCBR3: TRANSMIT CHANNEL BLOCKING REGISTERS (32h to 34h)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (34)

SYMBOL POSITION

CH24 TCBR3.7
CH1 TCBR1.0

NAME AND DESCRIPTION

Transmit Channel Blocking Registers.

0 = force the TCHBLK pin to remain low during this channel time.

1 = force the TCHBLK pin high during this channel time.

10.0 ELASTIC STORES OPERATION

The DS2141A has two onboard two-frame (386 bits) elastic stores. These elastic stores have two main purposes. First, they can be used to rate convert the T1 data stream to 2.048Mbps (or a multiple of 2.048Mbps) which is the E1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e. not frequency locked) backplane clock. Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The receive side elastic store can be enabled via CCR1.2 and the transmit side elastic store is enabled via CCR1.7.

10.1 Receive Side

If the receive side elastic store is enabled (CCR1.2 = 1), then the user must provide either a 1.544MHz (CCR1.3

= 0) or 2.048MHz (CCR1.3 = 1) clock at the SYSCLK pin. The user has the option of either providing a frame sync at the RFSYNC pin (RCR2.3 = 1) or having the RFSYNC pin provide a pulse on frame boundaries (RCR2.3 = 0). If the user wishes to obtain pulses at the frame boundary, then RCR2.4 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR2.4 must be set to one. If the user selects to apply a 2.048MHz clock to the SYSCLK pin, then the data output at RSER will be forced to all ones every fourth channel and the F-bit will be deleted. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be forced to a one. Also, in 2.048MHz applications, the RCHBLK output will be forced high during the same channels as the RSER pin. See Section 13 for more details. This is useful in T1 to CEPT (E1) conversion applications. If the 386-bit

elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (193 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

10.2 Transmit Side

The transmit side elastic store can only be used if the receive side elastic store is enabled. The operation of the transmit elastic store is very similar to the receive side; both have controlled slip operation and both can operate with either a 1.544 MHz or a 2.048 MHz SYSCLK. When the transmit elastic store is enabled, both the SYSCLK and RSYNC signals are shared by both the elastic stores. Hence, they will have the same

backplane PCM frame and data structure. Controlled slips in the transmit elastic store are reported in by setting both RIR.3 and RIR.4.

11.0 RECEIVE MARK REGISTERS

The DS2141A has the ability to replace the incoming data, on a channel-by-channel basis, with either an idle code (7F Hex) or the digital milliwatt code, which is an 8-byte repeating pattern that represents a 1 KHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). The RCR2.7 bit will determine which code is used. Each bit in the RMRs represents a particular channel. If a bit is set to a 1, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to 0, no replacement occurs.

RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (2Dh to 2Fh)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1 (2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2 (2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3 (2F)

SYMBOL POSITION

CH24 RMR3.7
CH1 RMR1.0

NAME AND DESCRIPTION

Receive Mark Registers.

0 = do not affect the receive data associated with this channel.

1 = replace the receive data associated with this channel with either the idle code or the digital milliwatt code.

12.0 LINE INTERFACE CONTROL FUNCTION

The DS2141A can control line interface units that contain serial ports. When Control Register Bytes 1 or 2 (CRB1, CRB2) are written to, the DS2141A will automatically write this data serially (LSB first) into the line interface by creating a chip select, serial clock and serial

data via the $\overline{\text{LI_CS}}$, LI_SCLK and LI_SDI pins respectively. This control function is driven off of the RCLK; therefore RCLK must be present for proper operation. Registers CRB1 and CRB2 can only be written to, not read from. Writes to these registers must be at least 20 μsec apart. See Section 13 for timing information.

CRB1: CONTROL REGISTER BYTE 1 (7Ch)

CRB2: CONTROL REGISTER BYTE 2 (7Dh)

(MSB)				(LSB)				
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	CRB1 (7C)
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	CRB2 (7D)

SYMBOL POSITION

CR1 CRB1.0
CR7 CRB2.7

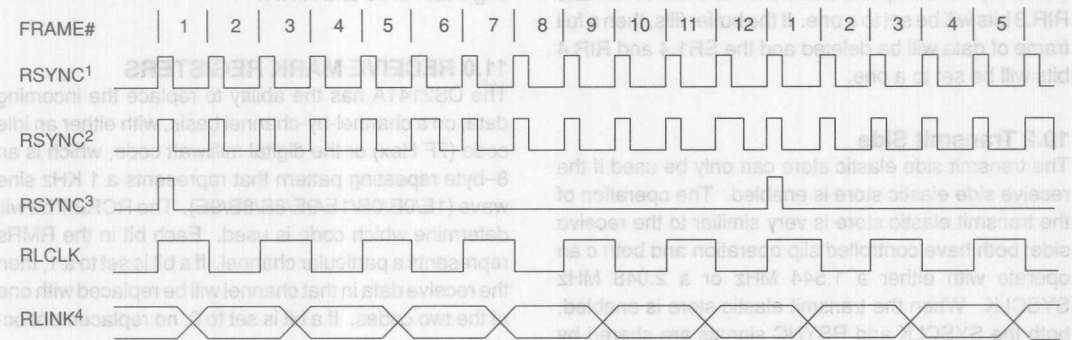
NAME AND DESCRIPTION

LSB of Control Register Byte 1.

MSB of Control Register Byte 2.

13.0 TIMING DIAGRAMS

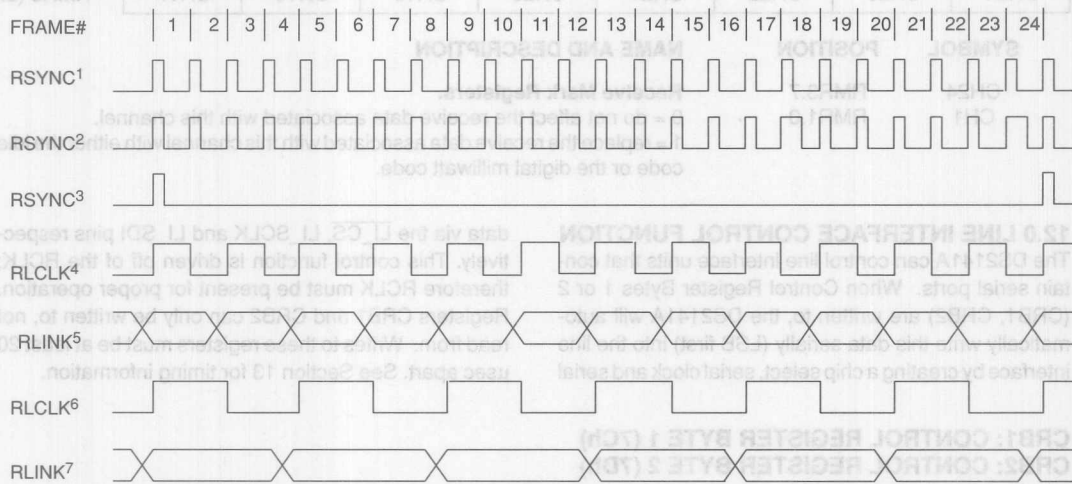
RECEIVE SIDE D4 TIMING



NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. RLINK data (S-bit) is updated one bit prior to even frames and held for two frames.

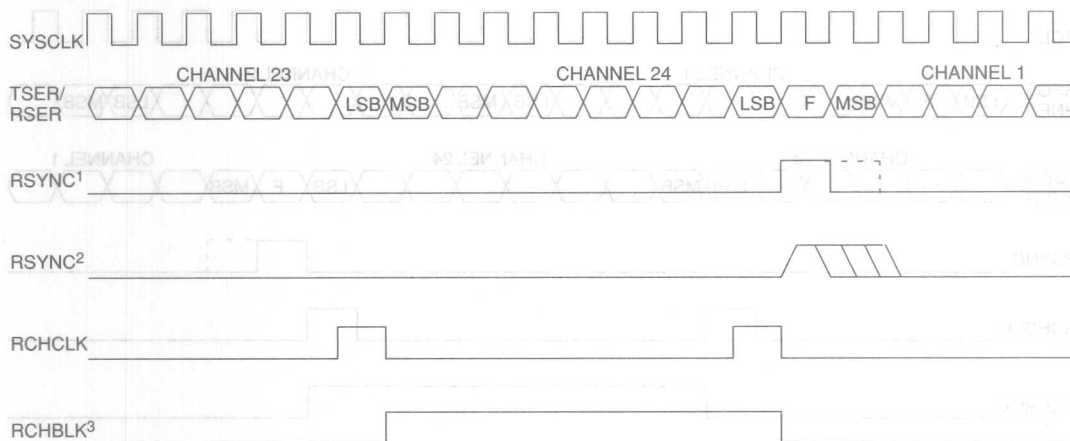
RECEIVE SIDE ESF TIMING



NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. ZBTSI mode disabled (RCR2.6=0).
5. RLINK data (FDL bits) is updated one bit time before odd frames and held for two frames.
6. ZBTSI mode is enabled (RCR2.6=1).
7. RLINK data (Z bits) is updated one bit time before odd frame and held for four frames.

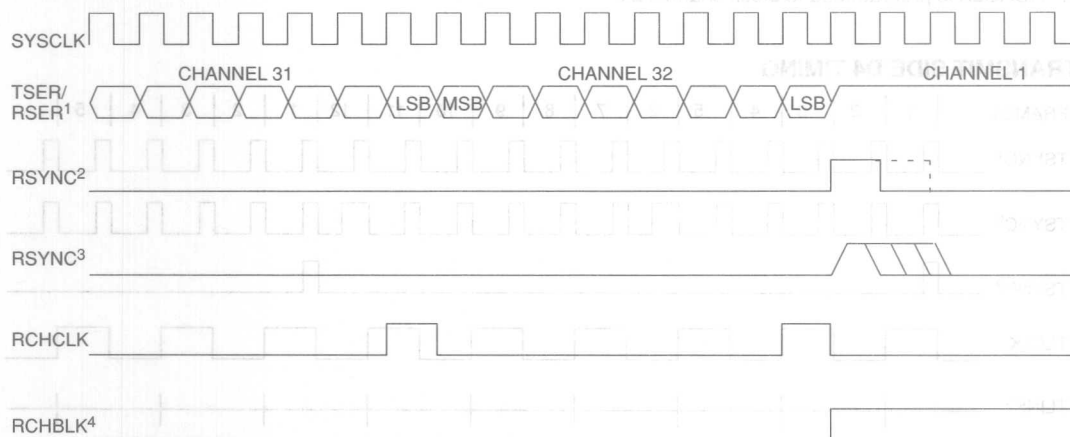
1.544 MHz BOUNDARY TIMING (WITH ELASTIC STORE(S) ENABLED)



NOTES:

1. RSYNC is in the output mode (RCR2.3=0).
2. RSYNC is in the input mode (RCR2.3=1).
3. RCHBLK is programmed to block channel 24.

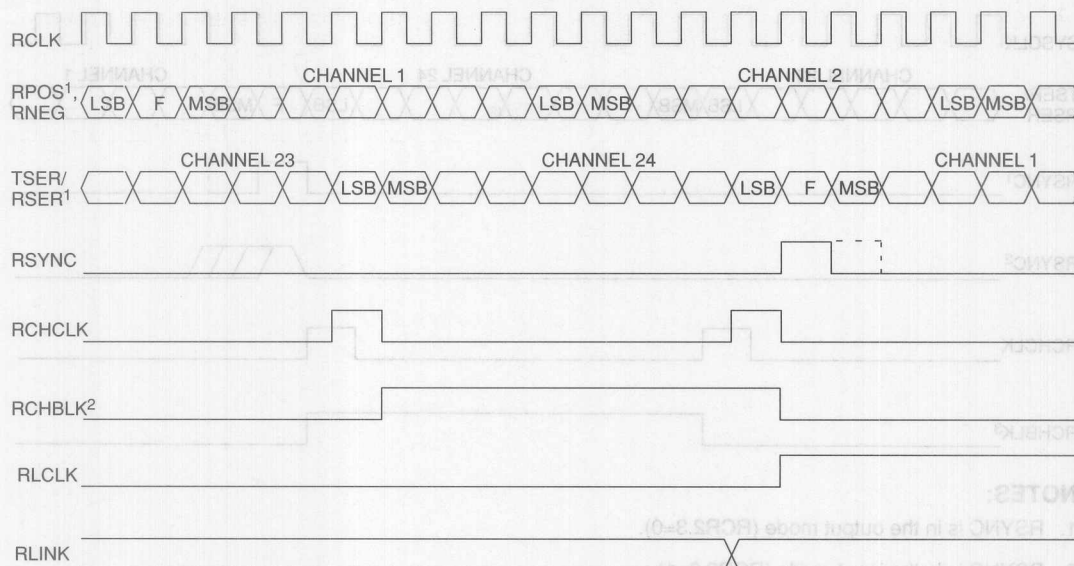
2.048 MHz BOUNDARY TIMING (WITH ELASTIC STORE(S) ENABLED)



NOTES:

1. RSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 are forced to 1; TSER data in these channels will be ignored.
2. RSYNC is in the output mode (RCR2.3=0).
3. RSYNC is in the input mode (RCR2.3=1).
4. RCHBLK is forced to 1 in the same channels as RSER (see Note 1).

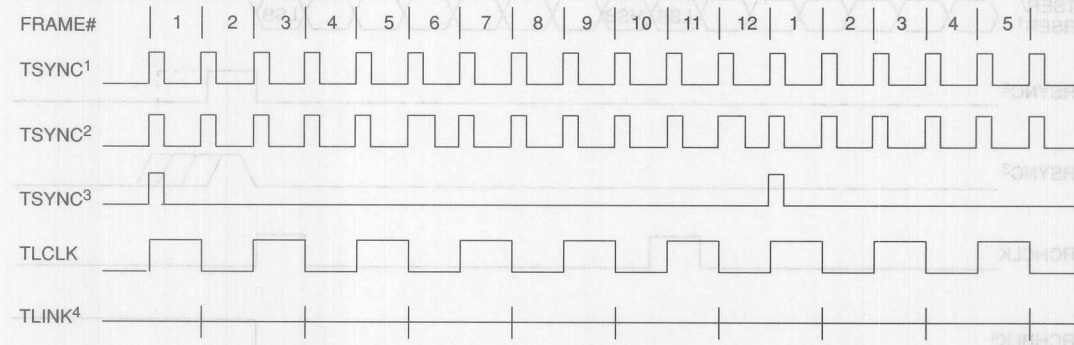
RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORE(S) DISABLED)



NOTES:

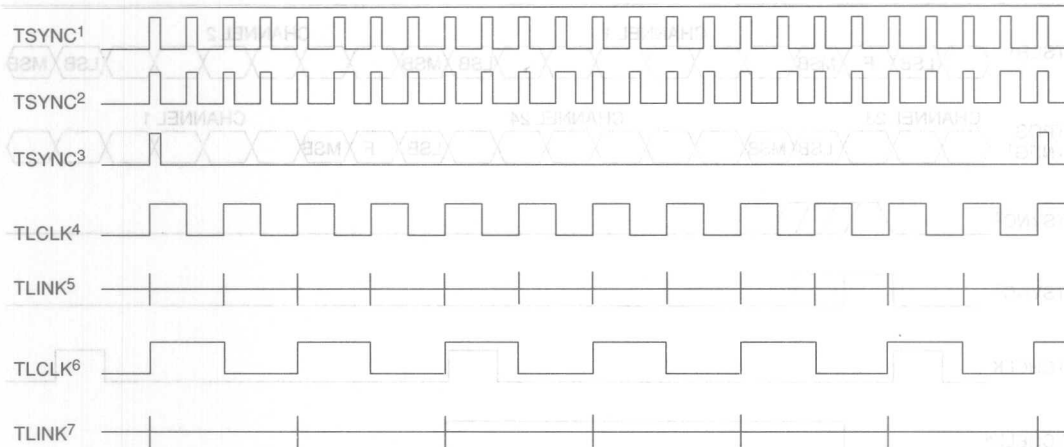
1. There is a 13 RCLK delay from RPOS, RNEG to RSER.
2. RCHBLK is programmed to block channel 24.

TRANSMIT SIDE D4 TIMING



NOTES:

1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.3=1).
4. TLINK data (S-bit) is sampled during the F-bit position of even frames for insertion into the outgoing T1 stream when enabled via TCR1.2.

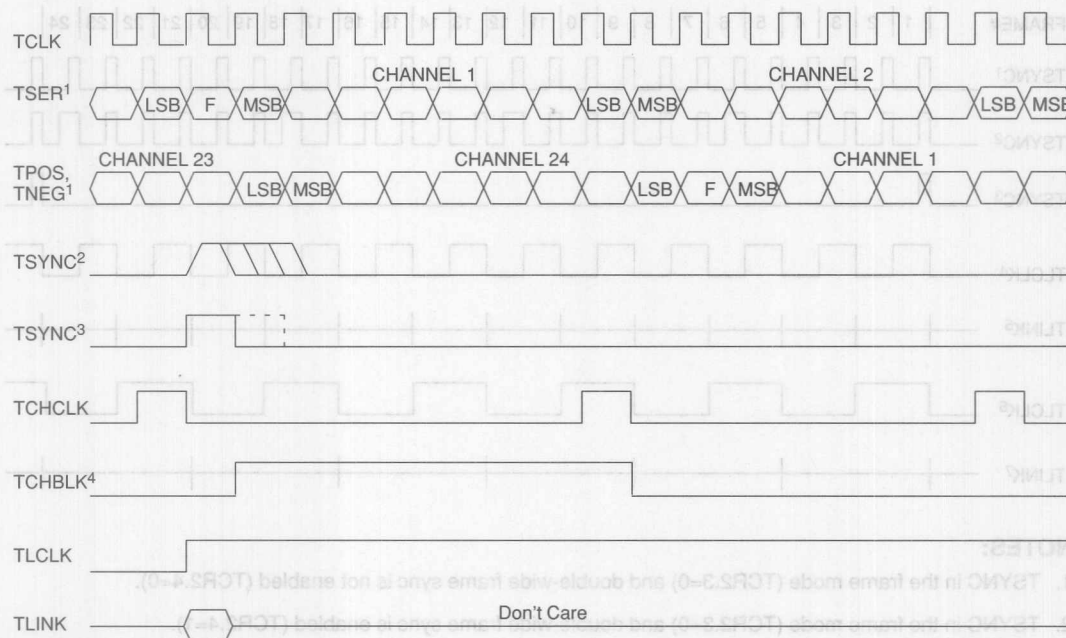
**NOTES:**

1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.4=1).
4. ZBTSI mode disabled (TCR2.5=0).
5. TLINK data (FDL bits) is sampled during the F-bit time of odd frame and inserted into the outgoing T1 stream if enabled via TCR1.2.
6. ZBTSI mode is enabled (TCR2.5=1).
7. TLINK data (Z bits) is sampled during the F-bit time of frame 1, 5, 9, 13, 17, and 21 and inserted into the outgoing stream if enabled via TCR1.2.

**NOTES:**

1. A write to ORB1 will cause the DS2141A to output this sequence.
2. A write to ORB2 will cause the DS2141A to output this sequence.
3. Timing numbers are based on TCLK=1.544 MHz with 50% duty cycle.

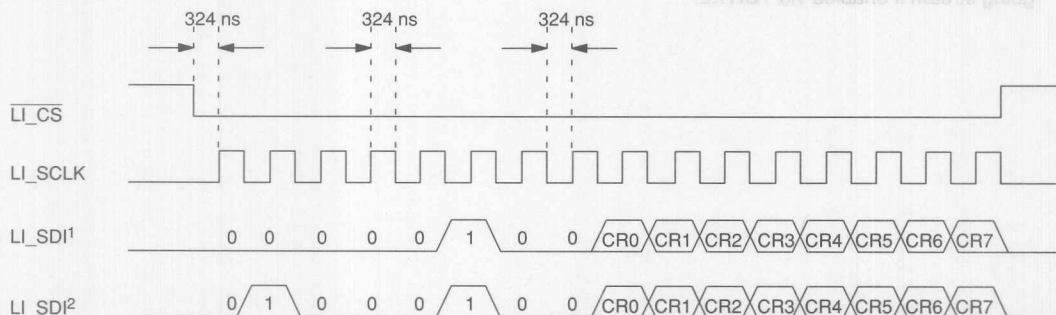
TRANSMIT SIDE BOUNDARY TIMING (WITH ELASTIC STORE(S) DISABLED)



NOTES:

1. There is a 10 TCLK delay from TSER to TPOS, TNEG.
2. TSYNC is in the input mode (TCR2.2=0).
3. TSYNC is in the output mode (TCR2.2=1).
4. TCHBLK is programmed to block channel 1.

LINE INTERFACE CONTROL TIMING



NOTES:

1. A write to CRB1 will cause the DS2141A to output this sequence.
2. A write to CRB2 will cause the DS2141A to output this sequence.
3. Timing numbers are based on RCLK=1.544 MHz with 50% duty cycle.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		10		mA	1
Input Leakage	I_{IL}	-1.0		+1.0	μA	2
Output Leakage	I_{LO}			1.0	μA	3
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

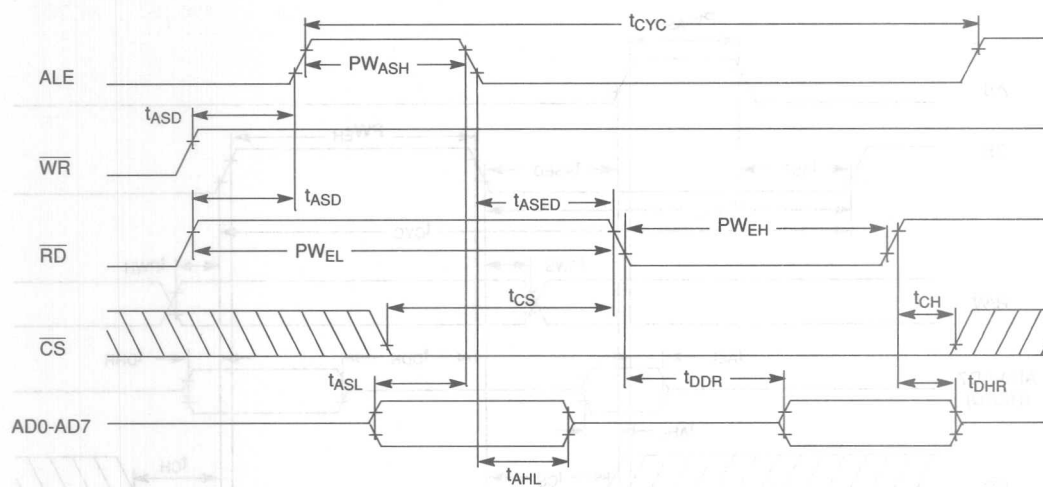
1. $RCLK = TCLK = 1.544 \text{ MHz}$; $V_{DD} = 5.5V$.
2. $0.0V < V_{IN} < V_{DD}$.
3. Applies to $\overline{INT1}$ and $\overline{INT2}$ when 3-stated.

AC CHARACTERISTICS - PARALLEL PORT (0°C to 70°C; V_{DD} = 5V ± 10%)

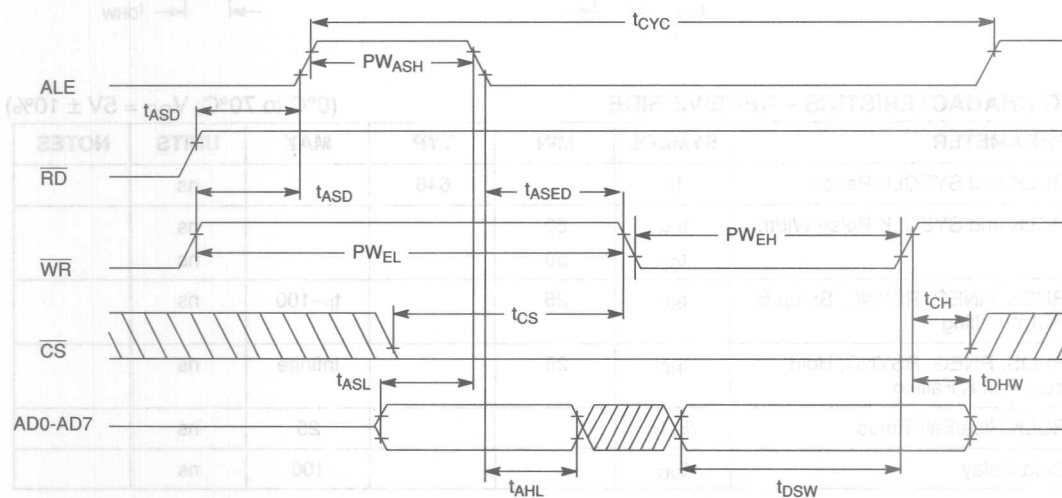
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t _{CYC}	250			ns	
Pulse Width, DS Low or $\overline{\text{RD}}$ High	PW _{EL}	150			ns	
Pulse Width, DS High or $\overline{\text{RD}}$ Low	PW _{EH}	100			ns	
Input Rise/Fall Times	t _R , t _F			30	ns	
R/ $\overline{\text{W}}$ Hold Time	t _{RWH}	10			ns	
R/ $\overline{\text{W}}$ Setup Time Before DS High	t _{RWS}	50			ns	
$\overline{\text{CS}}$ Setup Time Before DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$ active	t _{CS}	20			ns	
$\overline{\text{CS}}$ Hold Time	t _{CH}	0			ns	
Read Data Hold Time	t _{DHR}	10		50	ns	
Write Data Hold Time	t _{DHW}	0			ns	
Muxed Address Valid to AS or ALE fall	t _{ASL}	20			ns	
Muxed Address Hold Time	t _{AHL}	10			ns	
Delay Time DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$ to AS or ALE Rise	t _{ASD}	25			ns	
Pulse Width AS or ALE High	PW _{ASH}	40			ns	
Delay Time, AS or ALE to DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{ASED}	20			ns	
Output Data Delay Time from DS or $\overline{\text{RD}}$	t _{DDR}	20		100	ns	
Data Setup Time	t _{DSW}	80			ns	

NOTES:
1. FCLK = TCLK = 1.544 MHz; V_{DD} = 5.5V.
2. 0.0V < V_{in} < V_{DD}.
3. Applies to INT1 and INT2 when 3-state.

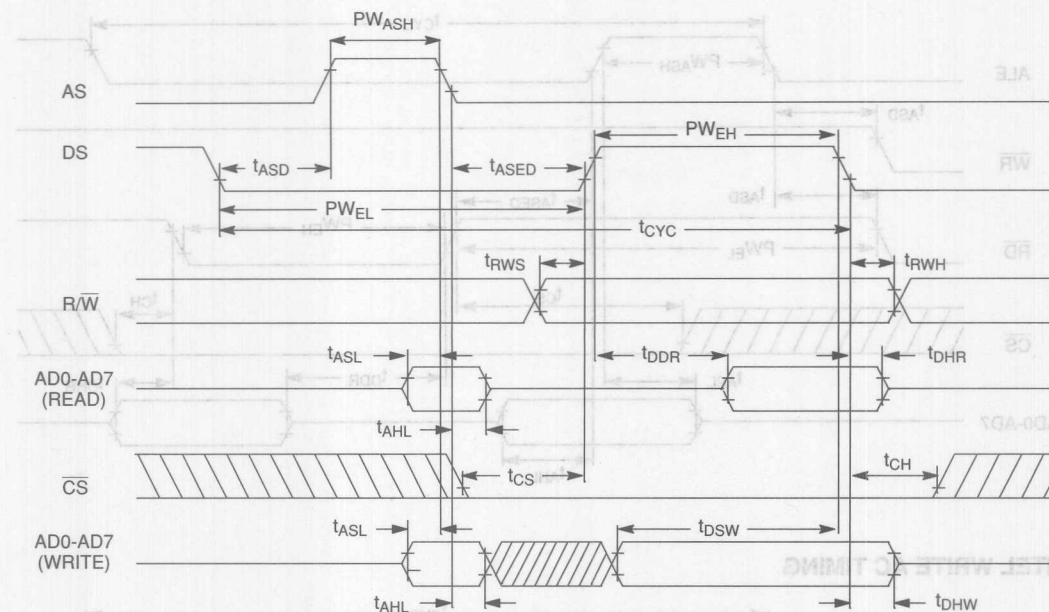
INTEL READ AC TIMING



INTEL WRITE AC TIMING



MOTOROLA AC TIMING

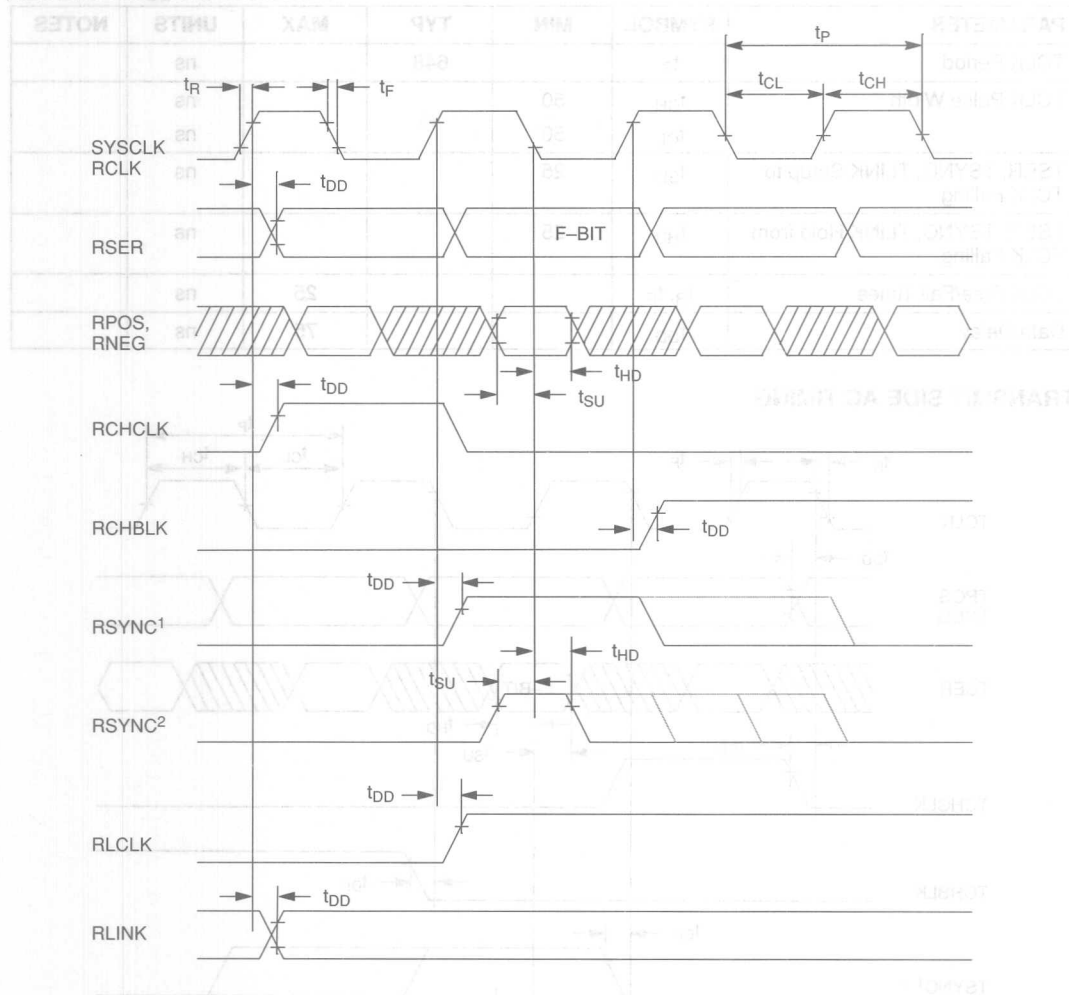


AC CHARACTERISTICS – RECEIVE SIDE

(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK and SYSCLK Period	t_p		648		ns	
RCLK and SYSCLK Pulse Width	t_{CH}	50			ns	
	t_{CL}	50			ns	
RPOS, RNEG, RSYNC, Setup to RCLK Falling	t_{SU}	25		$t_p - 100$	ns	
RPOS, RNEG, RSYNC, Hold from RCLK Falling	t_{HD}	25		infinite	ns	
RCLK Rise/Fall Times	t_R, t_F			25	ns	
Data Delay	t_{DD}			100	ns	

RECEIVE SIDE AC TIMING (1)

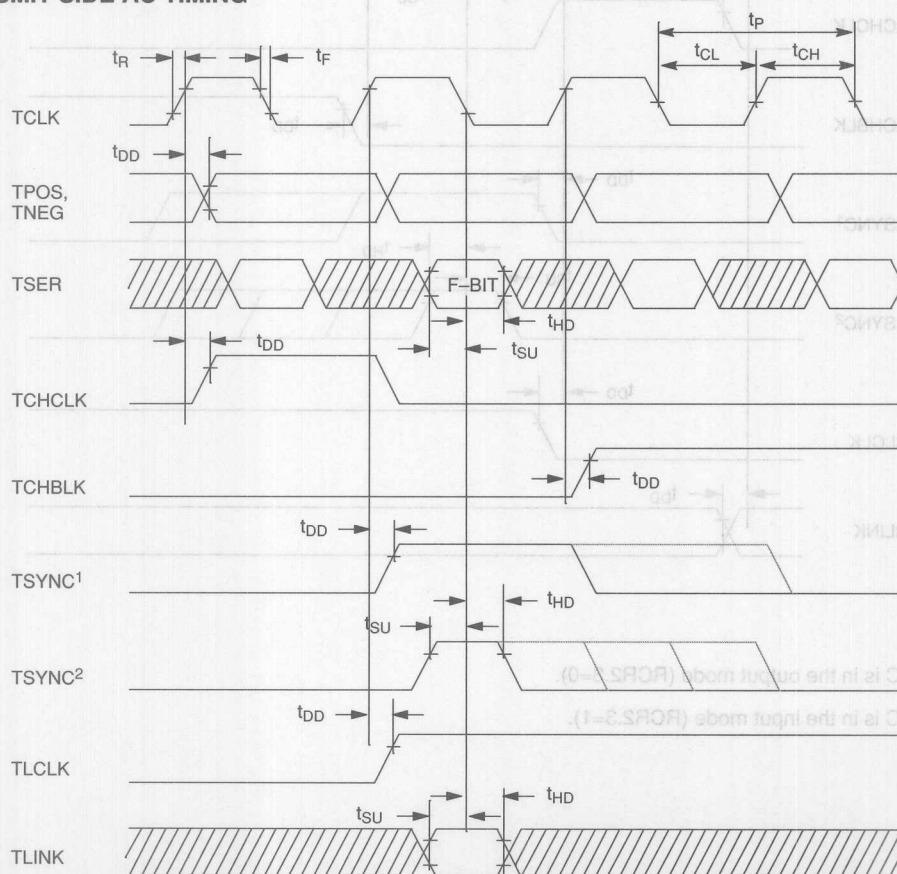


NOTES:

1. RSYNC is in the output mode (RCR2.3=0).
2. RSYNC is in the input mode (RCR2.3=1).

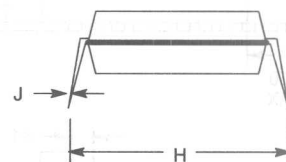
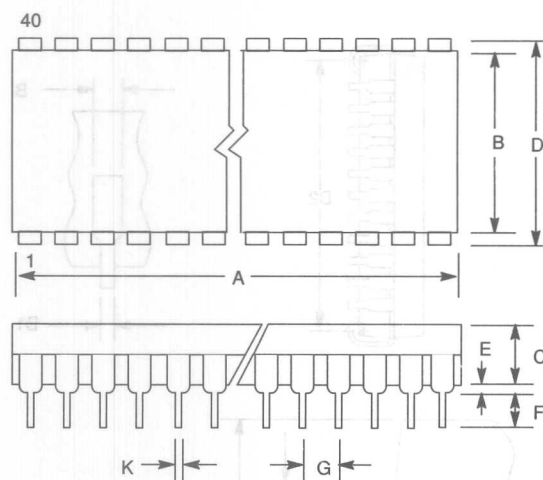
AC CHARACTERISTICS – TRANSMIT SIDE(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_p		648		ns	
TCLK Pulse Width	t_{CH}	50			ns	
	t_{CL}	50			ns	
TSER, TSYNC, TLINK Setup to TCLK Falling	t_{SU}	25			ns	
TSER, TSYNC, TLINK Hold from TCLK Falling	t_{HD}	25			ns	
TCLK Rise/Fall Times	t_R, t_F			25	ns	
Data Delay	t_{DD}			75	ns	

TRANSMIT SIDE AC TIMING**NOTES:**

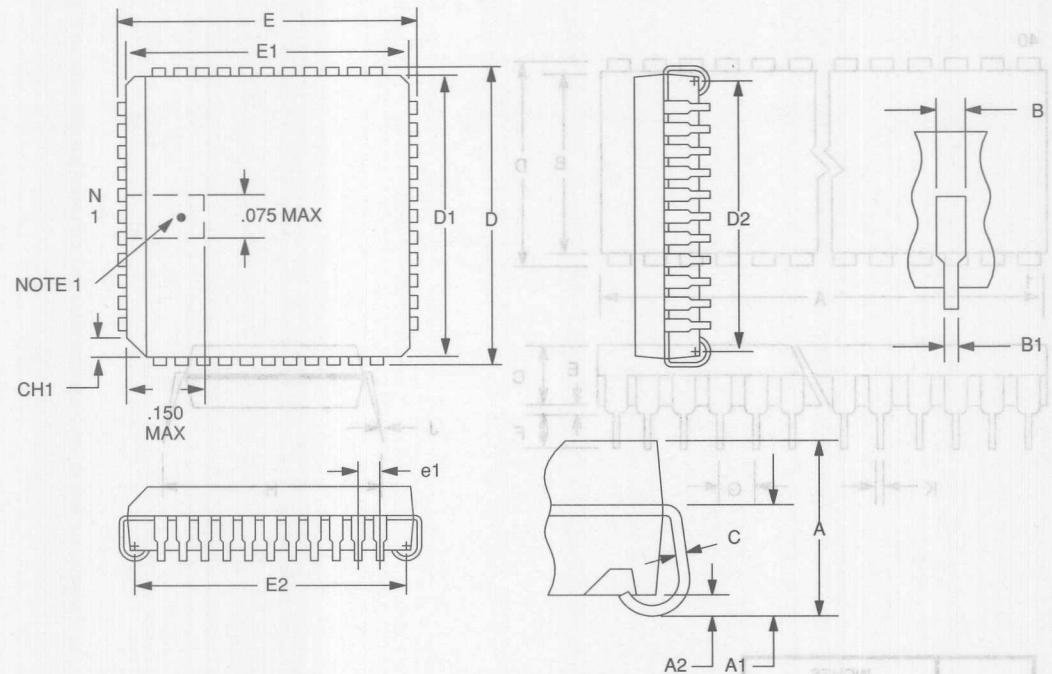
1. TSYNC is in the output mode (TCR2.2=1).
2. TSYNC is in the input mode (TCR2.2=0).

DS2141A T1 CONTROLLER (600 MIL) 40-PIN DIP



DIM	INCHES	
	MIN	MAX
A	2.040	2.070
B	0.530	0.560
C	0.145	0.155
D	0.600	0.625
E	0.015	0.040
F	0.120	0.140
G	0.090	0.110
H	0.625	0.675
J	0.008	0.012
K	0.015	0.022

DS2141AQ T1 CONTROLLER 44-PIN PLCC



DALLAS SEMICONDUCTOR

DS21Q41B Quad T1 Framer

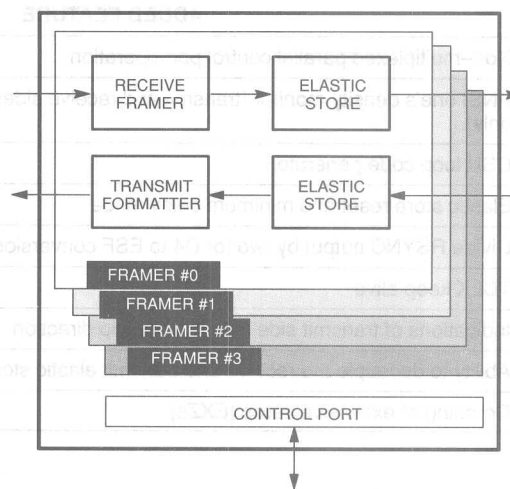
FEATURES

- Four T1 DS1/ISDN-PRI framing transceivers
- All four framers are fully independent
- Frames to D4, ESF, and SLC-96 formats
- 8-bit parallel control port that can be connected to either multiplexed or non-multiplexed buses
- Each of the four framers contains dual two-frame elastic stores that can connect to asynchronous or synchronous backplanes up to 8.192 MHz
- Extracts and inserts robbed bit signaling
- Framer and payload loopbacks
- Large counters for BPVs, LCVs, EXZs, CRC6, PCVs, F-bit errors and the number of multiframes out of sync
- Contains ANSI one's density monitor & enforcer
- CSU loop code generator and detector
- Programmable output clocks for Fractional T1, ISDN-PRI, Actual Size and per channel loopback applications
- Onboard FDL support circuitry
- Pin compatible with DS21Q43 Quad E1 Framer
- 5V supply; low power CMOS
- Available in 128-pin TQFP

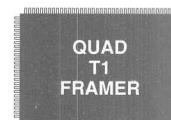
DESCRIPTION

The DS21Q41B combines four of the popular DS2141A T1 Controllers onto a single monolithic die. The "B" designation denotes that some new features are available in the Quad version that were not available in the single T1 device. The added features in the DS21Q41B are listed in Section 1. The DS21Q41B offers a substantial space savings to applications that require more than one T1 framer on a card. The Quad version is only slightly bigger than the single T1 device. All four framers in the DS21Q41B are totally independent, they do

FUNCTIONAL DIAGRAM



ACTUAL SIZE



not share a common framing synchronizer. Also, the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The DS21Q41B meets all of the latest specifications including ANSI T1.403 (and the emerging T1.403-199X), ANSI T1.231-1993, AT&T TR62411, AT&T TR54016, ITU G.704 and G.706.

1.0 INTRODUCTION

The DS21Q41B Quad T1 Framer is made up of five main parts: framer #0, framer #1, framer #2, framer #3, and the control port which is shared by all four framers. See the Block Diagram in Figure 1-1. Each of the four framers within the DS21Q41B maintain the same register structure that appeared in the DS2141A. The two framer select inputs (FS0 and FS1) are used to determine which framer within the DS21Q41B is being

accessed. In this manner, software written for the DS2141A can also be used with only slight modifications, in the DS21Q41B.

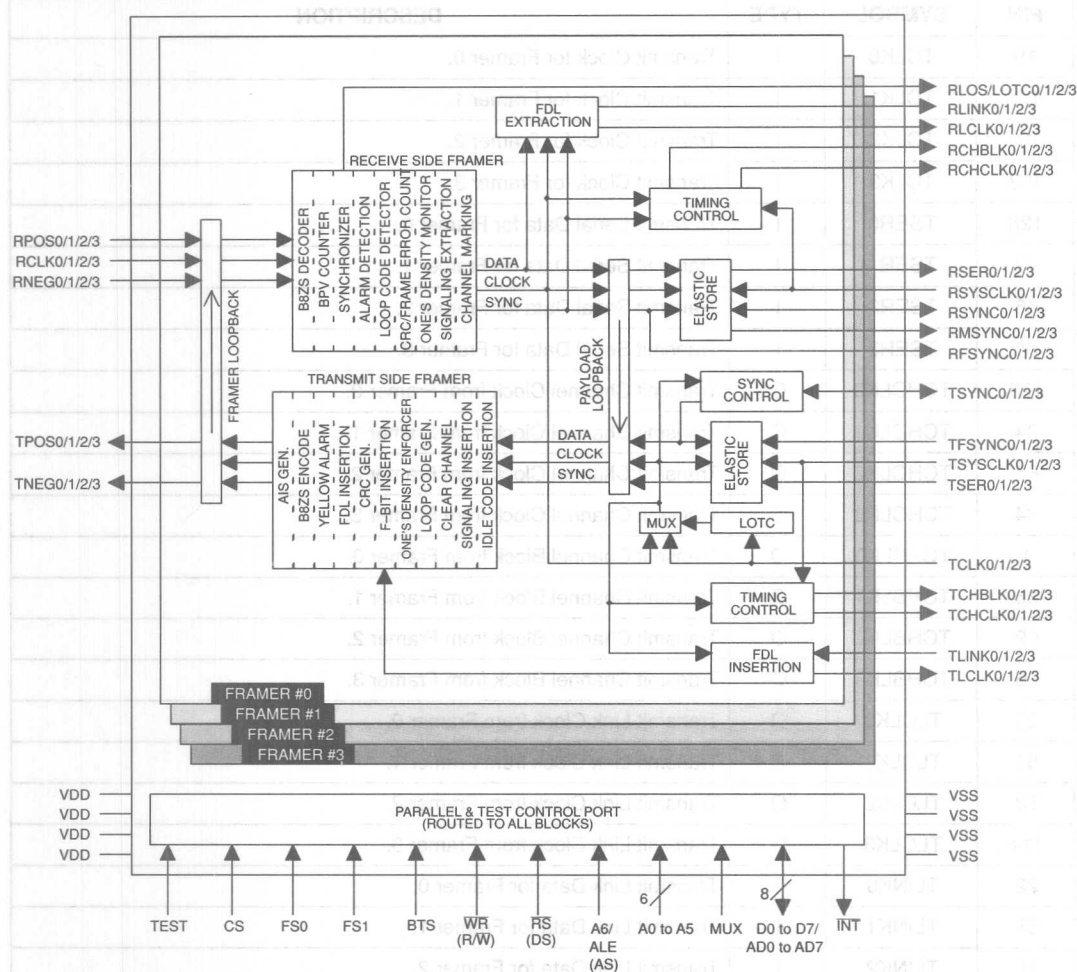
Several new features have been added to the framers in the DS21Q41B over the DS2141A. Below is short list of the new features. More details can be found in Sections 2 through 12.

ADDED FEATURE	SECTION
Non-multiplexed parallel control port operation	2
ANSI one's density monitor (transmit and receive sides) and enforcer (transmit side only)	3 and 4
CSU loop code generator	3
Elastic store reset and minimum delay mode	3 and 10
Divide RSYNC output by two for D4 to ESF conversion applications	3
TCLK keep alive	3
Indications of transmit side elastic store slip direction	4
Ability to decouple the receive and transmit elastic stores	10
Counting of excessive zeros (EXZs)	5

not share a common framing synchronizer. Also, the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The DS21Q41B meets all of the latest specifications including ANSI T1.403 (and the emerging T1.403-199X), ANSI T1.231-1983, AT&T TRS411, AT&T TRS401, ITU G.704 and G.706.

The DS21Q41B combines four of the popular DS2141A T1 Controllers onto a single monolithic die. The "B" designation denotes that some new features are available in the Quad version that were not available in the single T1 device. The added features in the DS21Q41B are listed in Section 1. The DS21Q41B offers a substantial space savings to applications that require more than one T1 framer on a card. The Quad version is only slightly bigger than the single T1 device. All four framers in the DS21Q41B are totally independent, they do

DS21Q41B BLOCK DIAGRAM Figure 1-1



TRANSMIT PIN LIST Table 1-1

PIN	SYMBOL	TYPE	DESCRIPTION
19	TCLK0	I	Transmit Clock for Framer 0.
53	TCLK1	I	Transmit Clock for Framer 1.
87	TCLK2	I	Transmit Clock for Framer 2.
113	TCLK3	I	Transmit Clock for Framer 3.
126	TSER0	I	Transmit Serial Data for Framer 0.
32	TSER1	I	Transmit Serial Data for Framer 1.
66	TSER2	I	Transmit Serial Data for Framer 2.
92	TSER3	I	Transmit Serial Data for Framer 3.
128	TCHCLK0	O	Transmit Channel Clock from Framer 0.
34	TCHCLK1	O	Transmit Channel Clock from Framer 1.
68	TCHCLK2	O	Transmit Channel Clock from Framer 2.
94	TCHCLK3	O	Transmit Channel Clock from Framer 3.
1	TCHBLK0	O	Transmit Channel Block from Framer 0.
35	TCHBLK1	O	Transmit Channel Block from Framer 1.
69	TCHBLK2	O	Transmit Channel Block from Framer 2.
95	TCHBLK3	O	Transmit Channel Block from Framer 3.
20	TLCLK0	O	Transmit Link Clock from Framer 0.
54	TLCLK1	O	Transmit Link Clock from Framer 1.
88	TLCLK2	O	Transmit Link Clock from Framer 2.
114	TLCLK3	O	Transmit Link Clock from Framer 3.
22	TLINK0	I	Transmit Link Data for Framer 0.
56	TLINK1	I	Transmit Link Data for Framer 1.
90	TLINK2	I	Transmit Link Data for Framer 2.
116	TLINK3	I	Transmit Link Data for Framer 3.
2	TPOS0	O	Transmit Bipolar Data from Framer 0.
36	TPOS1	O	Transmit Bipolar Data from Framer 1.
70	TPOS2	O	Transmit Bipolar Data from Framer 2.
96	TPOS3	O	Transmit Bipolar Data from Framer 3.
3	TNEG0	O	Transmit Bipolar Data from Framer 0.
37	TNEG1	O	Transmit Bipolar Data from Framer 1.
71	TNEG2	O	Transmit Bipolar Data from Framer 2.
97	TNEG3	O	Transmit Bipolar Data from Framer 3.

PIN	SYMBOL	TYPE	DESCRIPTION
21	TSYNC0	I/O	Transmit Sync for Framer 0.
55	TSYNC1	I/O	Transmit Sync for Framer 1.
89	TSYNC2	I/O	Transmit Sync for Framer 2.
115	TSYNC3	I/O	Transmit Sync for Framer 3.
127	TFSYNC0	I	Transmit Sync for Elastic Store in Framer 0.
33	TFSYNC1	I	Transmit Sync for Elastic Store in Framer 1.
67	TFSYNC2	I	Transmit Sync for Elastic Store in Framer 2.
93	TFSYNC3	I	Transmit Sync for Elastic Store in Framer 3.
125	TSYSCLK0	I	Transmit System Clock for Elastic Store in Framer 0.
31	TSYSCLK1	I	Transmit System Clock for Elastic Store in Framer 1.
65	TSYSCLK2	I	Transmit System Clock for Elastic Store in Framer 2.
91	TSYSCLK3	I	Transmit System Clock for Elastic Store in Framer 3.

RECEIVE PIN LIST Table 1–2

PIN	SYMBOL	TYPE	DESCRIPTION
6	RCLK0	I	Receive Clock for Framer 0.
40	RCLK1	I	Receive Clock for Framer 1.
74	RCLK2	I	Receive Clock for Framer 2.
100	RCLK3	I	Receive Clock for Framer 3.
13	RSER0	O	Receive Serial Data from Framer 0.
49	RSER1	O	Receive Serial Data from Framer 1.
83	RSER2	O	Receive Serial Data from Framer 2.
107	RSER3	O	Receive Serial Data from Framer 3.
9	RCHCLK0	O	Receive Channel Clock from Framer 0.
43	RCHCLK1	O	Receive Channel Clock from Framer 1.
77	RCHCLK2	O	Receive Channel Clock from Framer 2.
103	RCHCLK3	O	Receive Channel Clock from Framer 3.
10	RCHBLK0	O	Receive Channel Block from Framer 0.
44	RCHBLK1	O	Receive Channel Block from Framer 1.
80	RCHBLK2	O	Receive Channel Block from Framer 2.
104	RCHBLK3	O	Receive Channel Block from Framer 3.
5	RLCLK0	O	Receive Link Clock from Framer 0.
39	RLCLK1	O	Receive Link Clock from Framer 1.
73	RLCLK2	O	Receive Link Clock from Framer 2.

PIN	SYMBOL	TYPE	DESCRIPTION
99	RLCLK3	O	Receive Link Clock from Framer 3.
4	RLINK0	O	Receive Link Data from Framer 0.
38	RLINK1	O	Receive Link Data from Framer 1.
72	RLINK2	O	Receive Link Data from Framer 2.
98	RLINK3	O	Receive Link Data from Framer 3.
8	RPOS0	I	Receive Bipolar Data for Framer 0.
42	RPOS1	I	Receive Bipolar Data for Framer 1.
76	RPOS2	I	Receive Bipolar Data for Framer 2.
102	RPOS3	I	Receive Bipolar Data for Framer 3.
7	RNEG0	I	Receive Bipolar Data for Framer 0.
41	RNEG1	I	Receive Bipolar Data for Framer 1.
75	RNEG2	I	Receive Bipolar Data for Framer 2.
101	RNEG3	I	Receive Bipolar Data for Framer 3.
12	RSYNC0	I/O	Receive Sync for Framer 0.
48	RSYNC1	I/O	Receive Sync for Framer 1.
82	RSYNC2	I/O	Receive Sync for Framer 2.
106	RSYNC3	I/O	Receive Sync for Framer 3.
17	RFSYNC0	O	Receive Frame Sync from Framer 0.
51	RFSYNC1	O	Receive Frame Sync from Framer 1.
85	RFSYNC2	O	Receive Frame Sync from Framer 2.
109	RFSYNC3	O	Receive Frame Sync from Framer 3.
16	RMSYNC0	O	Receive Multiframe Sync from Framer 0.
50	RMSYNC1	O	Receive Multiframe Sync from Framer 1.
84	RMSYNC2	O	Receive Multiframe Sync from Framer 2.
108	RMSYNC3	O	Receive Multiframe Sync from Framer 3.
11	RSYSCLK0	I	Receive System Clock for Elastic Store in Framer 0.
45	RSYSCLK1	I	Receive System Clock for Elastic Store in Framer 1.
81	RSYSCLK2	I	Receive System Clock for Elastic Store in Framer 2.
105	RSYSCLK3	I	Receive System Clock for Elastic Store in Framer 3.
18	RLOS/LOT0	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 0.
52	RLOS/LOT1	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 1.
86	RLOS/LOT2	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 2.
112	RLOS/LOT3	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 3.

CONTROL PORT/TEST/SUPPLY PIN LIST Table 1–3

PIN	SYMBOL	TYPE	DESCRIPTION
57	TEST	I	3-State Control for all Output and I/O Pins.
60	CS	I	Chip Select.
58	FS0	I	Framer Select 0 for Parallel Control Port.
59	FS1	I	Framer Select 1 for Parallel Control Port.
61	BTS	I	Bus Type Select for Parallel Control Port.
63	WR(R/W)	I	Write Input (Read/Write).
62	RD (DS)	I	Read Input (Data Strobe).
23	A0	I	Address Bus Bit 0; LSB
24	A1	I	Address Bus Bit 1.
25	A2	I	Address Bus Bit 2.
26	A3	I	Address Bus Bit 3.
27	A4	I	Address Bus Bit 4.
28	A5	I	Address Bus Bit 5.
29	A6 or ALE (AS)	I	Address Bus Bit 6; MSB or Address Latch Enable (Address Strobe).
30	INT	O	Receive Alarm Interrupt for all Four Framers.
64	MUX	I	Non-Multiplexed or Multiplexed Bus Select.
117	D0 or AD0	I/O	Data Bus Bit 0 or Address/Data Bus Bit 0; LSB.
118	D1 or AD1	I/O	Data Bus Bit 1 or Address/Data Bus Bit 1.
119	D2 or AD2	I/O	Data Bus Bit 2 or Address/Data Bus Bit 2.
120	D3 or AD3	I/O	Data Bus Bit 3 or Address/Data Bus Bit 3.
121	D4 or AD4	I/O	Data Bus Bit 4 or Address/Data Bus Bit 4.
122	D5 or AD5	I/O	Data Bus Bit 5 or Address/Data Bus Bit 5.
123	D6 or AD6	I/O	Data Bus Bit 6 or Address/Data Bus Bit 6.
124	D7 or AD7	I/O	Data Bus Bit 7 or Address/Data Bus Bit 7; MSB.
15	V _{DD}	–	Positive Supply Voltage.
47	V _{DD}	–	Positive Supply Voltage.
79	V _{DD}	–	Positive Supply Voltage.
111	V _{DD}	–	Positive Supply Voltage.
14	V _{SS}	–	Signal Ground.
46	V _{SS}	–	Signal Ground.
78	V _{SS}	–	Signal Ground.
110	V _{SS}	–	Signal Ground.

DS21Q41B PIN DESCRIPTION Table 1-4

Transmit Clock [TCLK]. 1.544 MHz primary clock. Used to clock data through the transmit side formatter.

Transmit Serial Data [TSER]. Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYCLK when the transmit side elastic store is enabled.

Transmit Channel Clock [TCHCLK]. 192 KHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 12 for timing details.

Transmit Bipolar Data [TPOS and TNEG]. Updated on rising edge of TCLK. Can be programmed to output NRZ data on TPOS via the TCR1.7 control bit.

Transmit Channel Block [TCHBLK]. A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384Kbps service, 768Kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 12 for timing details.

Transmit System Clock [TSYCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store.

Transmit Link Clock [TLCLK]. 4 KHz or 2 KHz (ZBTSI) demand clock for the TLINK input. See Section 12 for timing details.

Transmit Link Data [TLINK]. If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 12 for timing details.

Transmit Sync [TSYNC]. A pulse at this pin will establish either frame or multiframe boundaries for the DS21Q41B. Via TCR2.2, the DS21Q41B can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 12 for timing details.

Transmit Frame Sync [TFSYNC]. 8 KHz pulse. Only used when the transmit side elastic store is enabled. A pulse at this pin will establish frame boundaries for the DS21Q41B. Should be tied low in applications that do not use the transmit side elastic store. See Section 12 for timing details.

Receive Link Data [RLINK]. Updated with either FDL data (ESF) or Fs bits (D4) or Z-bits (ZBTSI) one RCLK before the start of a frame. See Section 12 for timing details.

Receive Link Clock [RLCLK]. 4 KHz or 2 KHz (ZBTSI) demand clock for the RLINK input. See Section 12 for timing details.

Receive Clock [RCLK]. 1.544 MHz primary clock. Used to clock data through the receive side of the framer.

Receive Channel Clock [RCHCLK]. 192 KHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 12 for timing details.

Receive Channel Block [RCHBLK]. A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384Kbps service, 768Kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 12 for timing details.

Receive Serial Data [RSER]. Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYCLK when the receive side elastic store is enabled.

Receive Sync [RSYNC]. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4=0) or multiframe boundaries (RCR2.4=1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the receive side elastic store is enabled, then this pin can be enabled to be an input at which a frame boundary pulse is applied. See Section 12 for timing details.

Receive Frame Sync (RFSYNC). An extracted 8 KHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries. See Section 12 for timing details.

Receive Multiframe Sync [RMSYNC]. Only used when the receive side elastic store is enabled. An extracted pulse, one RSYCLK wide, is output at this pin which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output should be ignored. See Section 12 for timing details.

Receive Bipolar Data Inputs [RPOS and RNEG]. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.

Receive System Clock [RSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store.

Receive Loss of Sync/Loss of Transmit Clock [RLOS/LOTCL]. A dual function output. If CCR1.6=0, then this pin will toggle high when the synchronizer is searching for the T1 frame and multiframe. If CCR1.6=1, then this pin will toggle high if the TCLK pin has not been toggled for 5 μ s.

Receive Alarm Interrupt [INT]. Flags host controller during conditions defined in the Status Registers of the four framers. User can poll the Interrupt Status Register

(ISR) to determine which status register in which framer is active (if any). Active low, open drain output.

3-State Control [Test]. Set high to 3-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.

Bus Operation [MUX]. Set low to select non-multiplexed bus operation. Set high to select multiplexed bus operation.

Data Bus [D0 to D7] or Address/Data Bus [AD0 to AD7]. In non-multiplexed bus operation (MUX=0), serves as the data bus. In multiplexed bus operation (MUX=1), serves as a 8-bit multiplexed address/data bus.

Address Bus [A0 to A5]. In non-multiplexed bus operation (MUX=0), serves as the address bus. In multiplexed bus operation (MUX=1), these pins are not used and should be tied low.

Bus Type Select [BTS]. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the \overline{RD} (DS), ALE(AS), and \overline{WR} (R/W) pins. If BTS=1, then these pins assume the function listed in parenthesis ().

Read Input [RD] (Data Strobe [DS]).

Framer Selects [FS0 and FS1]. Selects which of the four framers to be accessed.

Chip Selects [CS]. Must be low to read or write to any of the four framers.

A6 or Address Latch Enable [ALE] (Address Strobe [AS]). In non-multiplexed bus operation (MUX=0), serves as the upper address bit. In multiplexed bus operation (MUX=1), serves to demultiplex the bus on a positive-going edge.

Write Input [WR] (Read/Write [R/W]).

Positive Supply [V_{DD}]. 5.0 volts \pm 0.5volts.

Signal Ground [V_{SS}]. 0.0 volts.

DS21Q41B REGISTER MAP Table 1–5

ADDRESS	R/W	REGISTER NAME
20	R/W	Status Register 1.
21	R/W	Status Register 2.
22	R/W	Receive Information Register 1.
23	R	Line Code Violation Count Register 1.
24	R	Line Code Violation Count Register 2.
25	R	Path Code Violation Count Register 1 ⁽¹⁾ .
26	R	Path Code Violation Count Register 2.
27	R	Multiframe Out of Sync Count Register 2.
28	R	Receive FDL Register.
29	R/W	Receive FDL Match Register 1.
2A	R/W	Receive FDL Match Register 2.
2B	R/W	Receive Control Register 1.
2C	R/W	Receive Control Register 2.
2D	R/W	Receive Mark Register 1.
2E	R/W	Receive Mark Register 2.
2F	R/W	Receive Mark Register 3.
30	R/W	Common Control Register 3.
31	R/W	Receive Information Register 2.
32	R/W	Transmit Channel Blocking Register 1.
33	R/W	Transmit Channel Blocking Register 2.
34	R/W	Transmit Channel Blocking Register 3.
35	R/W	Transmit Control Register 1.
36	R/W	Transmit Control Register 2.
37	R/W	Common Control Register 1.
38	R/W	Common Control Register 2.
39	R/W	Transmit Transparency Register 1.
3A	R/W	Transmit Transparency Register 2.
3B	R/W	Transmit Transparency Register 3.
3C	R/W	Transmit Idle Register 1.
3D	R/W	Transmit Idle Register 2.
3E	R/W	Transmit Idle Register 3.

NOTES:

1. Address 25 also contains Multiframe Out of Sync Count Register 1.
2. The Test Registers are used only by the factory; these registers must be cleared (set to all zeros) on power-up initialization to insure proper operation.
3. Any unused register address will allow the status of the interrupts to appear on the bus.

ADDRESS	R/W	REGISTER NAME
3F	R/W	Transmit Idle Definition Register.
60	R	Receive Signaling Register 1.
61	R	Receive Signaling Register 2.
62	R	Receive Signaling Register 3.
63	R	Receive Signaling Register 4.
64	R	Receive Signaling Register 5.
65	R	Receive Signaling Register 6.
66	R	Receive Signaling Register 7.
67	R	Receive Signaling Register 8.
68	R	Receive Signaling Register 9.
69	R	Receive Signaling Register 10.
6A	R	Receive Signaling Register 11.
6B	R	Receive Signaling Register 12.
6C	R/W	Receive Channel Blocking Register 1.
6D	R/W	Receive Channel Blocking Register 2.
6E	R/W	Receive Channel Blocking Register 3.
6F	R/W	Interrupt Mast Register 2.
70	R/W	Transmit Signaling Register 1.
71	R/W	Transmit Signaling Register 2.
72	R/W	Transmit Signaling Register 3.
73	R/W	Transmit Signaling Register 4.
74	R/W	Transmit Signaling Register 5.
75	R/W	Transmit Signaling Register 6.
76	R/W	Transmit Signaling Register 7.
77	R/W	Transmit Signaling Register 8.
78	R/W	Transmit Signaling Register 9.
79	R/W	Transmit Signaling Register 10.
7A	R/W	Transmit Signaling Register 11.
7B	R/W	Transmit Signaling Register 12.
7C	R/W	Test Register ⁽²⁾ .
7D	R/W	Test Register ⁽²⁾ .
7E	R/W	Transmit FDL Register.
7F	R/W	Interrupt Mask Register 1.

DS21Q41B FRAMER DECODE Table 1–6

FS1	FS0	FRAMER ACCESSED
0	0	#0
0	1	#1
1	0	#2
1	1	#3

2.0 PARALLEL PORT

The DS21Q41B is controlled via either a non-multiplexed (MUX=0) or multiplexed (MUX=1) by an external microcontroller or microprocessor. The DS21Q41B can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics for more details.

3.0 CONTROL REGISTERS

The operation of each framer within the DS21Q41B is configured via a set of seven registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS21Q41B has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and three Common Control Registers (CCR1, CCR2, and CCR3).

RCR1: RECEIVE CONTROL REGISTER 1 (Address=2B Hex)

(MSB)				(LSB)			
LCVCRF	ARC	OOF1	OOF2	SYNCC	CYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
LCVCRF	RCR1.7	Line Code Violation Count Register Function Select. 0=do not count excessive zeros 1=count excessive zeros
ARC	RCR1.6	Auto Resync Criteria. 0=Resync on OOF or RCL event 1=Resync on OOF only
OOF1	RCR1.5	Out Of Frame Select 1. 0=2/4 frame bits in error 1=2/5 frame bits in error
OOF2	RCR1.4	Out Of Frame Select 2. 0=follow RCR1.5 1=2/6 frame bits in error
SYNCC	RCR1.3	Sync Criteria. In D4 Framing Mode 0=search for Ft pattern, then search for Fs pattern 1=cross couple Ft and Fs pattern In ESF Framing Mode 0=search for FPS pattern only 1=search for FPS and verify with CRC6
SYNCT	RCR1.2	Sync Time. 0=qualify 10 bits 1=qualify 24 bits

SYNCE	RCR1.1	Sync Enable. 0=auto resync enabled 1=auto resync disabled
RESYNC	RCR1.0	Resync. When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

RCR2: RECEIVE CONTROL REGISTER 2 (Address=2C Hex)

(MSB)							(LSB)
RCS	ZBTSI	RSDW	RSM	RSIO	D4YM	FSBE	MOSCRF
SYMBOL	POSITION	NAME AND DESCRIPTION					
RCS	RCR2.7	Receive Code Select. 0=idle code (7F Hex) 1=digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex)					
ZBTSI	RCR2.6	ZBTSI Enable. 0=ZBTSI disabled 1=ZBTSI enabled					
RSDW	RCR2.5	RSYNC Double-Wide. 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames (note: this bit must be set to zero when RCR2.4=1 or when RCR2.3=1)					
RSM	RCR2.4	RSYNC Mode Select. 0=frame mode (see the timing in Section 12) 1=multiframe mode (see the timing in Section 12)					
RSIO	RCR2.3	RSYNC I/O Select. 0=RSYNC is an output 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to zero when CCR1.2=0)					
D4YM	RCR2.2	D4 Yellow Alarm Select. 0=zeros in bit 2 of all channels 1=a one in the S-bit position of frame 12					
FSBE	RCR2.1	PCVCR Fs Bit Error Report Enable. 0=do not report bit errors in Fs bit position; only Ft bit position 1=report bit errors in Fs bit position as well as Ft bit position					
MOSCRF	RCR2.0	Multiframe Out of Sync Count Register Function Select. 0=count errors in the framing bit position 1=count the number of multiframe out of sync					

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=35 Hex)

(MSB)

(LSB)

LOTCMC	TFPT	TCPT	RBSE	GB7S	TLINK	TBL	TYEL
--------	------	------	------	------	-------	-----	------

SYMBOL	POSITION	NAME AND DESCRIPTION
LOTCMC	TCR1.7	Loss Of Transmit Clock Mux Control. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK input should fail to transition (see Figure 1–1 for details). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
TFPT	TCR1.6	Transmit Framing Pass Through. (see note below) 0=Ft or FPS bits sourced internally 1=Ft or FPS bits sampled at TSER during F–bit time
TCPT	TCR1.5	Transmit CRC Pass Through. (see note below) 0=source CRC6 bits internally 1=CRC6 bits sampled at TSER during F–bit time
RBSE	TCR1.4	Robbed Bit Signaling Enable. (see note below) 0=no signaling is inserted in any channel 1=signaling is inserted in all channels (the TTR registers can be used to block insertion on a channel by channel basis)
GB7S	TCR1.3	Global Bit 7 Stuffing. (see note below) 0=allow the TTR registers to determine which channels containing all zeros are to be Bit 7 stuffed 1=force Bit 7 stuffing in all zero byte channels regardless of how the TTR registers are programmed
TLINK	TCR1.2	TLINK Select. (see note below) 0=source FDL or Fs bits from TFDL register 1=source FDL or Fs bits from the TLINK pin
TBL	TCR1.1	Transmit Blue Alarm. (see note below) 0=transmit data normally 1=transmit an unframed all one's code at TPOS and TNEG
TYEL	TCR1.0	Transmit Yellow Alarm. (see note below) 0=do not transmit yellow alarm 1=transmit yellow alarm

Note: for a detailed description of how the bits in TCR1 affect the transmit side formatter of the DS21Q41, please see Figure 12–9.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=36 Hex)

(MSB)				(LSB)			
TEST1	TEST0	ZBTSI	TSDW	TSM	TSIO	D4YM	B7ZS
SYMBOL	POSITION	NAME AND DESCRIPTION					
TEST1	TCR2.7	Test Mode Bit 1 for Output Pins. See Table 3–1.					
TEST0	TCR2.6	Test Mode Bit 0 for Output Pins. See Table 3–1.					
ZBTSI	TCR2.5	ZBTSI Enable. 0=ZBTSI disabled 1=ZBTSI enabled					
TSDW	TCR2.4	TSYNC Double–Wide. (Note: this bit must be set to zero when TCR2.3=1 or when TCR2.2=0) 0=do not pulse double–wide in signaling frames 1=do pulse double–wide in signaling frames					
TSM	TCR2.3	TSYNC Mode Select. 0=frame mode (see the timing in Section 12) 1=multiframe mode (see the timing in Section 12)					
TSIO	TCR2.2	TSYNC I/O Select. 0=TSYNC is an input 1=TSYNC is an output					
D4YM	TCR2.1	D4 Yellow Alarm Select. 0=zeros in bit 2 of all channels 1=a one in the S–bit position of frame 12					
B7ZS	TCR2.0	Bit 7 Zero Suppression Enable. 0=no stuffing occurs 1=Bit 7 force to a one in channels with all zeros					

OUTPUT PIN TEST MODES Table 3–1

TEST1	TEST0	EFFECT ON OUTPUT PINS
0	0	Operate normally
0	1	Force all output pins 3–state (including all I/O pins and parallel port pins)
1	0	Force all output pins low (including all I/O pins except parallel port pins)
1	1	Force all output pins high (including all I/O pins except parallel port pins)

CCR1: COMMON CONTROL REGISTER 1 (Address=37 Hex)

(MSB)

(LSB)

TESE	ODF	RSAO	TSCLKM	RSCLKM	RESE	PLB	FLB
------	-----	------	--------	--------	------	-----	-----

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR1.7	Transmit Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled
ODF	CCR1.6	Output Data Format. 0=bipolar data at TPOS and TNEG 1=NRZ data at TPOS; TNEG=0
RSAO	CCR1.5	Receive Signaling All One's. 0=allow robbed signaling bits to appear at RSER 1=force all robbed signaling bits at RSER to one
TSCLKM	CCR1.4	TSYSCLK Mode Select. 0=if TSYSCLK is 1.544 MHz 1=if TSYSCLK is 2.048 MHz
RSCLKM	CCR1.3	RSYSCLK Mode Select. 0=if RSYSCLK is 1.544 MHz 1=if RSYSCLK is 2.048 MHz
RESE	CCR1.2	Receive Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled
PLB	CCR1.1	Payload Loopback. 0=loopback disabled 1=loopback enabled
FLB	CCR1.0	Framer Loopback. 0=loopback disabled 1=loopback enabled

PAYLOAD LOOPBACK

When CCR1.1 is set to a one, the DS21Q41B will be forced into Payload LoopBack (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS21Q41B will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS21Q41B. When PLB is enabled, the following will occur:

1. data will be transmitted from the TPOS and TNEG pins synchronous with RCLK instead of TCLK
2. all of the receive side signals will continue to operate normally
3. the TCHCLK and TCHBLK signals are forced low

4. data at the TSER pin is ignored
5. the TLCLK signal will become synchronous with RCLK instead of TCLK.

FRAMER LOOPBACK

When CCR1.0 is set to a one, the DS21Q41B will enter a Framer LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS21Q41B will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. an unframed all one's code will be transmitted at TPOS and TNEG
2. data at RPOS and RNEG will be ignored
3. all receive side signals will take on timing synchronous with TCLK instead of RCLK.

CCR2: COMMON CONTROL REGISTER 2 (Address=38 Hex)

(MSB)				(LSB)			
TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL
SYMBOL	POSITION	NAME AND DESCRIPTION					
TFM	CCR2.7	Transmit Frame Mode Select. 0=D4 framing mode 1=ESF framing mode					
TB8ZS	CCR2.6	Transmit B8ZS Enable. 0=B8ZS disabled 1=B8ZS enabled					
TSLC96	CCR2.5	Transmit SLC-96/Fs Bit Insertion Enable. 0=SLC-96 disabled 1=SLC-96 enabled					
TFDL	CCR2.4	Transmit Zero Stuffer Enable. 0=zero stuffer disabled 1=zero stuffer enabled					
RFM	CCR2.3	Receive Frame Mode Select. 0=D4 framing mode 1=ESF framing mode					
RB8ZS	CCR2.2	Receive B8ZS Enable. 0=B8ZS disabled 1=B8ZS enabled					
RSLC96	CCR2.1	Receive SLC-96 Enable. 0=SLC-96 disabled 1=SLC-96 enabled					
RFDL	CCR2.0	Receive Zero Destuffer Enable. 0=zero destuffer disabled 1=zero destuffer enabled					

CCR3: COMMON CONTROL REGISTER 3 (Address=30 Hex)

(MSB)				(LSB)			
ESMDM	ESR	RLOS	RSMS	PDE	TLD	TLU	-
SYMBOL	POSITION	NAME AND DESCRIPTION					
ESMDM	CCR3.7	Elastic Store Minimum Delay Mode. See Section 10.3 for details. 0=elastic stores operate at full two frame depth 1=elastic stores operate at 32-bit depth					
ESR	CCR3.6	Elastic Store Reset. Setting this bit from a zero to a one will force the elastic stores to a known depth. Should be toggled after RSYCLK and TSYCLK have been applied and are stable. Must be cleared and set again for a subsequent reset.					
RLOS	CCR3.5	Function of the RLOS/LOTC Output. 0=Receive Loss of Sync (RLOS) 1=Loss of Transmit Clock (LOTC)					

RSMS	CCR3.4	RSYNC Multiframe Skip Control. Useful in framing format conversions from D4 to ESF. 0=RSYNC will output a pulse at every multiframe 1=RSYNC will output a pulse at every other multiframe note; for this bit to have any affect, the RSYNC must be set to output multiframe pulses (RCR2.4=1 and RCR2.3=0).
PDE	CCR3.3	Pulse Density Enforcer Enable. 0=disable transmit pulse density enforcer 1=enable transmit pulse density enforcer
TLU	CCR3.2	Transmit Loop Down Code (001). 0=transmit data normally 1=replace normal transmitted data with loop down code
TLU	CCR3.1	Transmit Loop Up Code (00001). 0=transmit data normally 1=replace normal transmitted data with loop up code
	CCR3.0	Not Assigned. Must be set to zero when written to.

LOOP CODE GENERATION

When either the CCR3.1 or CCR3.2 bits are set to one, the DS21Q41B will replace the normal transmitted payload with either the Loop Up or Loop Down code respectively. The DS21Q41B will overwrite the repeating loop code pattern with the framing bits. The SCT will continue to transmit the loop codes as long as either bit is set. It is an illegal state to have both CCR3.1 and CCR3.2 set to one at the same time.

PULSE DENSITY ENFORCER

The SCT always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403–1989: – no more than 15 consecutive zeros – at least N ones in each and every time window of $8 \times (N + 1)$ bits where N=1 through 23

Violations for the transmit and receive data streams are reported in the RIR2.2 and RIR2.1 bits respectively.

When the CCR3.3 is set to one, the DS21Q41B will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to zero since B8ZS encoded data streams cannot violate the pulse density requirements.

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS21Q41B should be configured for operation by writing to all of the internal registers (this includes setting

the Test Registers to 00Hex) since the contents of the internal registers cannot be predicted on power-up. Finally, after the TSYCLK and RSYCLK inputs are stable, the ESR bit should be toggled from a zero to a one (this step can be skipped if the elastic stores are disabled).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS21Q41B, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register 1 (RIR1), and Receive Information Register 2 (RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS21Q41B which bits the user wishes to read and have cleared. The user will write a byte to one of these four registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When

a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. The write-read-write scheme is unique to the four status registers and it allows an external microcontroller or microprocessor to individually poll certain bits

without disturbing the other bits in the register. This operation is key in controlling the DS21Q41B with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the INT output pin. All four framers within the DS21Q41B share the INT output. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively. The user can determine which framer has active interrupts by polling the Interrupt Status Register (ISR).

ISR: INTERRUPT STATUS REGISTER (any unused address)

(MSB)				(LSB)			
F32AR2	F3SR1	F2SR2	F2SR1	F1SR2	F1SR1	F0SR2	F0SR1
SYMBOL	POSITION	NAME AND DESCRIPTION					
F3SR2	ISR.7	Status of Interrupt for SR2 in Framer 3. 1=interrupt active.					
F3SR1	ISR.6	Status of Interrupt for SR1 in Framer 3. 1=interrupt active.					
F2SR2	ISR.5	Status of Interrupt for SR2 in Framer 2. 1=interrupt active.					
F2SR1	ISR.4	Status of Interrupt for SR1 in Framer 2. 1=interrupt active.					
F1SR2	ISR.3	Status of Interrupt for SR2 in Framer 1. 1=interrupt active.					
F1SR1	ISR.2	Status of Interrupt for SR1 in Framer 1. 1=interrupt active.					
F0SR2	ISR.1	Status of Interrupt for SR2 in Framer 0. 1=interrupt active.					
F0SR1	ISR.0	Status of Interrupt for SR1 in Framer 0. 1=interrupt active.					

RIR1: RECEIVE INFORMATION REGISTER 1 (Address=22 Hex)

(MSB)				(LSB)			
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE

SYMBOL	POSITION	NAME AND DESCRIPTION
COFA	RIR1.7	Change of Frame Alignment. Set when the last resync resulted in a change of frame or multiframe alignment.
8ZD	RIR1.6	Eight Zero Detect. Set when a string of at least eight consecutive zeros (regardless of the length of the string) have been received at RPOS and RNEG.
16ZD	RIR1.5	Sixteen Zero Detect. Set when a string of at least sixteen consecutive zeros (regardless of the length of the string) have been received at RPOS and RNEG.
RESF	RIR1.4	Receive Elastic Store Full. Set when the receive elastic store buffer fills and a frame is deleted.
RESE	RIR1.3	Receive Elastic Store Empty. Set when the receive elastic store buffer empties and a frame is repeated.
SEFE	RIR1.2	Severely Errored Framing Event. Set when 2 out of 6 framing bits (Ft or FPS) are received in error.
B8ZS	RIR1.1	B8ZS Code Word Detect. Set when a B8ZS code word is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.6. Useful for automatically setting the line coding.
FBE	RIR1.0	Frame Bit Error. Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

RIR2: RECEIVE INFORMATION REGISTER 2 (Address=31 Hex)

(MSB)				(LSB)			
RLOSC	RCLC	TESF	TESE	TSLIP	RBLC	RPDV	TPDV

SYMBOL	POSITION	NAME AND DESCRIPTION
RLOSC	RIR2.7	Receive Loss of Sync Clear. Set when the framer achieves synchronization; will remain set until read.
RCLC	RIR2.6	Receive Carrier Loss Clear. Set when the carrier signal is restored; will remain set until read.
TESF	RIR2.5	Transmit Elastic Store Full. Set when the transmit elastic store buffer fills and a frame is deleted.
TESE	RIR2.4	Transmit Elastic Store Empty. Set when the transmit elastic store buffer empties and a frame is repeated.
TSLIP	RIR2.3	Transmit Elastic Store Slip Occurance. Set when the transmit elastic store has either repeated or deleted a frame.
RBLC	RIR2.2	Receive Blue Alarm Clear. Set when the Blue Alarm (AIS) is no longer detected; will remain set until read.

RPDV RIR2.1

Receive Pulse Density Violation. Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.

TPDV RIR2.0

Transmit Pulse Density Violation. Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

SR1: STATUS REGISTER 1 (Address=20 Hex)

(MSB)

(LSB)

LUP	LDN	LOT	RSLIP	RBL	RYEL	RCL	RLOS
-----	-----	-----	-------	-----	------	-----	------

SYMBOL

POSITION

NAME AND DESCRIPTION

LUP

SR1.7

Loop Up Code Detected. Set when the repeating ...00001... loop up code is being received.

LDN

SR1.6

Loop Down Code Detected. Set when the repeating ...001... loop down code is being received.

LOT

SR1.5

Loss of Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 5.2 μ s). Will force the RLOS/LOT pin high if enabled via CCR1.6. Also will force transmit side formatter to switch to RCLK if so enabled via TCR1.7. Based on RCLK.

RSLIP

SR1.4

Receive Elastic Store Slip Occurance. Set when the receive elastic store has either repeated or deleted a frame.

RBL

SR1.3

Receive Blue Alarm. Set when an unframed all one's code is received at RPOS and RNEG.

RYEL

SR1.2

Receive Yellow Alarm. Set when a yellow alarm is received at RPOS and RNEG.

RCL

SR1.1

Receive Carrier Loss. Set when 192 consecutive zeros have been detected at RPOS and RNEG.

RLOS

SR1.0

Receive Loss of Sync. Set when the device is not synchronized to the receive T1 stream.

DS21Q41B ALARM SET & CLEAR CRITERIA Table 4-2

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (see note 1 below)	when over a 3 ms window, five or less zeros are received	when over a 3 ms window, six or more zeros are received
Yellow Alarm (RAI) 1. D4 bit 2 mode (RCR2.2=0) 2. D4 12th F-bit mode (RCR2.2=1; this mode is also referred to as the "Japanese Yellow Alarm") 3. ESF mode	when bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences when the 12th framing bit is set to one for two consecutive occurrences. when 16 consecutive patterns of 00FF appear in the FDL	when bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences when the 12th framing bit is set to zero for two consecutive occurrences when 14 or less patterns of 00FF hex out of 16 possible appear in the FDL
Red Alarm (RCL) (this alarm is also referred to as Loss of Signal)	when 192 consecutive zeros are received	when 14 or more ones out of 112 possible bit positions are received starting with the first one received

NOTES:

- The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all ones signal. Blue alarm detectors should be able to operate properly in the presence of a 10⁻³ error rate and they should not falsely trigger on a framed all ones signal. The blue alarm criteria in the DS21Q41B has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS bit.
- ANSI specifications use a different nomenclature than the DS21Q41B does; the following terms are equivalent:

RBL=AIS
RCL=LOS
RLOS=LOF
RYEL=RAI

LOOP UP/DOWN CODE DETECTION

Bits SR1.7 and SR1.6 will indicate when either the standard "loop up" or "loop down" codes are being received by the DS21Q41B. When a loop up code has been received for 5 seconds, the CPE is expected to loop the recovered data (without correcting BPVs) back to the source. The loop down code indicates that the loopback should be discontinued. See the AT&T publication TR 62411 for more details. The DS21Q41B will detect the

loop up/down codes in both framed and unframed circumstances with bit error rates as high as 10⁻². The loop code detector has a nominal integration period of 48 ms. Hence, after about 48 ms of receiving either code, the proper status bit will be set to a one. After this initial indication, it is recommended that the software poll the DS21Q41B every 100 ms to 500 ms until 5 seconds has elapsed to insure that the code is continuously present.

SR2: STATUS REGISTER 2 (Address=21 Hex)

(MSB)						(LSB)		
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	LORC	
SYMBOL	POSITION	NAME AND DESCRIPTION						
RMF	SR2.7	Receive Multiframe. Set on receive multiframe boundaries.						
TMF	SR2.6	Transmit Multiframe. Set on transmit multiframe boundaries.						
SEC	SR2.5	One Second Timer. Set on increments of one second based on RCLK; will be set in increments of 999 ms, 999 ms, and 1002 ms every 3 seconds.						
RFDL	SR2.4	Receive FDL Buffer Full. Set when the receive FDL buffer (RFDL) fills to capacity (8-bits).						
TFDL	SR2.3	Transmit FDL Buffer Empty. Set when the transmit FDL buffer (TFDL) empties.						
RMTCH	SR2.2	Receive FDL Match Occurance. Set when the RFDL matches either RFDLM1 or RFDLM2.						
RAF	SR2.1	Receive FDL Abort. Set when eight consecutive one's are received in the FDL.						
LORC	SR2.0	Loss of Receive Clock. Set when the RCLK pin has not transitioned for at least 2 μ s (3 μ s \pm 1 μ s)						

IMR1: INTERRUPT MASK REGISTER 1 (Address=7F Hex)

(MSB)						(LSB)		
LUP	LDN	LOT	SLIP	RBL	RYEL	RCL	RLOS	
SYMBOL	POSITION	NAME AND DESCRIPTION						
LUP	IMR1.7	Loop Up Code Detected. 0=interrupt masked 1=interrupt enabled						
LDN	IMR1.6	Loop Down Code Detected. 0=interrupt masked 1=interrupt enabled						
LOT	IMR1.5	Loss of Transmit Clock. 0=interrupt masked 1=interrupt enabled						
SLIP	IMR1.4	Elastic Store Slip Occurance. 0=interrupt masked 1=interrupt enabled						
RBL	IMR1.3	Receive Blue Alarm. 0=interrupt masked 1=interrupt enabled						
RYEL	IMR1.2	Receive Yellow Alarm. 0=interrupt masked 1=interrupt enabled						

IMR1.1 Receive Carrier Loss.
 0=interrupt masked
 1=interrupt enabled

IMR1.0 Receive Loss of Sync.
 0=interrupt masked
 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=6F Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	LORC
SYMBOL		POSITION	NAME AND DESCRIPTION				
RMF		IMR2.7	Receive Multiframe. 0=interrupt masked 1=interrupt enabled				
TMF		IMR2.6	Transmit Multiframe. 0=interrupt masked 1=interrupt enabled				
SEC		IMR2.5	One Second Timer. 0=interrupt masked 1=interrupt enabled				
RFDL		IMR2.4	Receive FDL Buffer Full. 0=interrupt masked 1=interrupt enabled				
TFDL		IMR2.3	Transmit FDL Buffer Empty. 0=interrupt masked 1=interrupt enabled				
RMTCH		IMR2.2	Receive FDL Match Occurance. 0=interrupt masked 1=interrupt enabled				
RAF		IMR2.1	Receive FDL Abort. 0=interrupt masked 1=interrupt enabled				
LORC		IMR2.0	Loss of Receive Clock. 0=interrupt masked 1=interrupt enabled				

5.0 ERROR COUNT REGISTERS

There are a set of three counters in the DS21Q41B that record bipolar violations, excessive zeros, errors in the CRC6 code words, framing bit errors, and number of multiframe that the device is out of receive synchronization. Each of these three counters are automatically updated on one second boundaries as determined by the one second timer in Status Register 2 (SR2.5). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the one second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost. All three counters will saturate at their respective maximum counts and they

will not rollover (note: only the Line Code Violation Count Register has the potential to overflow).

5.1 Line Code Violation Count Register (LCVCR)

Line Code Violation Count Register 1 High (LCVCR1) is the most significant word and LCVCR2 is the least significant word of a 16-bit counter that records code violations (CVs). CVs are defined as Bipolar Violations (BPVs) or excessive zeros. See Table 5-1 for details of exactly what the LCVCRs count. If the B8ZS mode is set for the receive side via CCR2.2, then B8ZS code words are not counted. This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS=1) conditions.

LCVCR1: LINE CODE VIOLATION COUNT REGISTER 1 (Address=23 Hex)

LCVCR2: LINE CODE VIOLATION COUNT REGISTER 2 (Address=24 Hex)

(MSB)				(LSB)				
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	LCVCR1
LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	LCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CV16	LCVCR1.7	MSB of the 16-Bit code violation count
CV0	LCVCR2.0	LSB of the 16-Bit code violation count

LINE CODE VIOLATION COUNTING ARRANGEMENTS Table 5-1

COUNT EXCESSIVE ZEROS? (RCR1.7)	B8ZS ENABLED? (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs
no	no	BPVs
yes	no	BPVs + 16 consecutive zeros
no	yes	BPVs (B8ZS code words not counted)
yes	yes	BPVs + 8 consecutive zeros

5.2 Path Code Violation Count Register (PCVCR)

When the receive side of the DS21Q41B is set to operate in the ESF framing mode (CCR2.3=1), PCVCR will automatically be set as a 12-bit counter that will record errors in the CRC6 code words. When set to operate in the D4 framing mode (CCR2.3=0), PCVCR will auto-

matically count errors in the Ft framing bit position. Via the RCR2.1 bit, the DS21Q41B can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5-2 for a detailed description of exactly what errors the PCVCR counts.

PCVCR1: PATH VIOLATION COUNT REGISTER 1 (Address=25 Hex)**PCVCR2: PATH VIOLATION COUNT REGISTER 2** (Address=26 Hex)

(MSB)	(MSB)						(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	CRC/FB11	CRC/FB10	CRC/FB9	CRC/FB8	PCVCR1
CRC/FB7	CRC/FB6	CRC/FB5	CRC/FB4	CRC/FB3	CRC/FB2	CRC/FB1	CRC/FB0	PCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC/FB11	PCVCR1.3	MSB of the 12–Bit CRC6 Error or Frame Bit Error Count (note 2)
CRC/FB0	PCVCR2.0	LSB of the 12–Bit CRC6 Error or Frame Bit Error Count (note 2)

NOTES:

1. The upper nibble of the counter at address 25 is used by the Multiframe Out of Sync Count Register.
2. PCVCR counts either errors in CRC code words (in the ESF framing mode; CCR2.3=1) or errors in the framing bit position (in the D4 framing mode; CCR2.3=0).

PATH CODE VIOLATION COUNTING ARRANGEMENTS Table 5–2

FRAMING MODE (CCR2.3)	COUNT FS ERRORS? (RCR2.1)	WHAT IS COUNTED IN THE PCVCRs
D4	no	errors in the Ft pattern
D4	yes	errors in both the Ft and Fs patterns
ESF	don't care	errors in the CRC6 code words

5.3 Multiframe Out of Sync Count Register (MOSCR)

Normally the MOSCR is used to count the number of multiframe that the receive synchronizer is out of sync (RCR2.0=1). This number is useful in ESF applications needing to measure the parameters Loss Of Frame Count (LOFC) and ESF Error Events as described in AT&T publication TR54016. When the MOSCR is operated in this mode, it is not disabled during receive loss of

synchronization (RLOS=1) conditions. The MOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the MOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5–3 for a detailed description of what the MOSCR is capable of counting.

MOSCR1: MULTIFRAMES OUT OF SYNC COUNT REGISTER 1 (Address=25 Hex)**MOSCR2: MULTIFRAMES OUT OF SYNC COUNT REGISTER 2** (Address=27 Hex)

(MSB)				(LSB)				
MOS/FB11	MOS/FB10	MOS/FB9	MOS/FB8	(note 1)	(note 1)	(note 1)	(note 1)	MOSCR1
MOS/FB7	MOS/FB6	MOS/FB5	MOS/FB4	MOS/FB3	MOS/FB2	MOS/FB1	MOS/FB0	MOSCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
MOS/FB11	MOSCR1.7	MSB of the 12-Bit Multiframe Out of Sync or F-Bit Error Count (note 2)
MOS/FB0	MOSCR2.0	LSB of the 12-Bit Multiframe Out of Sync or F-Bit Error Count (note 2)

NOTES:

1. The lower nibble of the counter at address 25 is used by the Path Code Violation Count Register.
2. MOSCR counts either errors in framing bit position (RCR2.0=0) or the number of multiframe out of sync (RCR2.0=1)

MULTIFRAMES OUT OF SYNC COUNTING ARRANGEMENTS Table 5-3

FRAMING MODE (CCR2.3)	COUNT MOS OR F-BIT ERRORS? (RCR2.0)	WHAT IS COUNTED IN THE MOSCRs
D4	MOS	number of multiframe out of sync
D4	F-BIT	errors in the Ft pattern
ESF	MOS	number of multiframe out of sync
ESF	F-BIT	errors in the FPS pattern

6.0 FDL/Fs EXTRACTION AND INSERTION

The DS21Q41B has the ability to extract/insert data from/into the Facility Data Link (FDL) in the ESF framing mode and from/into Fs bit position in the D4 framing mode. Since SLC-96 utilizes the Fs bit position, this capability can also be used in SLC-96 applications. The operation of the receive and transmit sections will be discussed separately. Contact the factory for a copy of C language source code for implementing the FDL on the DS21Q41B.

6.1 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2 ms (8 times 250 μ s). The DS21Q41B will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the $\overline{\text{INT}}$ pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2 ms to read this data before it is lost. If the byte in the RFDL matches either of the

bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR2.2 bit will be set to a one and the $\overline{\text{INT}}$ pin will toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The DS21Q41B also contains a zero destuffer which is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than 5 ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.0, the DS21Q41B will automatically look for 5 ones in a row, followed by a zero. If it finds such a pattern, it will automatically remove the zero. If the zero destuffer sees six or more ones in a row followed by a zero, the zero is not removed. The CCR2.0 bit should always be set to a one when the DS21Q41B is extracting the FDL. More on how to use the DS21Q41B in FDL applications is covered in a separate Application Note.

RFDL: RECEIVE FDL REGISTER (Address=28 Hex)

(MSB)				(LSB)			
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the Received FDL Code
RFDL0	RFDL.0	LSB of the Received FDL Code

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RFDLM1: RECEIVE FDL MATCH REGISTER 1 (Address=29 Hex)**RFDLM2: RECEIVE FDL MATCH REGISTER 2** (Address=2A Hex)

(MSB)				(LSB)			
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the FDL Match Code
RFDL0	RFDL.0	LSB of the FDL Match Code

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RFDLM1/RFDLM2), RSR2.2 will be set to a one and the $\overline{\text{INT}}$ will go active if enabled via IMR2.2.

6.2 Transmit Section

The transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full eight bits has been shifted out, the DS21Q41B will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to a one. The $\overline{\text{INT}}$ will also toggle low if enabled via IMR2.3. The user has 2 ms (1.5 ms in SLC-96 applications) to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again.

The DS21Q41B also contains a zero stuffer which is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the DS21Q41B will automatically look for 5 ones in a row.

If it finds such a pattern, it will automatically insert a zero after the five ones. The CCR2.0 bit should always be set to a one when the DS21Q41B is inserting the FDL. More on how to use the DS21Q41B in FDL applications is covered in a separate Application Note.

TFDL: TRANSMIT FDL REGISTER (Address=7E Hex)

(MSB)				(LSB)			
TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
TFDL7	TFDL.7	MSB of the FDL code to be transmitted
TFDL0	TFDL.0	LSB of the FDL code to be transmitted

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first.

7.0 SIGNALING OPERATION

The robbed bit signaling bits in embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS21Q41B. There is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The

CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to zero, then the robbed signaling bits will appear at RSER in their proper position as they are received. If CCR1.5 is set to a one, then the robbed signaling bit positions will be forced to a one at RSER.

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (Address=60 to 6B Hex)

(MSB)								(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)	
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)	
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)	
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)	
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)	
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)	
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	RS7 (66)	
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	RS8 (67)	
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	RS9 (68)	
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	RS10 (69)	
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	RS11 (6A)	
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	RS12 (6B)	

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	RS12.7	Signaling Bit D in Channel 24
A(1)	RS1.0	Signaling Bit A in Channel 1

Each Receive Signaling Register (RS1 to RS12) reports the incoming robbed bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two framing bits per channel (A and B). In the D4 framing mode, the DS21Q41B will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the DS21Q41B is operated in either

framing mode, the user needs only to retrieve the signaling bits every 3 ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0=1). They will contain the most recent signaling information before the "OOF" occurred.

TS1 TO TS12: TRANSMIT SIGNALING REGISTERS (Address=70 to 7B Hex)

(MSB)				(LSB)				
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	TS1 (70)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	TS2 (71)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	TS3 (72)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	TS4 (73)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	TS5 (74)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	TS6 (75)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	TS7 (76)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	TS8 (77)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	TS9 (78)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	TS10 (79)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	TS11 (7A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	TS12 (7B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	Signaling Bit A in Channel 24
A(1)	TS1.0	Signaling Bit D in Channel 1

Each Transmit Signaling Register (TS1 to TS12) contains the Robbed Bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). On multiframe boundaries, the DS21Q41B will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits. In the ESF framing mode, the interrupt will come every 3 ms and the user has a full 3 ms to update the TSR's. In the D4 framing mode, there are only two framing bits per channel (A and B). However in the D4 framing mode, the DS21Q41B uses the C

and D bit positions as the A and B bit positions for the next multi frame. The DS21Q41B will load the values in the TSRs into the outgoing shift register every other D4 multiframe.

8.0 SPECIAL TRANSMIT SIDE REGISTERS

There is a set of seven registers in the DS21Q41B that can be used to custom tailor the data that is to be transmitted onto the T1 line, on a channel by channel basis. Each of the 24 T1 channels can be either forced to be transparent or to have a user defined idle code inserted into them. Each of these special registers is defined below.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTERS (Address=39 to 3B Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (29)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	Transmit Transparency Registers. 0=this DS0 channel is not transparent 1=this DS0 channel is transparent
CH1	TTR1.0	

Each of the bit positions in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel is transparent (or clear). If a DS 0 is programmed to be clear, no robbed bit signaling will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, bit 2 will be overwritten by a zero when a Yellow Alarm is transmitted. Also the user has the option to prevent the TTR registers from determining which channels are to have Bit 7 stuffing performed. If the TCR2.0 and TCR1.3 bits are set to one, then all 24 T1 channels will have Bit 7 stuffing performed on them regardless of how the TTR registers are programmed. In this manner, the TTR registers are only affecting which channels are to have robbed bit signaling inserted into them. Please see Figure 13–9 for more details.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address=3C to 3E Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	Transmit Idle Registers. 0=do not insert the Idle Code into this DS0 channel 1=insert the Idle Code into this channel
CH1	TIR1.0	

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=3F Hex)

(MSB)				(LSB)			
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code
TIDR0	TIDR.0	LSB of the Idle Code

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel

Blocking Registers (TCBR1/TCBR2/TCBR3) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in Fractional T1 or ISDN-PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 12 for an example.

RCBR1/RCBR2/RCBR3: RECEIVE CHANNEL BLOCKING REGISTERS (Address=6C to 6E Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RCBR3.7	Receive Channel Blocking Registers. 0=force the RCHBLK pin to remain low during this channel time 1=force the RCHBLK pin high during this channel time
CH1	RCBR1.0	

TCBR1/TCBR2/TCBR3: TRANSMIT CHANNEL BLOCKING REGISTERS (Address=32 to 34 Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (34)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TCBR3.7	Transmit Channel Blocking Registers. 0=force the TCHBLK pin to remain low during this channel time 1=force the TCHBLK pin high during this channel time
CH1	TCBR1.0	

10.0 ELASTIC STORES OPERATION

Each framer within the DS21Q41B contains dual two-frame (386 bits) elastic stores, one for the receive direction, and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the T1 data stream to 2.048Mbps (or a multiple of 2.048Mbps) which is the E1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e. not frequency locked) backplane clock (which can be 1.544 MHz or 2.048 MHz). Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The receive side elastic store can be enabled via CCR1.2 and the transmit side elastic store is enabled via CCR1.7. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.6). Toggling the CCR3.6 bit forces the read and write pointers into opposite frames. Both elastic stores within the DS21Q41B are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544 MHz or 2.048 MHz backplane without regard to the backplane rate the other elastic store is interfacing to.

10.1 Receive Side

If the receive side elastic store is enabled (CCR1.2=1), then the user must provide either a 1.544 MHz (CCR1.3=0) or 2.048 MHz (CCR1.3=1) clock at the RSYCLK pin. The user has the option of either providing a frame sync at the RSYNC pin (RCR2.3=1) or having the RSYNC pin provide a pulse on frame boundaries (RCR2.3=0). If the user wishes to obtain pulses at the frame boundary, then RCR2.4 must be set to zero and if the user wishes to have pulses occur at the multi-frame boundary, then RCR2.4 must be set to one. The DS21Q41B will always indicate frame boundaries via the RFSYNC output whether the elastic store is enabled or not. If the elastic store is enabled, then multi-frame boundaries will be indicated via the RMSYNC output. If the user selects to apply a 2.048 MHz clock to the SYSCLK pin, then the data output at RSER will be forced to all ones every fourth channel and the F-bit will be deleted. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be forced to a one. Also, in 2.048 MHz applications, the RCHBLK output will be forced high during the same channels as the RSER pin. See Section 12 for more details. This is useful in T1 to CEPT (E1) conversion applications. If the

386-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (193 bits) will be repeated at RSER and the SR1.4 and RIR1.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR1.4 bits will be set to a one.

10.2 Transmit Side

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR1.7. A 1.544 MHz (CCR1.4=0) or 2.048 MHz (CCR1.4=1) clock can be applied to the TSYSCLK input. If the user selects to apply a 2.048 MHz clock to the TSYSCLK pin, then the data output at TSER will be ignored every fourth channel. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be ignored. The user must supply a 8 KHz frame sync pulse to the TFSYNC input. Also, in 2.048 MHz applications, the TCHBLK output will be forced high during the channels ignored by the DS21Q41B. See Section 12 for more details. Controlled slips in the transmit elastic store are reported in the RIR2.3 bit and the direction of the slip is reported in the RIR2.3 and RIR2.4 bits.

10.3 Minimum Delay Synchronous SYSCLK Mode

In applications where the DS21Q41B is connected to backplanes that are frequency locked to the recovered T1 clock (i.e. the RCLK output), the full two frame depth of the onboard elastic stores is really not needed. In fact, in some delay sensitive applications, the normal two frame depth may be excessive. If the CCR3.7 bit is set to one, then the receive elastic store (and also the transmit elastic store if it is enabled) will be forced to a maximum depth of 32 bits instead of the normal 386 bits. In this mode, RSYCLK and TSYSCLK must be tied together and they must be frequency locked to RCLK. All of the slip contention logic in the DS21Q41B is disabled (since slips cannot occur). Also, since the buffer depth is no longer two frames deep, the DS21Q41B must be set up to source either a frame pulse at the RSYNC pin and this output must be tied to the TFSYNC input. On power-up after the RSYCLK and TSYSCLK signals have locked to the RCLK signal, the elastic store reset bit (CCR3.6) should be toggled from a zero to a one to insure proper operation.

11.0 RECEIVE MARK REGISTERS

The DS21Q41B has the ability to replace the incoming data, on a channel-by-channel basis with either an idle code (7F Hex) or the digital milliwatt code which is a eight byte repeating pattern that represents a 1 KHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). The RCR2.7

bit will determine which code is used. Each bit in the RMRs, represents a particular channel. If a bit is set to a one, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to zero, no replacement occurs.

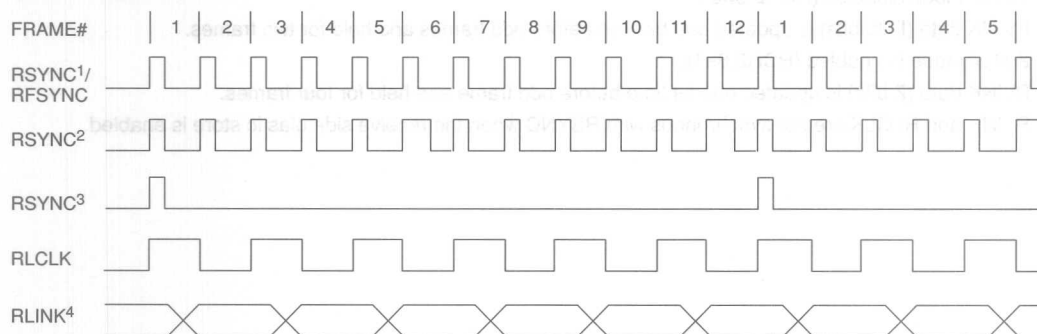
RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (Address=2D to 2F Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1 (2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2 (2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3 (2F)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RCBR3.7	Receive Channel Blocking Registers. 0=do not affect the receive data associated with this channel 1=replace the receive data associated with this channel with either the idle code or the digital milliwatt code (depends on the RCR2.7 bit)
CH1	RCBR1.0	

12.0 TIMING DIAGRAMS

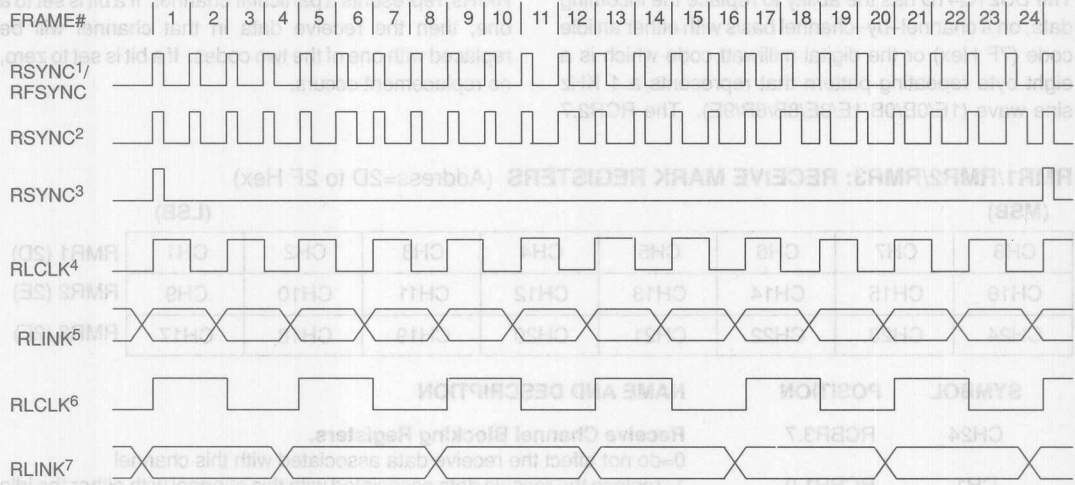
RECEIVE SIDE D4 TIMING Figure 12-1



NOTES:

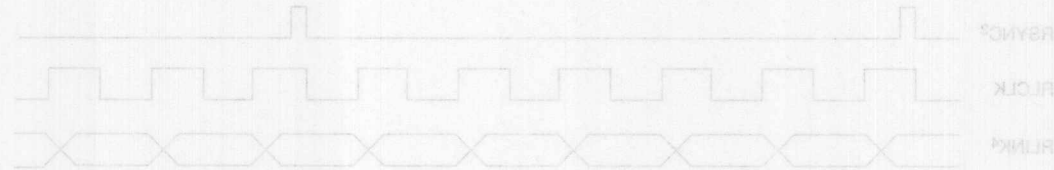
1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. RLINK data (S-bit) is updated one bit prior to even frames and held for two frames.
5. RLINK and RLCLK are not synchronous with RSYNC when the receive side elastic store is enabled.

RECEIVE SIDE ESF TIMING Figure 12-2



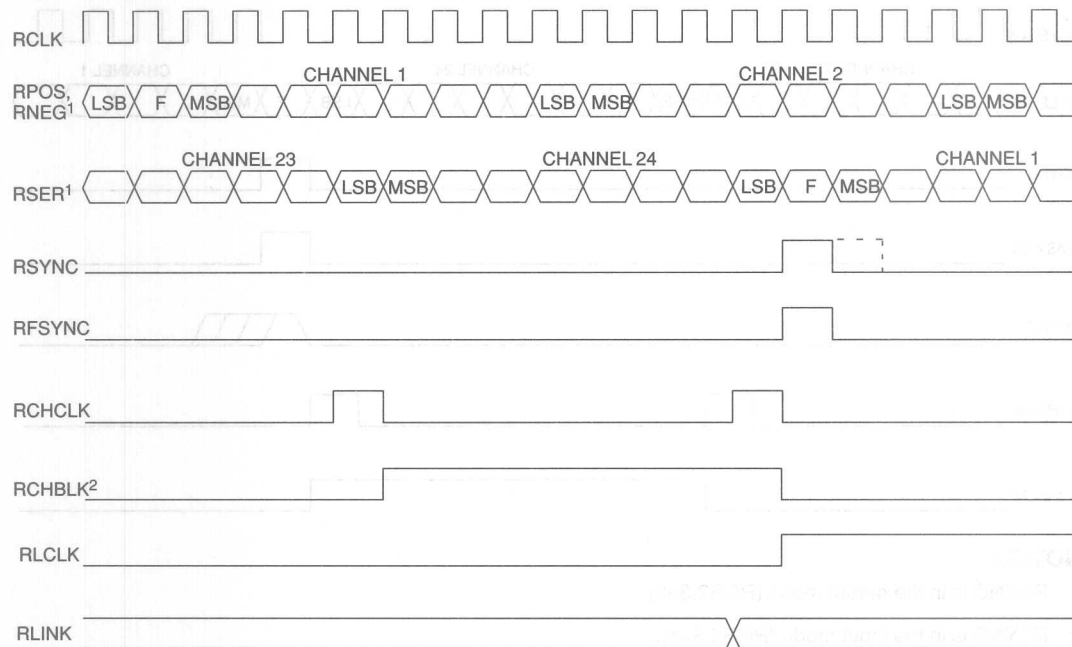
NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. ZBTSI mode disabled (RCR2.6=0).
5. RLINK data (FDL bits) is updated one bit time before odd frames and held for two frames.
6. ZBTSI mode is enabled (RCR2.6=1).
7. RLINK data (Z bits) is updated one bit time before odd frame and held for four frames.
8. RLINK and RLCLK are not synchronous with RSYNC when the receive side elastic store is enabled.

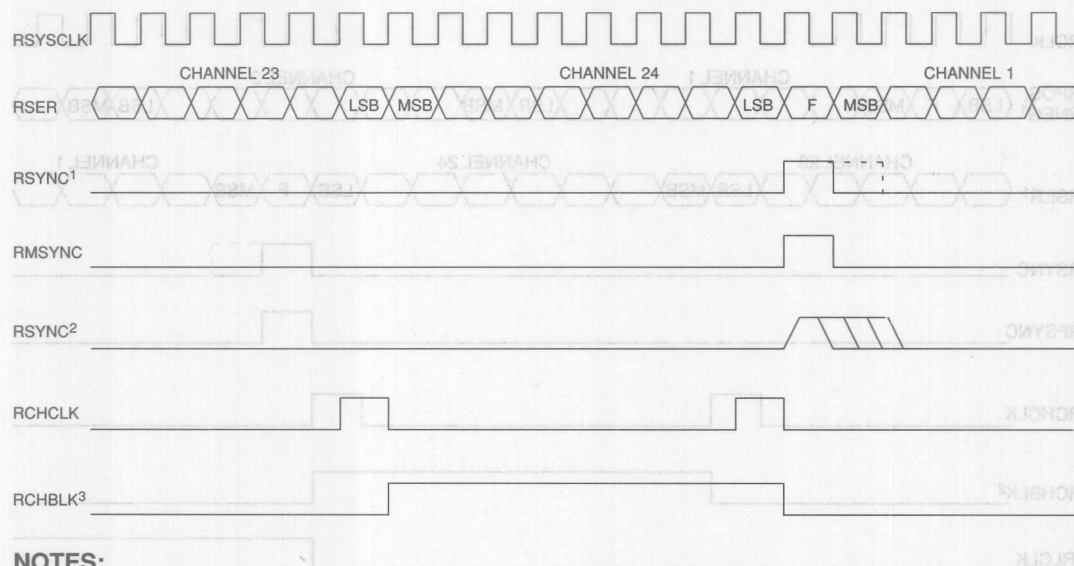


NOTES:

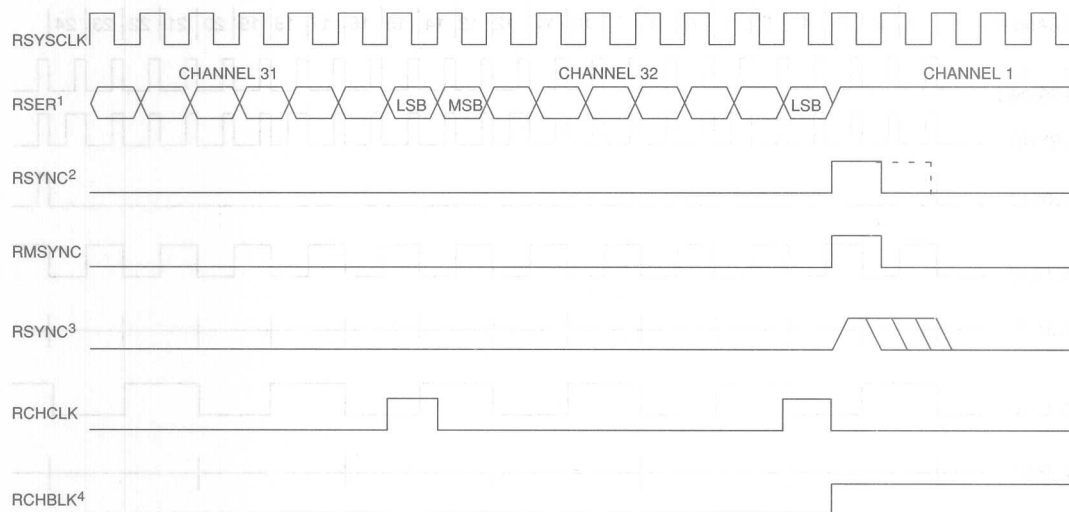
1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. RLINK data (S-bit) is updated one bit prior to even frames and held for two frames.
5. RLINK and RLCLK are not synchronous with RSYNC when the receive side elastic store is enabled.

RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED) Figure 12–3**NOTES:**

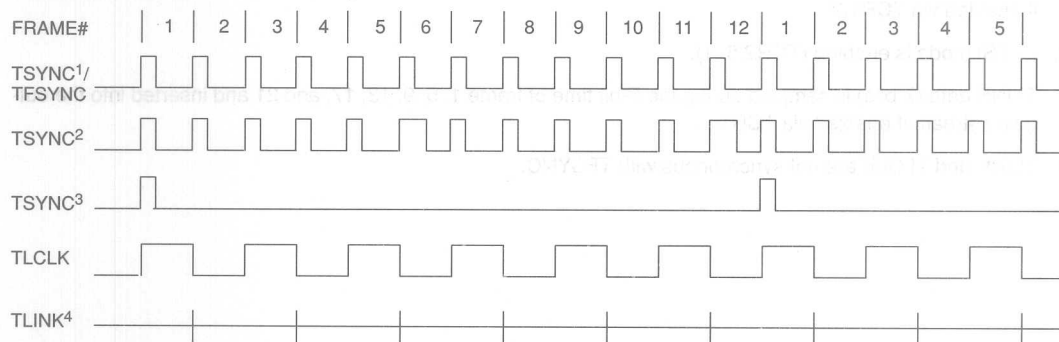
1. There is a 13 RCLK delay from RPOS/RNEG to RSER.
2. RCHBLK is programmed to block channel 24.

RECEIVE SIDE 1.544 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 12-4**NOTES:**

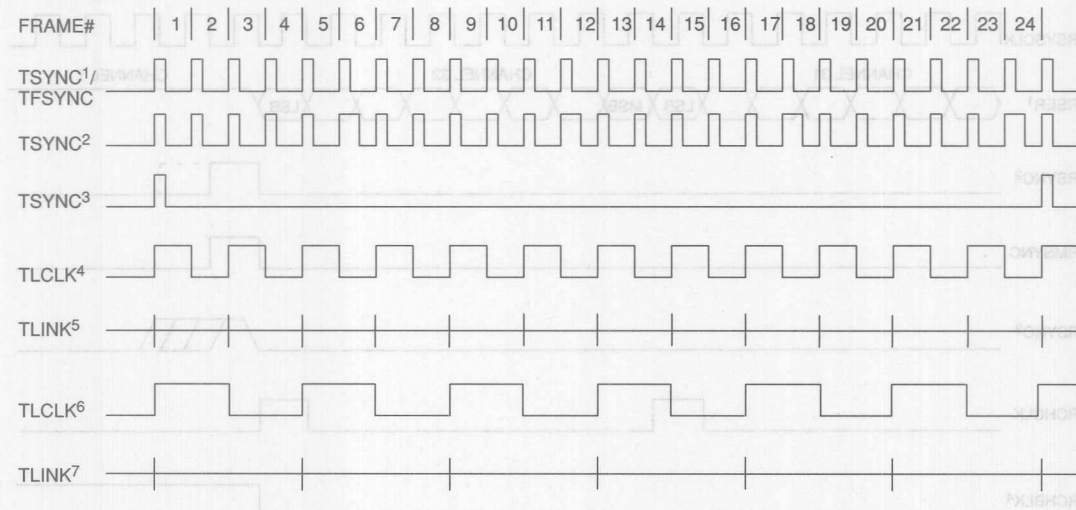
1. RSYNC is in the output mode (RCR2.3=0).
2. RSYNC is in the input mode (RCR2.3=1).
3. RCHBLK is programmed to block channel 24.

RECEIVE SIDE 2.048 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 12–5**NOTES:**

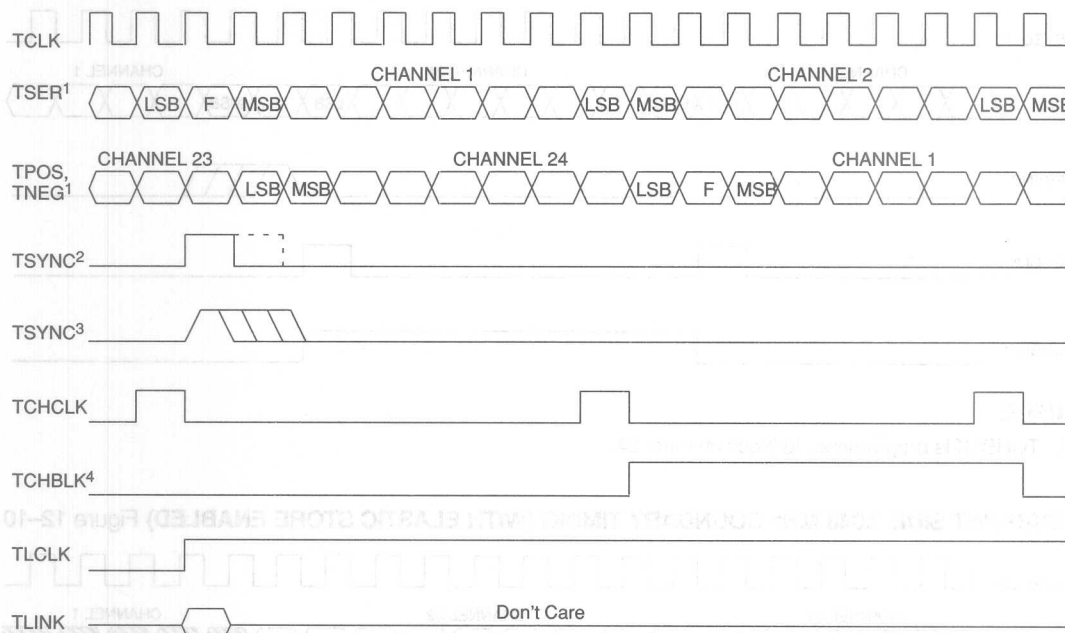
1. RSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 are forced to 1.
2. RSYNC is in the output mode (RCR2.3=0).
3. RSYNC is in the input mode (RCR2.3=1).
4. RCHBLK is forced to 1 in the same channels as RSER (see Note 1).

TRANSMIT SIDE D4 TIMING Figure 12–6**NOTES:**

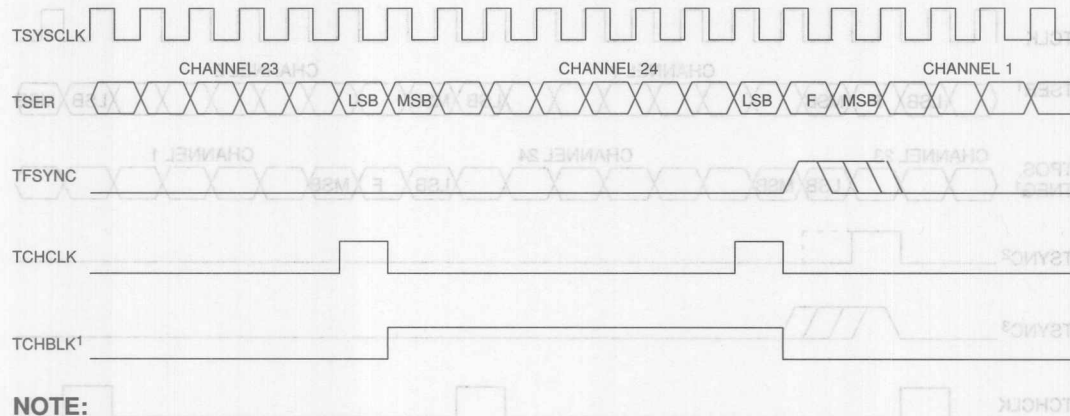
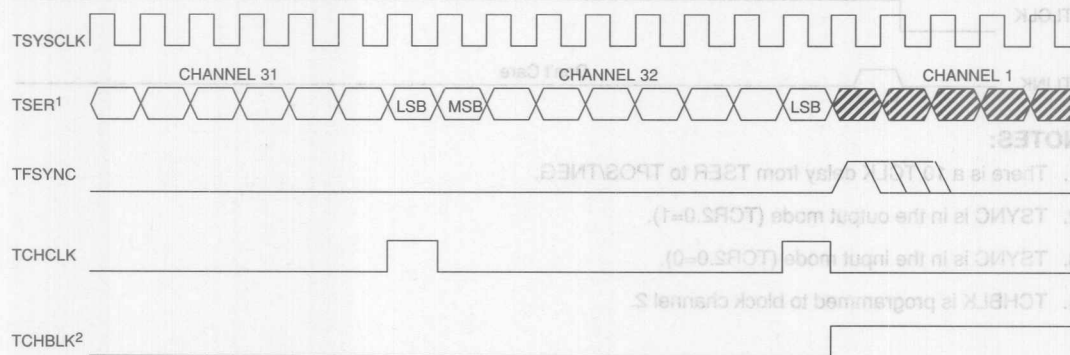
1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.3=1).
4. TLINK data (S-bit) is sampled during the F-bit position of even frames for insertion into the outgoing T1 stream when enabled via TCR1.2.
5. TLINK and TLCLK are not synchronous with TFSYNC.

TRANSMIT SIDE ESF TIMING Figure 12-7**NOTES:**

1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.4=1).
4. ZBTSI mode disabled (TCR2.5=0).
5. TLINK data (FDL bits) is sampled during the F-bit time of odd frame and inserted into the outgoing T1 stream if enabled via TCR1.2.
6. ZBTSI mode is enabled (TCR2.5=1).
7. TLINK data (Z bits) is sampled during the F-bit time of frame 1, 5, 9, 13, 17, and 21 and inserted into the outgoing stream if enabled via TCR1.2.
8. TLINK and TLCLK are not synchronous with TFSYNC.

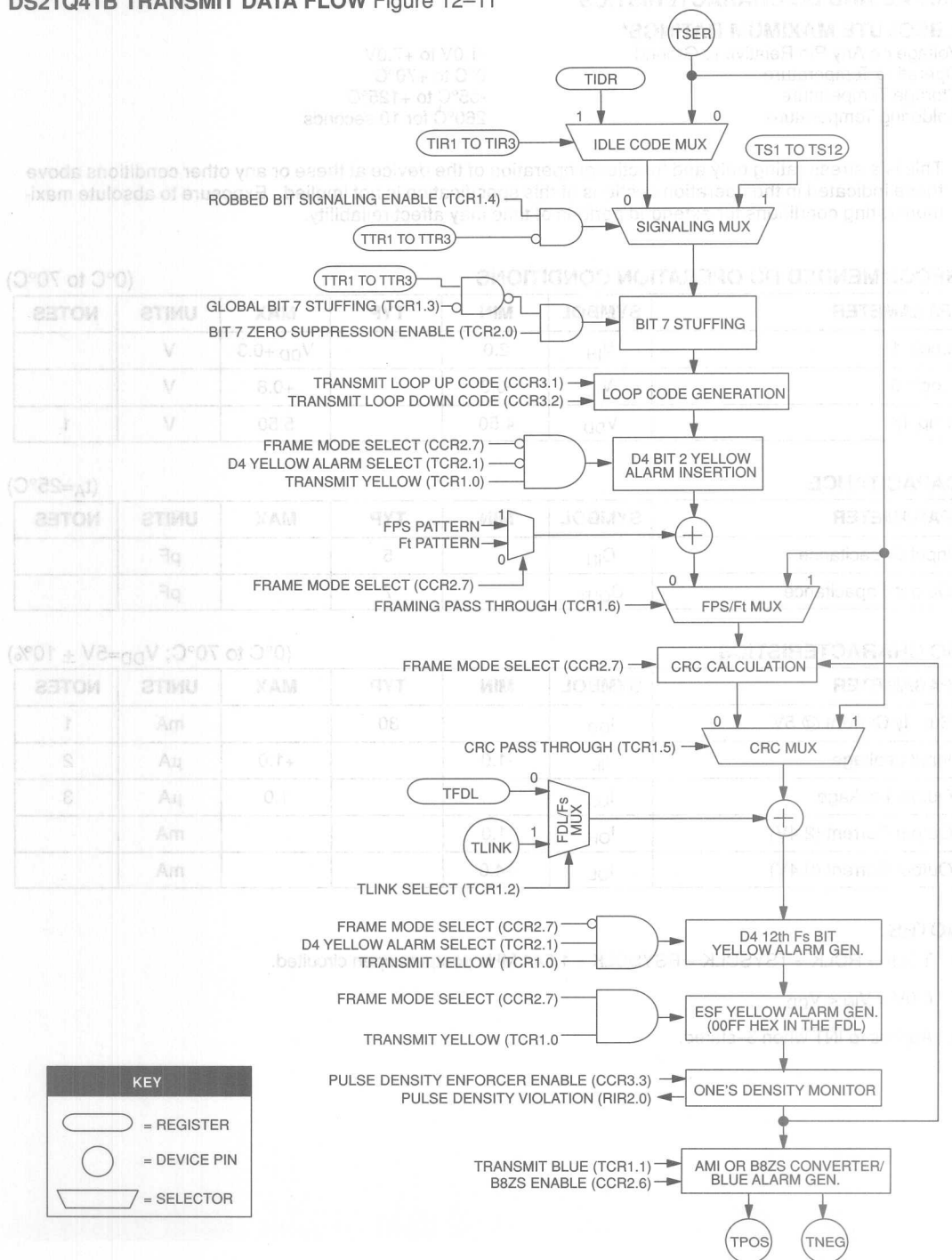
TRANSMIT SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED) Figure 12-8**NOTES:**

1. There is a 10 TCLK delay from TSER to TPOS/TNEG.
2. TSYNC is in the output mode (TCR2.0=1).
3. TSYNC is in the input mode (TCR2.0=0).
4. TCHBLK is programmed to block channel 2.

TRANSMIT SIDE 1.544 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 12–9**TRANSMIT SIDE 2.048 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED)** Figure 12–10**NOTES:**

1. TSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 is ignored.
2. TCHBLK is forced to 1 in the same channels as TSER (see Note 1).

DS21Q41B TRANSMIT DATA FLOW Figure 12–11



13.0 AC AND DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

-1.0V to +7.0V

Operating Temperature

0°C to +70°C

Storage Temperature

-55°C to +125°C

Soldering Temperature

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.50		5.50	V	1

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		30		mA	1
Input Leakage	I_{IL}	-1.0		+1.0	μA	2
Output Leakage	I_{LO}			1.0	μA	3
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. TCLK = RCLK = TSYCLK = RSYCLK = 1.544 MHz ; outputs open circuited.
2. $0.0V < V_{IN} < V_{DD}$
3. Applies to INT when 3—stated.

**AC CHARACTERISTICS – MULTIPLEXED PARALLEL
PORT (MUX=1)**
(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS Low or \overline{RD} High	PW_{EL}	100			ns	
Pulse Width, DS High or \overline{RD} Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			20	ns	
R/W Hold Time	t_{RWH}	10			ns	
R/W Setup Time Before DS High	t_{RWS}	50			ns	
\overline{CS} , FS0, FS1 Setup Time before DS, \overline{WR} , or \overline{RD} Active	t_{CS}	20			ns	
\overline{CS} , FS0, FS1 Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t_{ASL}	15			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS, \overline{WR} or \overline{RD} to AS or ALE Rise	t_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, \overline{WR} or \overline{RD}	t_{ASED}	10			ns	
Output Data Delay Time from DS or \overline{RD}	t_{DDR}	20		80	ns	
Data Setup Time	t_{DSW}	50			ns	

See Figures 13–1 to 13–3 for details.

AC CHARACTERISTICS – RECEIVE SIDE (0°C to 70°C; V_{DD}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t _{CP}		648		ns	
RCLK Pulse Width	t _{CH} t _{CL}	75 75			ns ns	
RSYSCLK Period	t _{SP} t _{SP}		648 488		ns ns	1 2
RSYSCLK Pulse Width	t _{SH} t _{SL}	75 75			ns	
RSYNC Set Up to RSYCLK Falling or RPOS/RNEG Set Up to RCLK Falling	t _{SU}	20			ns	
RSYNC Hold from RSYCLK Falling or RPOS/RNEG Hold from RCLK Falling	t _{HD}	20			ns	
RCLK and RSYCLK Rise and Fall Times	t _R , t _F			25	ns	
Delay RCLK or RSYCLK to RSER Valid	t _{DD}			75	ns	
Delay RCLK or RSYCLK to RCHCLK	t _{D1}			75	ns	
Delay RCLK or RSYCLK to RCHBLK	t _{D2}			75	ns	
Delay RCLK to RFSYNC or RSYNC or Delay RSYCLK to RMSYNC or RSYNC	t _{D3}			75	ns	
Delay RCLK to RLCLK	t _{D4}			75	ns	
Delay RCLK to RLINK Valid	t _{D5}			75	ns	

See Figures 13–4 to 13–6 for details.

NOTES:

1. RSYCLK=1.544 MHz
2. RSYCLK=2.048 MHz

AC CHARACTERISTICS – TRANSMIT SIDE (0°C to 70°C; $V_{DD}=5V \pm 10\%$)

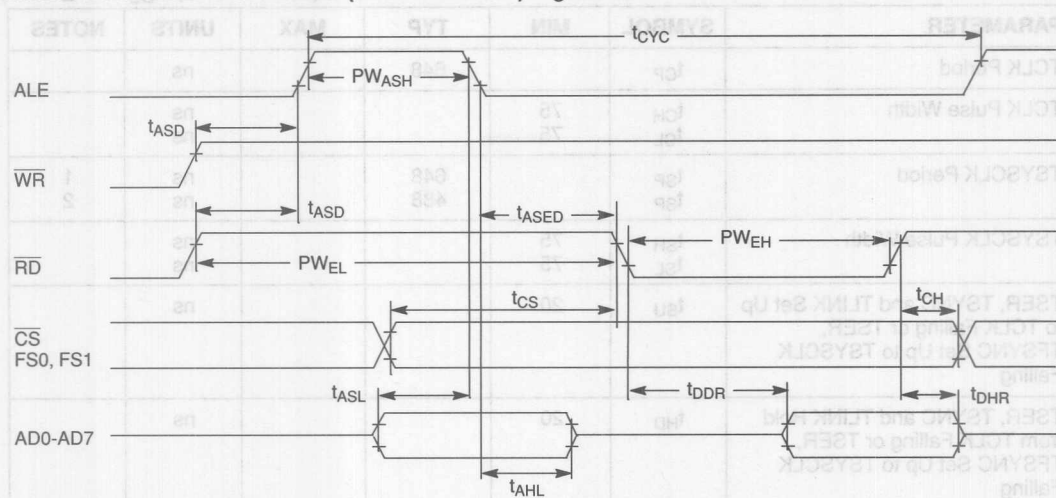
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		648		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TSYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	1 2
TSYSCLK Pulse Width	t_{SH} t_{SL}	75 75			ns ns	
TSER, TSYNC and TLINK Set Up to TCLK Falling or TSER, TFSYNC Set Up to TSYSCLK Falling	t_{SU}	20			ns	
TSER, TSYNC and TLINK Hold from TCLK Falling or TSER, TFSYNC Set Up to TSYSCLK Falling	t_{HD}	20			ns	
TCLK or TSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay TCLK to TPOS/TNEG Valid	t_{DD}			75	ns	
Delay TCLK to TCHCLK or TSYSCLK to TCHCLK	t_{D1}			75	ns	
Delay TCLK to TCHBLK or TSYSCLK to TCHBLK	t_{D2}			75	ns	
Delay TCLK to TSYNC	t_{D3}			75	ns	
Delay TCLK to TLCLK	t_{D4}			75	ns	

See Figures 13–7 to 13–9 for details.

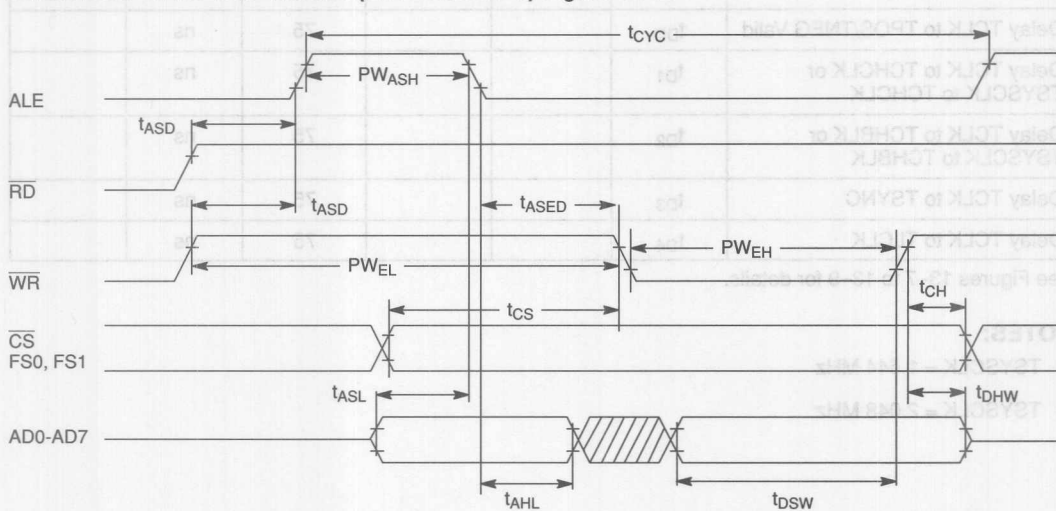
NOTES:

1. TSYSCLK = 1.544 MHz
2. TSYSCLK = 2.048 MHz

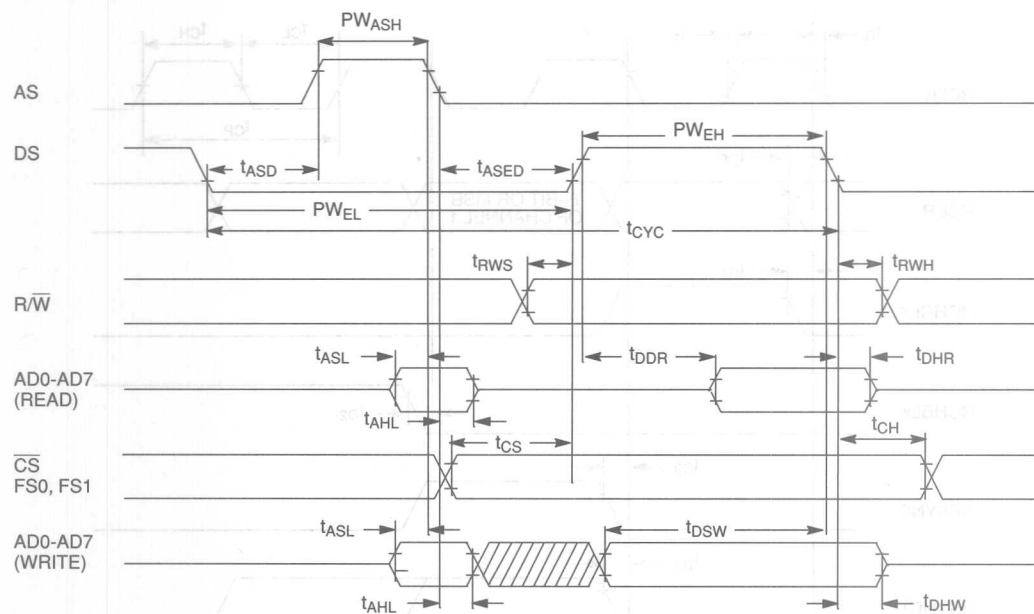
INTEL BUS READ AC TIMING (BTS=0/MUX=1) Figure 13-1



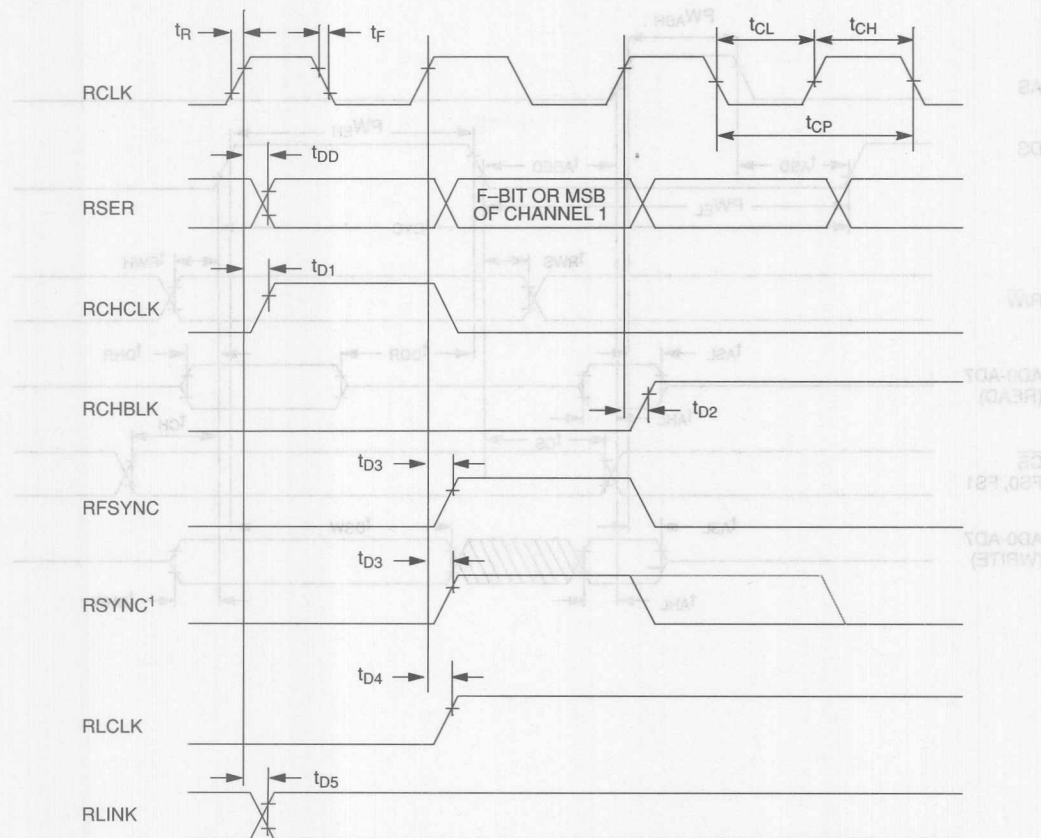
INTEL BUS WRITE AC TIMING (BTS=0/MUX=1) Figure 13-2



MOTOROLA BUS AC TIMING (BTS=1/MUX=1) Figure 13-3

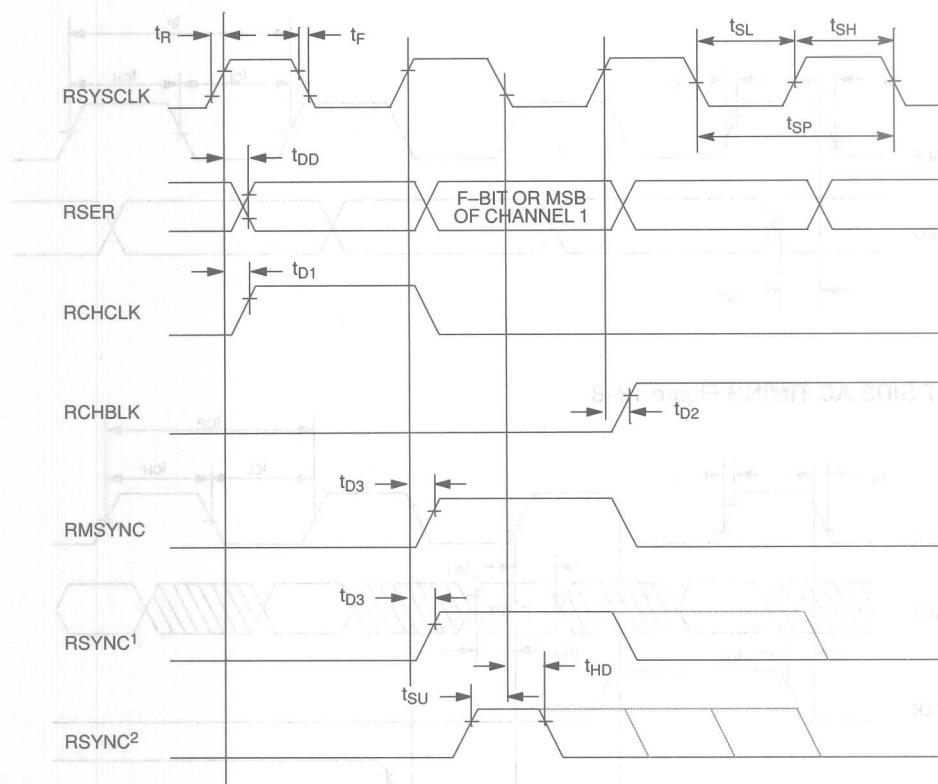


RECEIVE SIDE AC TIMING Figure 13-4

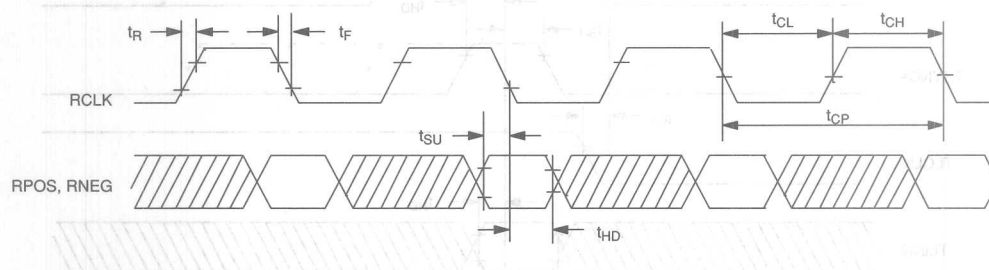
**NOTE:**

1. RSYNC is in the output mode (RCR2.3=0).

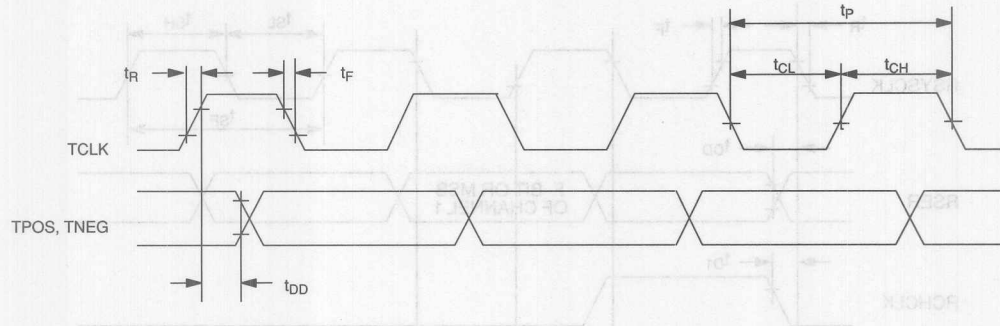
RECEIVE SYSTEM SIDE AC TIMING Figure 13-5



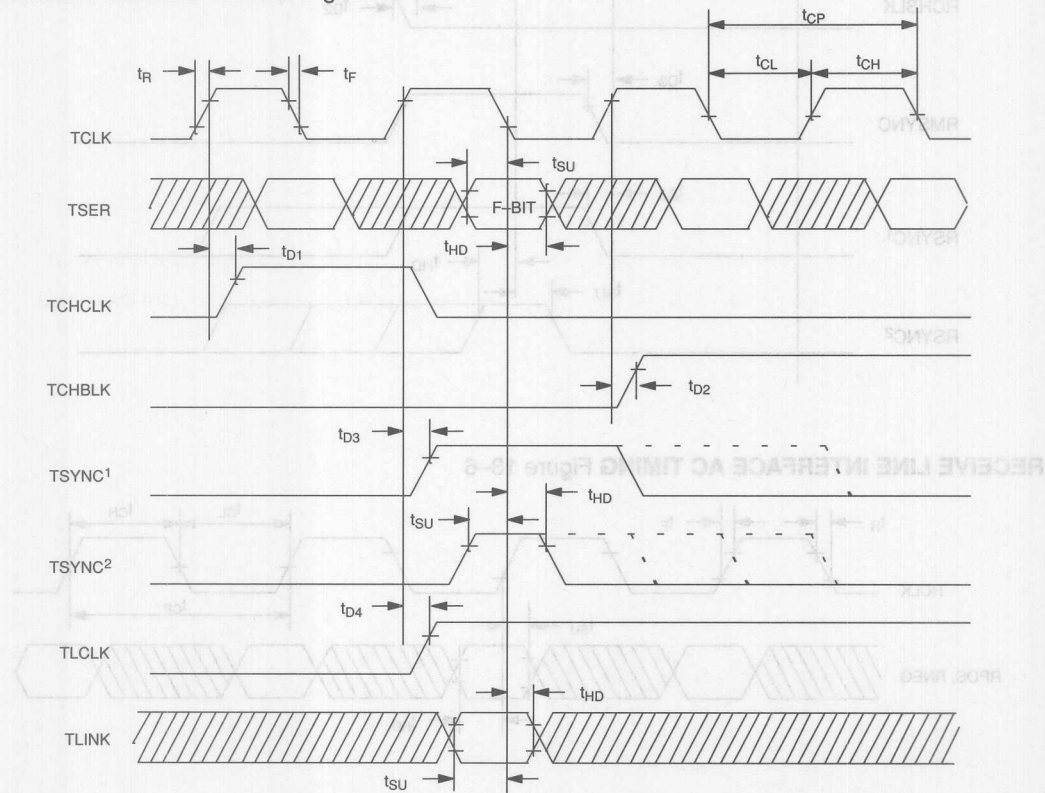
RECEIVE LINE INTERFACE AC TIMING Figure 13-6



TRANSMIT LINE INTERFACE SIDE AC TIMING Figure 13–7

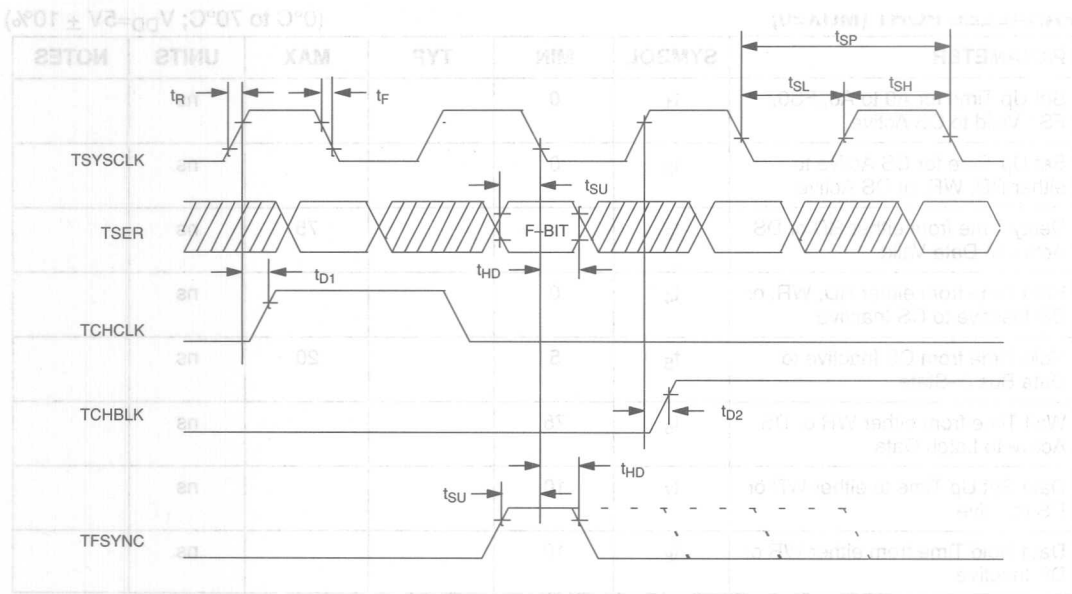


TRANSMIT SIDE AC TIMING Figure 13–8



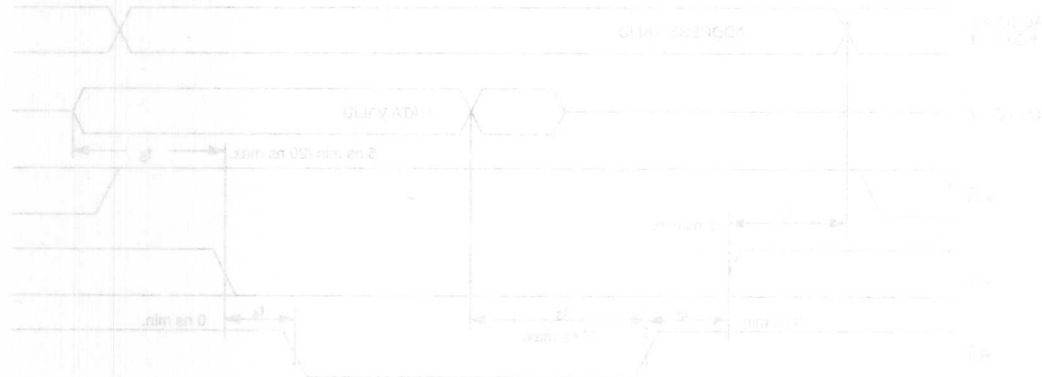
NOTES:

1. TSYNC is in the output mode (TCR2.2=1).
2. TSYNC is in the input mode (TCR2.2=0).
3. TSER is sampled on the falling edge of TCLK when the transmit side elastic store is disabled.
4. TCHCLK and TCHBLK are synchronous with TCLK when the transmit side elastic store is disabled.



NOTES:

1. TSER is only sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
2. TCHCLK and TCHBLK are synchronous with TSYSCLK when the transmit side elastic store is enabled.

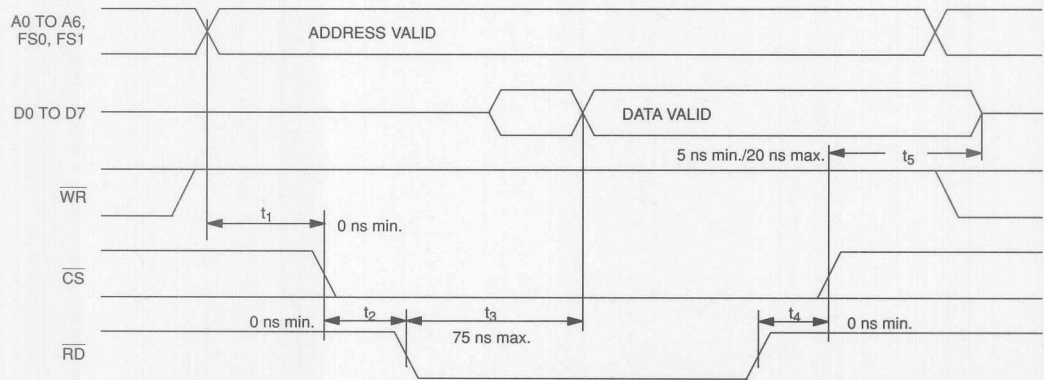


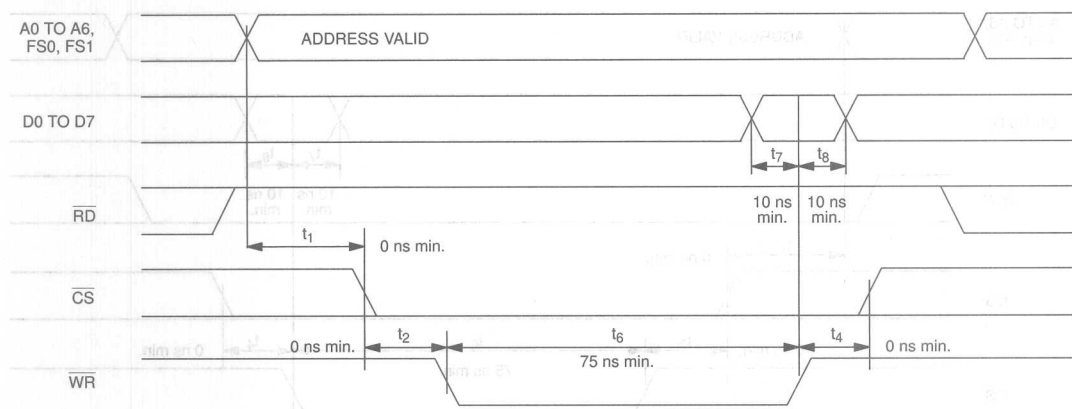
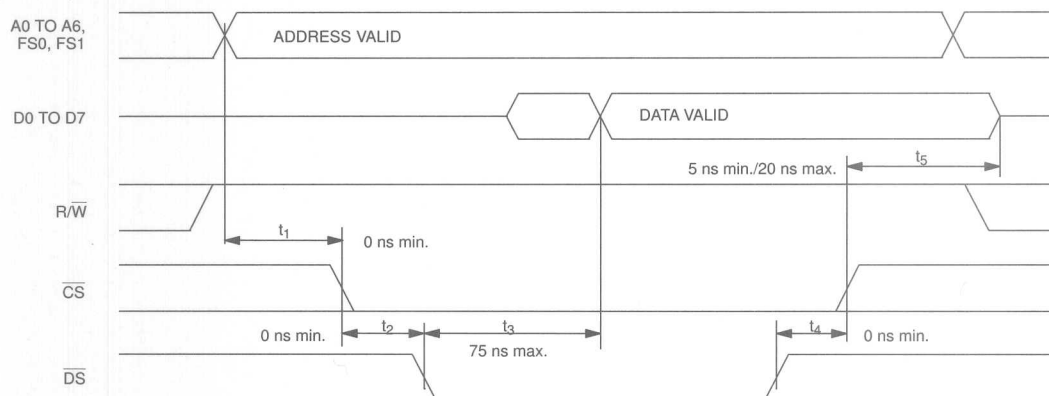
**AC CHARACTERISTICS – NON-MULTIPLEXED
PARALLEL PORT (MUX=0)** (0°C to 70°C; V_{DD}=5V ± 10%)

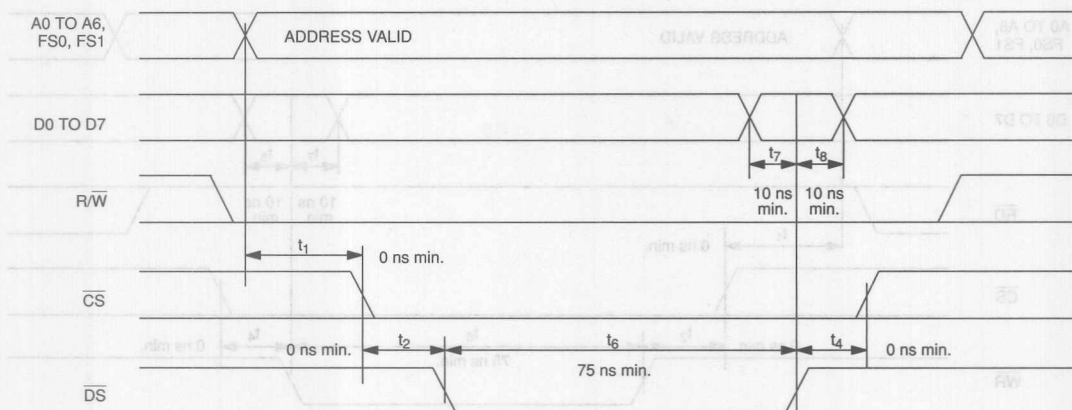
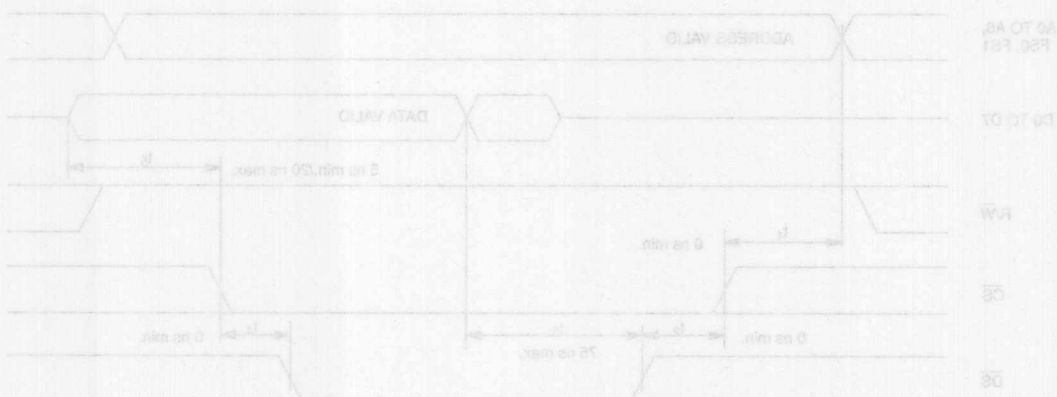
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A6, FS0, FS1 Valid to CS Active	t ₁	0			ns	
Set Up Time for CS Active to either RD, WR, or DS Active	t ₂	0			ns	
Delay Time from either RD or DS Active to Data Valid	t ₃			75	ns	
Hold Time from either RD, WR, or DS Inactive to CS Inactive	t ₄	0			ns	
Hold Time from CS Inactive to Data Bus 3-State	t ₅	5		20	ns	
Wait Time from either WR or DS Active to Latch Data	t ₆	75			ns	
Data Set Up Time to either WR or DS Inactive	t ₇	10			ns	
Data Hold Time from either WR or DS Inactive	t ₈	10			ns	

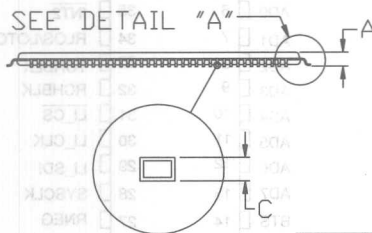
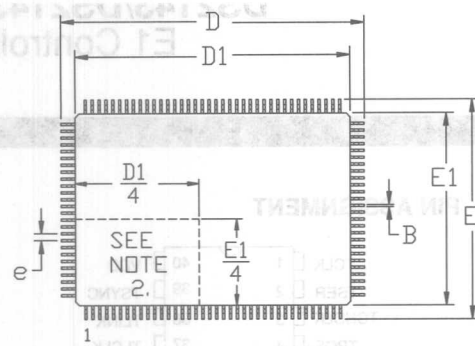
See Figures 13–10 to 13–13 for details.

INTEL BUS READ AC TIMING (BTS=0/MUX=0) Figure 13–10



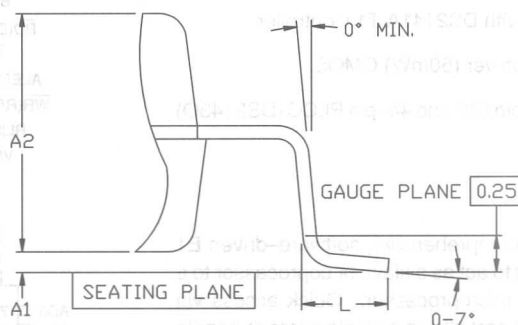
INTEL BUS WRITE AC TIMING (BTS=0/MUX=0) Figure 13–11

MOTOROLA BUS READ AC TIMING (BTS=1/MUX=0) Figure 13–12


MOTOROLA BUS WRITE AC TIMING (BTS=1/MUX=0) Figure 13-13

MOTOROLA BUS READ AC TIMING (BTS=1/MUX=0) Figure 13-12




NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.



DETAIL A

DIMENSIONS ARE IN MILLIMETERS

PKG	128-PIN	
DIM	MIN	MAX
A		1.60
A1	0.05	—
A2	1.35	1.45
B	0.17	0.27
C	0.09	0.20
D	21.80	22.20
D1	20.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75

56-G4011-000

1.0 INTRODUCTION

The DS2143 E1 Controller has four main sections: the receive side, the transmit side, the line interface controller, and the parallel control port. See the Block Diagram. On the receive side, the device will clock in the serial E1 stream via the RPOS and RNEG pins. The synchronizer will locate the frame and multiframe patterns and establish their respective positions. This information will be used by the rest of the receive side circuitry.

The DS2143 is an "off-line" framer, which means that all of the E1 serial stream that goes into the device, will come out of it, unchanged. Once the E1 data has been framed to, the signaling data can be extracted. The two-frame elastic store can either be enabled or bypassed.

The transmit side clocks in the unframed E1 stream at TSER and adds in the framing pattern and the signaling. The line Interface control port will update line interface devices that contain a serial port. The parallel control port contains a multiplexed address and data structure which can be connected to either a microcontroller or microprocessor.

Reader's Note:

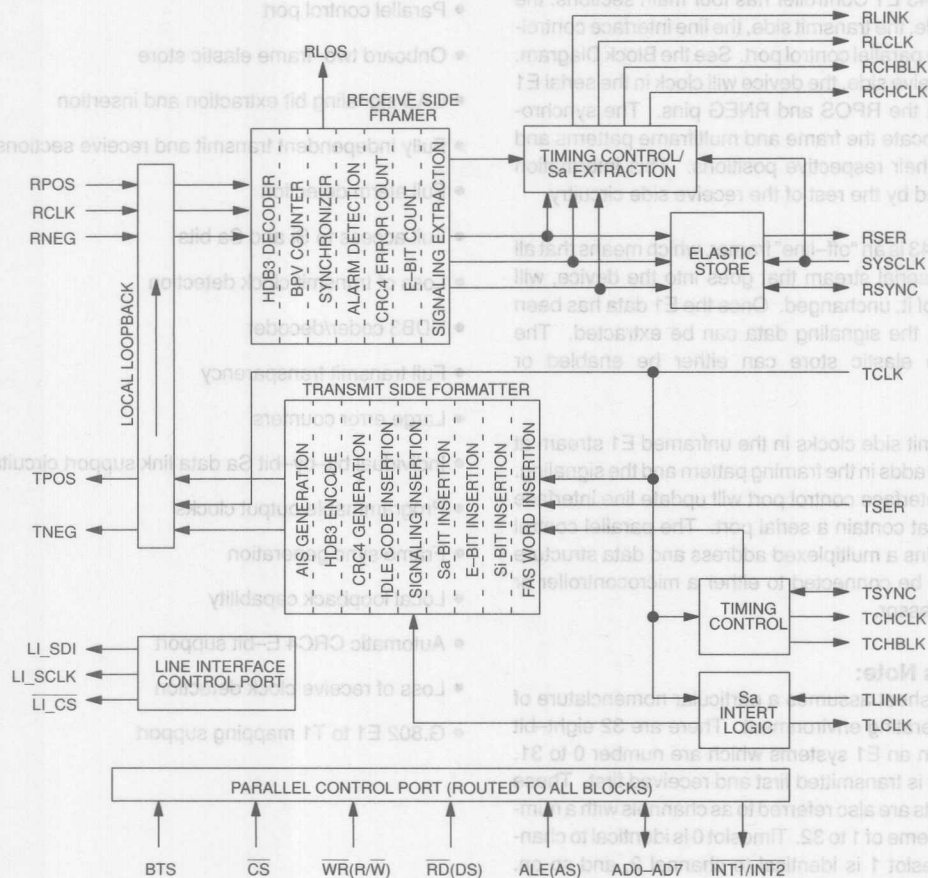
This data sheet assumes a particular nomenclature of the E1 operating environment. There are 32 eight-bit timeslots in an E1 systems which are number 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to channel 2, and so on. Each timeslot (or channel) is made up of eight bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment Signal
CRC4	Cyclical Redundancy Check
CAS	Channel Associated Signaling
CCS	Common Channel Signaling
MF	Multiframe
Sa	Additional bits
Si	International bits
E-bit	CRC4 Error bits

DS2143 FEATURES

- Parallel control port
- Onboard two-frame elastic store
- CAS signaling bit extraction and insertion
- Fully independent transmit and receive sections
- Full alarm detection
- Full access to Si and Sa bits
- Loss of transmit clock detection
- HDB3 coder/decoder
- Full transmit transparency
- Large error counters
- Individual bit-by-bit Sa data link support circuitry
- Programmable output clocks
- Frame sync generation
- Local loopback capability
- Automatic CRC4 E-bit support
- Loss of receive clock detection
- G.802 E1 to T1 mapping support

DS2143 BLOCK DIAGRAM



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TCLK	I	Transmit Clock. 2.048 MHz primary clock. A clock must be applied at the TCLK pin for the parallel port to operate properly.
2	TSER	I	Transmit Serial Data. Transmit NRZ serial data, sampled on the falling edge of TCLK.
3	TCHCLK	O	Transmit Channel Clock. 256 KHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data. See Section 13 for timing details.
4 5	TPOS TNEG	O	Transmit Bipolar Data. Updated on rising edge of TCLK. For optical links, can be programmed to output NRZ data.
6–13	AD0–AD7	I/O	Address/Data Bus. A 8-bit multiplexed address/data bus.
14	BTS	I	Bus Type Select. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}(DS)$, ALE(AS), and WR(R/W) pins. If BTS=1, then these pins assume the function listed in parenthesis ().
15	$\overline{RD}(DS)$	I	Read Input (Data Strobe).
16	\overline{CS}	I	Chip Select. Must be low to read or write the port.
17	ALE(AS)	I	Address Latch Enable (Address Strobe). A positive going edge serves to demultiplex the bus.
18	WR(R/W)	I	Write Input (Read/Write).
19	RLINK	O	Receive Link Data. Outputs 8a bits. See Section 13 for timing details.
20	V _{SS}	–	Signal Ground. 0.0 volts.
21	RLCLK	O	Receive Link Clock. 4 KHz to 20 KHz demand clock for the RLINK output. Controlled by RCR2. See Section 13 for timing details.
22	RCLK	I	Receive Clock. 2.048 MHz primary clock. A clock must be applied at the RCLK pin for the parallel port to operate properly.
23	RCHCLK	O	Receive Channel Clock. 256 KHz clock which pulses high during the LSB of each channel. Useful for serial to parallel conversion of channel data. See Section 13 for timing details.
24	RSER	O	Receive Serial Data. Received NRZ serial data, updated on rising edges of RCLK.
25	RSYNC	I/O	Receive Sync. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR1.6=0) or multiframe boundaries (RCR1.6=1). If the elastic store is enabled via the RCR2.1, then this pin can be enabled to be an input via RCR1.5 at which a frame boundary pulse is applied. See Section 13 for timing details.
26 27	RPOS RNEG	I	Receive Bipolar Data Inputs. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable BPV monitoring circuitry.
28	SYSCLK	I	System Clock. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled via the RCR2.1. Should be tied low in applications that do not use the elastic store.
29	LI_SDI	O	Serial Port Data for the Line Interface. Connects directly to the SDI input pin on the line interface. See Sections 12 and 13 for timing details.

PIN	SYMBOL	TYPE	DESCRIPTION
30	LI_CLK	O	Serial Port Clock for the Line Interface. Connects directly to the SCLK input pin on the line interface. See Sections 12 and 13 for timing details.
31	LI_CS	O	Serial Port Chip Select for the Line Interface. Connects directly to the CS input pin on the line interface. See Sections 12 and 13 for timing details.
32	RCHBLK	O	Receive/Transmit Channel Block. A user programmable output that can be forced high or low during any of the 32 E1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1 or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Sections 9 and 13 for details.
33	TCHBLK	O	
34	RLOS/LOTC	O	Receive Loss of Sync/Loss of Transmit Clock. A dual function output. If TCR2.0=0, then this pin will toggle high when the synchronizer is searching for the E1 frame and multiframe. If TCR2.0=1, then this pin will toggle high if the TCLK pin has not toggled for 5 μ s.
35	INT2	O	Receive Alarm Interrupt 2. Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
36	INT1	O	Receive Alarm Interrupt 1. Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
37	TLCLK	O	Transmit Link Clock. 4 KHz to 20 KHz demand clock for the TLINK input. Controlled by TCR2. See Section 13 for timing details.
38	TLINK	I	Transmit Link Data. If enabled, this pin will be sampled on the falling edge of TCLK to insert Sa bits. See Section 13 for timing details.
39	TSYNC	I/O	Transmit Sync. A pulse at this pin will establish either frame or CAS multiframe boundaries for the DS2143. Via TCR1.1, the DS2143 can be programmed to output either a frame or multiframe pulse at this pin. See Section 13 for timing details.
40	VDD	—	Positive Supply. 5.0 volts.

DS2143 REGISTER MAP

ADDRESS A7 to A0	HEX	R/W	REGISTER NAME
00000000	00	R	Bipolar Violation Count Register 1.
00000001	01	R	Bipolar Violation Count Register 2.
00000010	02	R	CRC4 Count Register 1.
00000011	03	R	CRC4 Count Register 2.
00000100	04	R	E-Bit Count Register 1.
00000101	05	R	E-Bit Count Register 2.
00000110	06	R/W	Status Register 1.
00000111	07	R/W	Status Register 2.
00001000	08	R/W	Receive Information Register.
00011110	1E	R	Synchronizer Status Register.
00010110	16	R/W	Interrupt Mask Register 1.
00010111	17	R/W	Interrupt Mask Register 2.
00010000	10	R/W	Receive Control Register 1.
00010001	11	R/W	Receive Control Register 2.
00010010	12	R/W	Transmit Control Register 1.
00010011	13	R/W	Transmit Control Register 2.
00010100	14	R/W	Common Control Register.
00010101	15	R/W	Test Register.
00011000	18	W	LI Control Register Byte 1.
00011001	19	W	LI Control Register Byte 2.
00100000	20	R/W	Transmit Align Frame Register.
00100001	21	R/W	Transmit Non-Align Frame Register.
00101111	2F	R	Receive Align Frame Register.
00011111	1F	R	Receive Non-Align Frame Register.
00100010	22	R/W	Transmit Channel Blocking Register 1.

ADDRESS A7 to A0	HEX	R/W	REGISTER NAME
00100011	23	R/W	Transmit Channel Blocking Register 2.
00100100	24	R/W	Transmit Channel Blocking Register 3.
00100101	25	R/W	Transmit Channel Blocking Register 4.
00100110	26	R/W	Transmit Idle Register 1.
00100111	27	R/W	Transmit Idle Register 2.
00101000	28	R/W	Transmit Idle Register 3.
00101001	29	R/W	Transmit Idle Register 4.
00101010	2A	R/W	Transmit Idle Definition Register.
00101011	2B	R/W	Receive Channel Blocking Register 1.
00101100	2C	R/W	Receive Channel Blocking Register 2.
00101101	2D	R/W	Receive Channel Blocking Register 3.
00101110	2E	R/W	Receive Channel Blocking Register 4.
00110000	30	R	Receive Signaling Register 1.
00110001	31	R	Receive Signaling Register 2.
00110010	32	R	Receive Signaling Register 3.
00110011	33	R	Receive Signaling Register 4.
00110100	34	R	Receive Signaling Register 5.
00110101	35	R	Receive Signaling Register 6.
00110110	36	R	Receive Signaling Register 7.
00110111	37	R	Receive Signaling Register 8.
00111000	38	R	Receive Signaling Register 9.
00111001	39	R	Receive Signaling Register 10.
00111010	3A	R	Receive Signaling Register 11.

ADDRESS A7 to A0	HEX	R/W	REGISTER NAME
00111011	3B	R	Receive Signaling Register 12.
00111100	3C	R	Receive Signaling Register 13.
00111101	3D	R	Receive Signaling Register 14.
00111110	3E	R	Receive Signaling Register 15.
00111111	3F	R	Receive Signaling Register 16.
01000000	40	R/W	Transmit Signaling Register 1.
01000001	41	R/W	Transmit Signaling Register 2.
01000010	42	R/W	Transmit Signaling Register 3.
01000011	43	R/W	Transmit Signaling Register 4.
01000100	44	R/W	Transmit Signaling Register 5.
01000101	45	R/W	Transmit Signaling Register 6.
01000110	46	R/W	Transmit Signaling Register 7.
01000111	47	R/W	Transmit Signaling Register 8.
01001000	48	R/W	Transmit Signaling Register 9.
01001001	49	R/W	Transmit Signaling Register 10.
01001010	4A	R/W	Transmit Signaling Register 11.
01001011	4B	R/W	Transmit Signaling Register 12.
01001100	4C	R/W	Transmit Signaling Register 13.
01001101	4D	R/W	Transmit Signaling Register 14.
01001110	4E	R/W	Transmit Signaling Register 15.
01001111	4F	R/W	Transmit Signaling Register 16.

2.0 PARALLEL PORT

The DS2143 is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2143 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the AC Electrical Characteristics for more details. The multiplexed bus on the DS2143 saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the DS2143 latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or \overline{WR} pulses. In a read cycle, the DS2143 outputs a byte of data during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as \overline{RD} transitions high in Intel timing or as DS transitions low in Motorola timing.

3.0 CONTROL AND TEST REGISTERS

The operation of the DS2143 is configured via a set of five registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2143 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and a Common Control Register (CCR). Each of the five registers are described in this section.

The Test Register at address 15 hex is used by the factory in testing the DS2143. On power-up, the Test Register should be set to 00 hex in order for the DS2143 to operate properly.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB)

(LSB)

RSMF	RSM	RSIO	—	—	FRC	SYNCE	RESYNC
------	-----	------	---	---	-----	-------	--------

SYMBOL

POSITION

NAME AND DESCRIPTION

RSMF	RCR1.7	RSYNC Multiframe Function. Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6=1). 0 = RSYNC outputs CAS multiframe boundaries 1 = RSYNC outputs CRC4 multiframe boundaries
RSM	RCR1.6	RSYNC Mode Select. 0 = frame mode (see the timing in Section 13) 1 = multiframe mode (see the timing in Section 13)
RSIO	RCR1.5	RSYNC I/O Select. 0 = RSYNC is an output (depends on RCR1.6) 1 = RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to zero when RCR2.1=0)
—	RCR1.4	Not Assigned. Should be set to zero when written to.
—	RCR1.3	Not Assigned. Should be set to zero when written to.
FRC	RCR1.2	Frame Resync Criteria. 0 = resync if FAS received in error 3 consecutive times 1 = resync if FAS or bit 2 of non-FAS is received in error 3 consecutive times
SYNCE	RCR1.1	Sync Enable. 0 = auto resync enabled 1 = auto resync disabled
RESYNC	RCR1.0	Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

SYNC/RESYNC CRITERIA Table 2

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frames N and N + 2, and FAS not present in frame N + 1.	Three consecutive incorrect FAS received. Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non-FAS received.	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms.	915 or more CRC4 code words out of 1000 received in error.	G.706 4.2 4.3.2
CAS	Valid MF alignment word found and previous time slot 16 contains code other than all zeros.	Two consecutive MF alignment words received in error.	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB)				(LSB)			
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	SCLKM	ESE	—
SYMBOL	POSITION	NAME AND DESCRIPTION					
Sa8S	RCR2.7	Sa8 Bit Select. Set to one to report the Sa8 bit at the RLINK pin; set to zero to not report the Sa8 bit.					
Sa7S	RCR2.6	Sa7 Bit Select. Set to one to report the Sa7 bit at the RLINK pin; set to zero to not report the Sa7 bit.					
Sa6S	RCR2.5	Sa6 Bit Select. Set to one to report the Sa6 bit at the RLINK pin; set to zero to not report the Sa6 bit.					
Sa5S	RCR2.4	Sa5 Bit Select. Set to one to report the Sa5 bit at the RLINK pin; set to zero to not report the Sa5 bit.					
Sa4S	RCR2.3	Sa4 Bit Select. Set to one to report the Sa4 bit at the RLINK pin; set to zero to not report the Sa4 bit.					
SCLKM	RCR2.2	SYSCCLK Mode Select. 0 = if SYSCCLK is 1.544 MHz 1 = if SYSCCLK is 2.048 MHz					
ESE	RCR2.1	Elastic Store Enable. 0 = elastic store is bypassed 1 = elastic store is enabled					
—	RCR2.0	Not Assigned. Should be set to zero when written to.					

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)				(LSB)			
ODF	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO
SYMBOL	POSITION	NAME AND DESCRIPTION					
ODF	TCR1.7	Output Data Format. 0 = bipolar data at TPOS and TNEG 1 = NRZ data at TPOS; TNEG=0					
TFPT	TCR1.6	Transmit Timeslot 0 Pass Through. 0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1 = FAS bits/Sa bits/Remote Alarm sourced from TSER					
T16S	TCR1.5	Transmit Timeslot 16 Data Select. 0 = sample timeslot 16 at TSER pin 1 = source timeslot 16 from TS1 to TS16 registers					
TUA1	TCR1.4	Transmit Unframed All Ones. 0 = transmit data normally 1 = transmit an unframed all one's code at TPOS and TNEG					
TSiS	TCR1.3	Transmit International Bit Select. 0 = sample Si bits at TSER pin 1 = source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)					

TSA1	TCR1.2	Transmit Signaling All Ones. 0 = normal operation 1 = force timeslot 16 in every frame to all ones
TSM	TCR1.1	TSYNC Mode Select. 0 = frame mode (see the timing in Section 13) 1 = CAS and CRC4 multiframe mode (see the timing in Section 13)
TSIO	TCR1.0	TSYNC I/O Select. 0 = TSYNC is an input 1 = TSYNC is an output

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)			(LSB)				
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	—	AEBE	P34F

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	Sa8 Bit Select. Set to one to source the Sa8 bit from the TLINK pin; set to zero to not source the Sa8 bit.
Sa7S	TCR2.6	Sa7 Bit Select. Set to one to source the Sa7 bit from the TLINK pin; set to zero to not source the Sa7 bit.
Sa6S	TCR2.5	Sa6 Bit Select. Set to one to source the Sa6 bit from the TLINK pin; set to zero to not source the Sa6 bit.
Sa5S	TCR2.4	Sa5 Bit Select. Set to one to source the Sa5 bit from the TLINK pin; set to zero to not source the Sa5 bit.
Sa4S	TCR2.3	Sa4 Bit Select. Set to one to source the Sa4 bit from the TLINK pin; set to zero to not source the Sa4 bit.
—	TCR2.2	Not Assigned. Should be set to zero when written to.
AEBE	TCR2.1	Automatic E-Bit Enable. 0 = E-bits not automatically set in the transmit direction 1 = E-bits automatically set in the transmit direction
P34F	TCR2.0	Function of Pin 34. 0 = Receive Loss of Sync (RLOS) 1 = Loss of Transmit Clock (LOTIC)

CCR: COMMON CONTROL REGISTER (Address=14 Hex)

(MSB)				(LSB)			
LLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOL	POSITION	NAME AND DESCRIPTION
LLB	CCR.7	Local Loopback. 0 = loopback disabled 1 = loopback enabled
THDB3	CCR.6	Transmit HDB3 Enable. 0 = HDB3 disabled 1 = HDB3 enabled

TG802	CCR.5	Transmit G.802 Enable. See Section 13 for details. 0 = do not force TCHBLK high during bit 1 of timeslot 26 1 = force TCHBLK high during bit 1 of timeslot 26
TCRC4	CCR.4	Transmit CRC4 Enable. 0 = CRC4 disabled 1 = CRC4 enabled
RSM	CCR.3	Receive Signaling Mode Select. 0 = CAS signaling mode 1 = CCS signaling mode
RHDB3	CCR.2	Receive HDB3 Enable. 0 = HDB3 disabled 1 = HDB3 enabled
RG802	CCR.1	Receive G.802 Enable. See Section 13 for details. 0 = do not force RCHBLK high during bit 1 of timeslot 26 1 = force RCHBLK high during bit 1 of timeslot 26
RCRC4	CCR.0	Receive CRC4 Enable. 0 = CRC4 disabled 1 = CRC4 enabled

LOCAL LOOPBACK

When CCR.7 is set to a one, the DS2143 will enter a Local LoopBack (LLB) mode. This loopback is useful in testing and debugging applications. In LLB, the DS2143 will loop data from the transmit side back to the receive side. This loopback is synonymous with replacing the RCLK input with the TCLK signal, and the RPOS/RNEG inputs with the TPOS/TNEG outputs. When LLB is enabled, the following will occur;

1. data at RPOS and RNEG will be ignored
2. all receive side signals will take on timing synchronous with TCLK instead of RCLK
3. all functions are available.

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2143, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR). When a particular event has occurred (or is occurring), the appropriate bit in one of these three registers will be set to a one. All of the bits in these registers operate in a latched fashion (except for the SSR). This means that if an event occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of the SR1, SR2, and RIR registers with a write. The byte written to the register will inform the DS2143 which bits the user wishes to read and have cleared. The user will write a byte to one of these three registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2143 with higher order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this registers with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the INT1 and INT2 pins respectively. Each of the alarms and events in the SR1

and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

RIR: RECEIVE INFORMATION REGISTER (Address=08 Hex)

(MSB)				(LSB)			
—	—	—	ESF	ESE	—	FASRC	CASRC

SYMBOL	POSITION	NAME AND DESCRIPTION
—	RIR.7	Not Assigned. Could be any value when read.
—	RIR.6	Not Assigned. Could be any value when read.
—	RIR.5	Not Assigned. Could be any value when read.
ESF	RIR.4	Elastic Store Full. Set when the elastic store buffer fills and a frame is deleted.
ESE	RIR.3	Elastic Store Empty. Set when the elastic store buffer empties and a frame is repeated.
—	RIR.2	Not Assigned. Could be any value when read.
FASRC	RIR.1	FAS Resync Criteria Met. Set when three consecutive FAS words are received in error.
CASRC	RIR.0	CAS Resync Criteria Met. Set when two consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)				(LSB)			
CSC5	CSC4	CSC3	CSC2	CSC1	FASSA	CASSA	CRC4SA

SYMBOL	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	CRC4 Sync Counter Bit 5. MSB of the 6-bit counter.
CSC4	SSR.6	CRC4 Sync Counter Bit 4.
CSC3	SSR.5	CRC4 Sync Counter Bit 3.
CSC2	SSR.4	CRC4 Sync Counter Bit 2.
CSC1	SSR.3	CRC4 Sync Counter Bit 1. Next to LSB of the 6-bit counter. The LSB is not accessible.
FASSA	SSR.2	FAS Sync Active. Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	CAS MF Sync Active. Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	CRC4 MF Sync Active. Set while the synchronizer is searching for the CRC4 MF alignment word.

CRC4 SYNC COUNTER

The CRC4 Sync Counter increments each time the 8ms CRC4 multiframe search times out. The counter is cleared when the DS2143 has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR.0=0). This counter is useful for determining the

amount of time the DS2143 has been searching for synchronization at the CRC4 level. Annex B of CCITT G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

SR1: STATUS REGISTER 1 (Address=06 Hex)

(MSB)				(LSB)			
SYMBOL		POSITION		NAME AND DESCRIPTION			
RSA1	RDMA	RSA0	SLIP	RUA1	RRA	RCL	RLOS
RSA1	SR1.7	RDMA	SR1.6	RSA0	SR1.5	SLIP	SR1.4
RUA1	SR1.3	RRA	SR1.2	RCL	SR1.1	RLOS	SR1.0
Receive Signaling All Ones. Set when the contents of timeslot 16 contains less than 3 zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.				Receive Distant MF Alarm. Set when bit 6 of timeslot 16 in frame 0 has been set for 2 consecutive multiframe. This alarm is not disabled in the CCS signaling mode.			
Receive Signaling All Zeros. Set when over a full MF, timeslot 16 contains all zeros.				Elastic Store Slip Occurrence. Set when the elastic store has either repeated or deleted a frame of data.			
Receive Unframed All Ones. Set when an unframed all ones code is received at RPOS and RNEG.				Receive Remote Alarm. Set when a remote alarm is received at RPOS and RNEG.			
Receive Carrier Loss. Set when 255 consecutive zeros have been detected at RPOS and RNEG.				Receive Loss of Sync. Set when the device is not synchronized to the receive E1 stream.			

ALARM CRITERIA Table 3

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all ones)	over 16 consecutive frames (one full MF) timeslot 16 contains less than 3 zeros	over 16 consecutive frames (one full MF) timeslot 16 contains 3 or more zeros	G.732 4.2
RSA0 (receive signaling all zeros)	over 16 consecutive frames (one full MF) timeslot 16 contains all zeros	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to one for two consecutive MF	bit 6 in timeslot 16 of frame 0 set to zero for a two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all ones)	less than 3 zeros in two frames (512 bits)	more than 2 zeros in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non-align frame set to one for 3 consecutive occasions	bit 3 of non-align frame set to zero for 3 consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 consecutive zeros received	in 255 bit times, at least 32 ones are received	G.775

Note: all the alarm bits in Status Register 1 except the RUA1 will remain set after they are read if the alarm condition still exists; the RUA1 will clear and check the next 512 bits for an all one's condition at which point it will again be set if the alarm condition still is present.

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB)

(LSB)

RMF	RAF	TMF	SEC	TAF	LOT	RCMF	LORC
-----	-----	-----	-----	-----	-----	------	------

SYMBOL POSITION**NAME AND DESCRIPTION**

RMF	SR2.7	Receive CAS Multiframe. Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	Receive Align Frame. Set every 250 μ s at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	Transmit Multiframe. Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	One Second Timer. Set on increments of one second based on RCLK.
TAF	SR2.3	Transmit Align Frame. Set every 250 μ s at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.

LOT	SR2.2	Loss of Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 3.9 μ s). Will force pin 34 high if enabled via TCR2.0. Based on RCLK.					
RCMF	SR2.1	Receive CRC4 Multiframe. Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.					
LORC	SR2.0	Loss of Receive Clock. Set when the RCLK pin has not transitioned for at least 2 μ s (3 μ s \pm 1 μ s).					
IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)							
(MSB)		(LSB)					
RSA1	RDMA	RSA0	SLIP	RUA1	RRA	RCL	RLOS
SYMBOL		POSITION		NAME AND DESCRIPTION			
RSA1		IMR1.7		Receive Signaling All Ones. 0 = interrupt masked 1 = interrupt enabled			
RDMA		IMR1.6		Receive Distant MF Alarm. 0 = interrupt masked 1 = interrupt enabled			
RSA0		IMR1.5		Receive Signaling All Zeros. 0 = interrupt masked 1 = interrupt enabled			
SLIP		IMR1.4		Elastic Store Slip Occurrence. 0 = interrupt masked 1 = interrupt enabled			
RUA1		IMR1.3		Receive Unframed All Ones. 0 = interrupt masked 1 = interrupt enabled			
RRA		IMR1.2		Receive Remote Alarm. 0 = interrupt masked 1 = interrupt enabled			
RCL		IMR1.1		Receive Carrier Loss. 0 = interrupt masked 1 = interrupt enabled			
RLOS		IMR1.0		Receive Loss of Sync. 0 = interrupt masked 1 = interrupt enabled			

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)				(LSB)			
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	LORC
SYMBOL	POSITION	NAME AND DESCRIPTION					
RMF	IMR2.7	Receive CAS Multiframe. 0 = interrupt masked 1 = interrupt enabled					
RAF	IMR2.6	Receive Align Frame. 0 = interrupt masked 1 = interrupt enabled					
TMF	IMR2.5	Transmit Multiframe. 0 = interrupt masked 1 = interrupt enabled					
SEC	IMR2.4	One Second Timer. 0 = interrupt masked 1 = interrupt enabled					
TAF	IMR2.3	Transmit Align Frame. 0 = interrupt masked 1 = interrupt enabled					
LOTC	IMR2.2	Loss Of Transmit Clock. 0 = interrupt masked 1 = interrupt enabled					
RCMF	IMR2.1	Receive CRC4 Multiframe. 0 = interrupt masked 1 = interrupt enabled					
LORC	IMR2.0	Loss of Receive Clock. 0 = interrupt masked 1 = interrupt enabled					

5.0 ERROR COUNT REGISTERS

There are a set of three counters in the DS2143 that record bipolar violations, errors in the CRC4 SMF code words, and E-bits as reported by the far end. Each of these three counters are automatically updated on one second boundaries as determined by the one second timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the one second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost.

SYMBOL	POSITION	NAME AND DESCRIPTION
EBIT3	EBIT3	MSB of the E-bit error count
EBIT2	EBIT2	MSB of the E-bit error count
EBIT1	EBIT1	MSB of the E-bit error count

BPVCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)**BPVCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2** (Address=01 Hex)

(MSB)				(LSB)				
BV7	BV6	BV5	BV4	BV3	BV2	BV1	BV0	BPVCR2
BV15	BV14	BV13	BV12	BV11	BV10	BV9	BV8	BPVCR1

SYMBOL	POSITION	NAME AND DESCRIPTION
BV15	BPVCR1.7	MSB of the bipolar violation count
BV0	BPVCR2.0	LSB of the bipolar violation count

Bipolar Violation Count Register 1 (BPVCR1) is the most significant word and BPVCR2 is the least significant word of a 16-bit counter that records bipolar violations (BPVs). If the HDB3 mode is set for the receive side via CCR.2, then HDB3 code words are not counted.

This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on a E1 line would have to be greater than 10^{-2} before the BPVCR would saturate.

CRCCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)**CRCCR2: CRC4 COUNT REGISTER 2** (Address=03 Hex)

(MSB)				(LSB)				
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2
CRC14	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	CRCCR1

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC15	CRCCR1.7	MSB of the CRC4 error count
CRC0	CRCCR2.0	LSB of the CRC4 error count

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 16-bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum

CRC4 count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of sync occurs at the CAS level.

EBCR1: E-BIT COUNT REGISTER 1 (Address=04 Hex)**EBCR2: E-BIT COUNT REGISTER 2** (Address=05 Hex)

(MSB)				(LSB)				
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2
EB15	EB14	EB13	EB12	EB11	EB10	EB9	EB8	EBCR1

SYMBOL	POSITION	NAME AND DESCRIPTION
EB15	EBCR1.7	MSB of the E-Bit error count
EB0	EBCR2.0	LSB of the E-Bit error count

E-bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 16-bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers

will increment once each time the received E-bit is set to zero. Since the maximum E-bit count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS

or CRC4 level; it will continue to count if loss of sync occurs at the CAS level.

6.0 Sa DATA LINK CONTROL AND OPERATION

The DS2143 provides for access to the proposed E1 performance monitor data link in the Sa bit positions. The device allows access to the Sa bits either via a set of two internal registers (RNAF and TNAF) or via two external pins (RLINK and TLINK).

On the receive side, the Sa bits are always reported in the internal RNAF register (see Section 11 for more details). All five Sa bits are always output at the RLINK pin. See Section 13 for detailed timing. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (TCR1.6=0) or from the external TLINK pin. Via TCR2, the DS2143 can be programmed to source any combination of the

additional bits from the TLINK pin. If the user wishes to pass the Sa bits through the DS2143 without them being altered, then the device should be set up to source all five Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Please see the timing diagrams and the transmit data flow diagram in Section 13 for examples.

7.0 SIGNALING OPERATION

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2143. Each of the 30 channels has four signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the channel associated with a particular signaling bit. The channel numbers have been assigned as described in the CCITT documents. For example, channel 1 is associated with timeslot 1 and channel 30 is associated with timeslot 31. There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB)				(LSB)				
0	0	0	0	X	Y	X	X	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	RS4 (33)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	RS7 (36)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	RS16 (3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	Spare Bits
Y	RS1.2	Remote Alarm Bit (integrated and reported in SR1.6)
A(1)	RS2.7	Signaling Bit A for Channel 1
D(30)	RS16.0	Signaling Bit D for Channel 30

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling from two timeslots. The bits in the Receive Signaling Registers are updated on multi-frame boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all

conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	Spare Bits
Y	TS1.2	Remote Alarm Bit
A(1)	TS2.7	Signaling Bit A for Channel 1
D(30)	TS16.0	Signaling Bit D for Channel 30

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the DS2143 will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSR's before the old data will be retransmitted.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper four bits must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to

the far end, then the TS1.5 bit should be set to a one. If no alarm is to be transmitted, then the TS1.5 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to one. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be informed when the signaling register's need to be loaded with data. The user has 2 ms to load the data before the old data will be retransmitted.

8.0 TRANSMIT IDLE REGISTERS

There is a set of five registers in the DS2143 that can be used to custom tailor the data that is to be transmitted onto the E1 line, on a channel by channel basis. Each of the 32 E1 channels can be forced to have a user defined idle code inserted into them.

TIR1/TIR2/TIR3/TIR4: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TIR4.7	Transmit Idle Registers. 0 = do not insert the Idle Code into this channel 1 = insert the Idle Code into this channel
CH1	TIR1.0	

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)				(LSB)			
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0
SYMBOL	POSITION	NAME AND DESCRIPTION					
TIDR7	TIDR.7	MSB of the Idle Code					
TIDR0	TIDR.0	LSB of the Idle Code					

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represent a timeslot in the outgoing frame. When these bits are set to a one, the corre-

sponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). In the TIDR, the MSB is transmitted first.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3/RCBR4) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHCLK pins respectively. The RCHBLK and TCHCLK pins are user programmable outputs that can be forced either high or

low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 13 for an example.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS

(Address=2B to 2E Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	RCBR4.7	Receive Channel Blocking Registers. 0 = force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1 = force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS

(Address=22 to 25 Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TCBR4.7	Transmit Channel Blocking Registers. 0 = force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1 = force the TCHBLK pin high during this channel time

10.0 ELASTIC STORE OPERATION

The DS2143 has an onboard two frame (512 bits) elastic store. This elastic store can be enabled via RCR2.1. If the elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2=0) or 2.048 MHz (RCR2.2=1) clock at the SYSCLK pin. If the elastic store is enabled, then the user has the option of either providing a frame sync at the RFSYNC pin (RCR1.5=1) or having the RFSYNC pin provide a pulse on frame or multiframe boundaries (RCR1.5=0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to one. If the user selects to apply a 1.544 MHz clock to the SYSCLK pin, then every fourth channel will be deleted and the F-bit position inserted (forced to one). Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted. Also, in 1.544 MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). See Section 13 for more details. If the 512-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

11.0 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS2143 provides for access to both the Additional (Sa) and International (Si) bits. On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 μs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 μs to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the DS2143 is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to one. Please see the register descriptions for TCR1 and TCR2 and the Transmit Data Flow diagram in Section 13 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB)				(LSB)			
Si	0	0	1	1	0	1	1
SYMBOL	POSITION	NAME AND DESCRIPTION					
Si	RAF.7	International Bit.					
0	RAF.6	Frame Alignment Signal Bit.					
0	RAF.5	Frame Alignment Signal Bit.					
1	RAF.4	Frame Alignment Signal Bit.					
1	RAF.3	Frame Alignment Signal Bit.					
0	RAF.2	Frame Alignment Signal Bit.					
1	RAF.1	Frame Alignment Signal Bit.					
1	RAF.0	Frame Alignment Signal Bit.					

RNAF: RECEIVE NON-ALIGN FRAME REGISTER (Address=1F Hex)

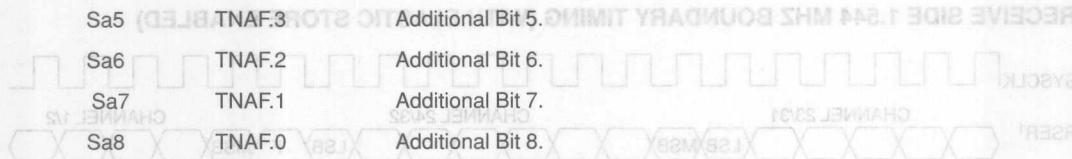
(MSB)				(LSB)			
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
SYMBOL	POSITION	NAME AND DESCRIPTION					
Si	RNAF.7	International Bit.					
1	RNAF.6	Frame Non-Alignment Signal Bit.					
A	RNAF.5	Remote Alarm.					
Sa4	RNAF.4	Additional Bit 4.					
Sa5	RNAF.3	Additional Bit 5.					
Sa6	RNAF.2	Additional Bit 6.					
Sa7	RNAF.1	Additional Bit 7.					
Sa8	RNAF.0	Additional Bit 8.					

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB)				(LSB)			
Si	0	0	1	1	0	1	1
SYMBOL	POSITION	NAME AND DESCRIPTION					
Si	TAF.7	International Bit.					
0	TAF.6	Frame Alignment Signal Bit.					
0	TAF.5	Frame Alignment Signal Bit.					
1	TAF.4	Frame Alignment Signal Bit.					
1	TAF.3	Frame Alignment Signal Bit.					
0	TAF.2	Frame Alignment Signal Bit.					
1	TAF.1	Frame Alignment Signal Bit.					
1	TAF.0	Frame Alignment Signal Bit.					

TNAF: TRANSMIT NON-ALIGN FRAME REGISTER (Address=21 Hex)

(MSB)				(LSB)			
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
SYMBOL	POSITION	NAME AND DESCRIPTION					
Si	TNAF.7	International Bit.					
1	TNAF.6	Frame Non-Alignment Signal Bit.					
A	TNAF.5	Remote Alarm.					
Sa4	TNAF.4	Additional Bit 4.					



12.0 LINE INTERFACE CONTROL FUNCTION

The DS2143 can control line interface units that contain serial ports. When Control Register Bytes 1 or 2 (CRB1, CRB2) are written to, the DS2143 will automatically write this data serially (LSB first) into the line interface by creating a chip select, serial clock and serial data via the

LI_CS, LI_SCLK and LI_SDI pins respectively. This control function is driven off of the RCLK and it must be present for proper operation. Registers CRB1 and CRB2 can only be written to, they cannot be read from. Writes to these registers must be at least 20 μ s apart. See Section 13 for timing information.

CRB1: CONTROL REGISTER BYTE 1 (Address=18 Hex)

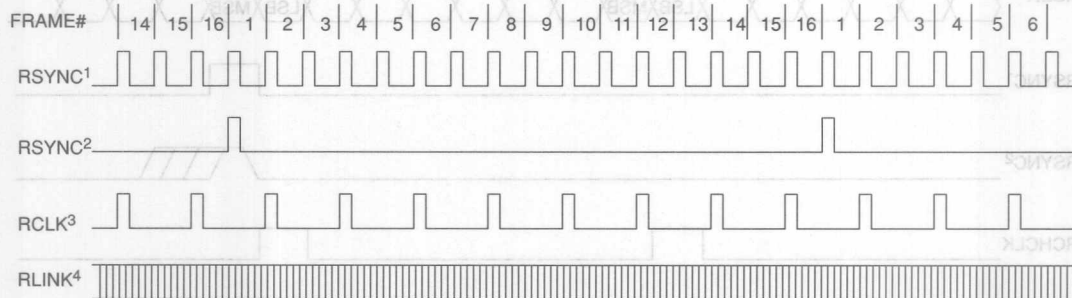
CRB2: CONTROL REGISTER BYTE 2 (Address=19 Hex)

(MSB)				(LSB)				
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	CRB1
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	CRB2

SYMBOL	POSITION	NAME AND DESCRIPTION
CR1	CRB1.0	LSB of Control Register Byte 1
CR7	CRB2.7	MSB of Control Register Byte 2

13.0 TIMING DIAGRAMS

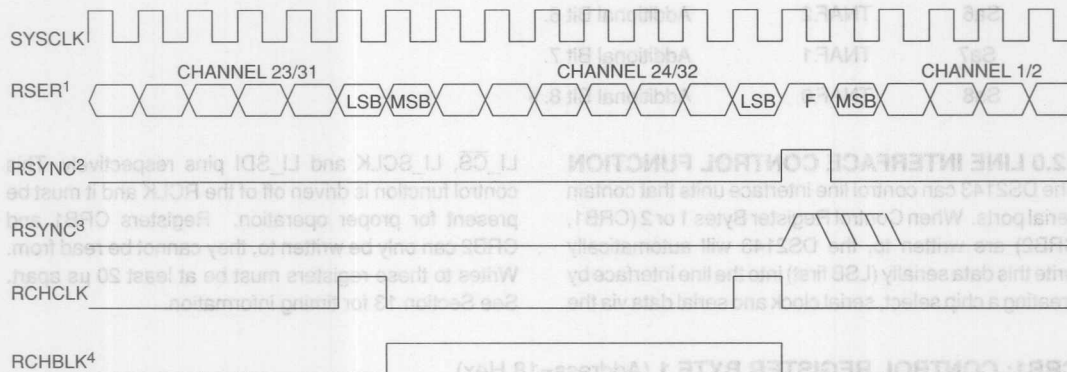
RECEIVE SIDE TIMING



NOTES:

1. RSYNC in the frame mode (RCR1.6=0).
2. RSYNC in the multiframe mode (RCR1.6=1).
3. RLCLK is programmed to output just the Sa4 bit.
4. RLINK will always output all five Sa bits as well as the rest of the receive data stream.
5. This diagram assumes the CAS MF begins with the FAS word.

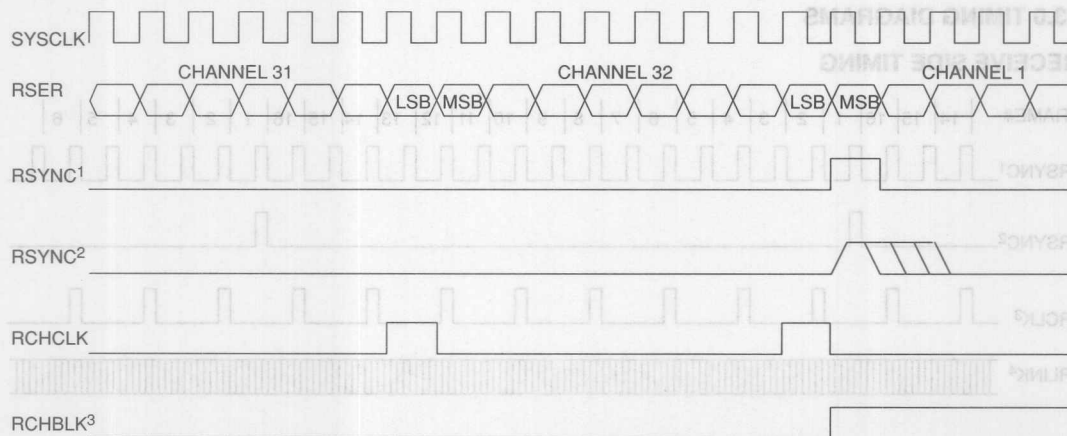
RECEIVE SIDE 1.544 MHZ BOUNDARY TIMING (WITH ELASTIC STORE ENABLED)



NOTES:

1. Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to one).
2. RSYNC is in the output mode (RCR1.5=0).
3. RSYNC is in the input mode (RCR1.5=1).
4. RCHBLK is programmed to block channel 24.

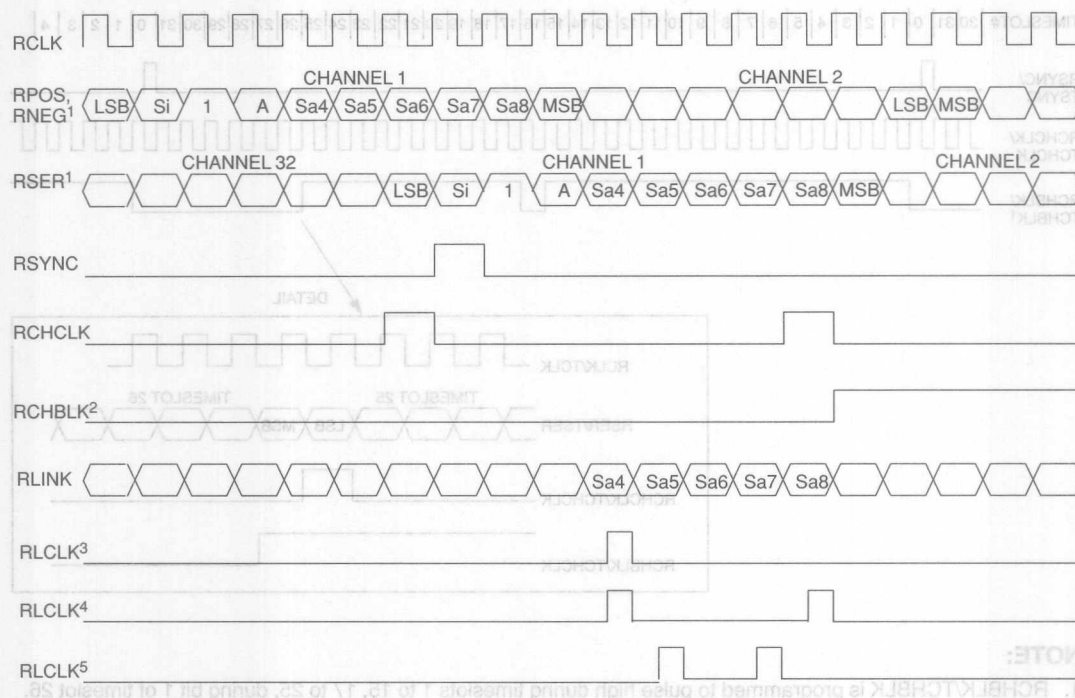
RECEIVE SIDE 2.048 MHZ BOUNDARY TIMING (WITH ELASTIC STORE ENABLED)



NOTES:

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RCHBLK is programmed to block channel 1.

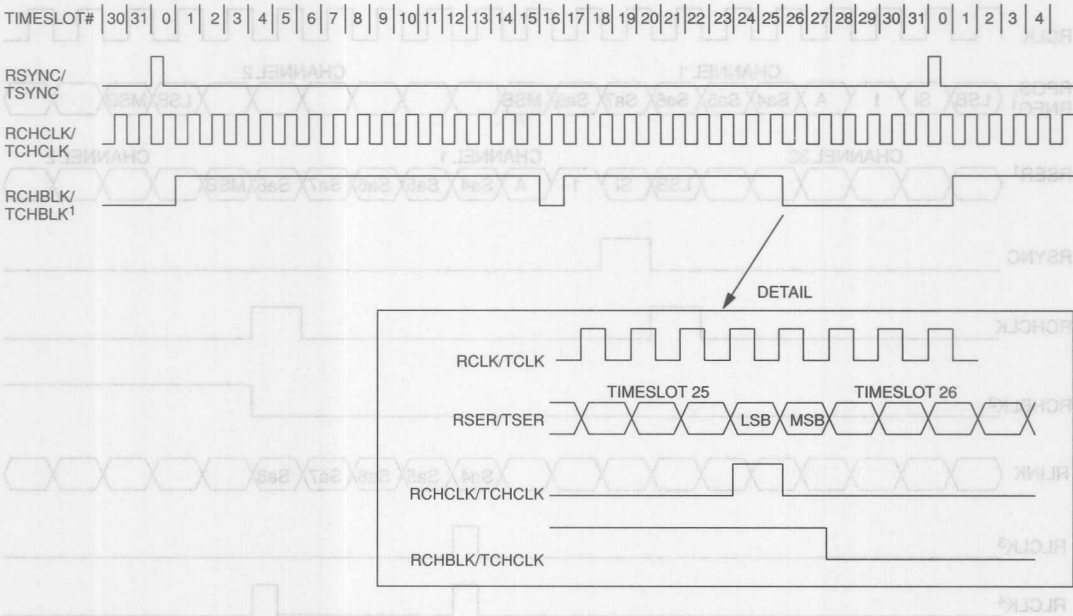
RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED)



NOTES:

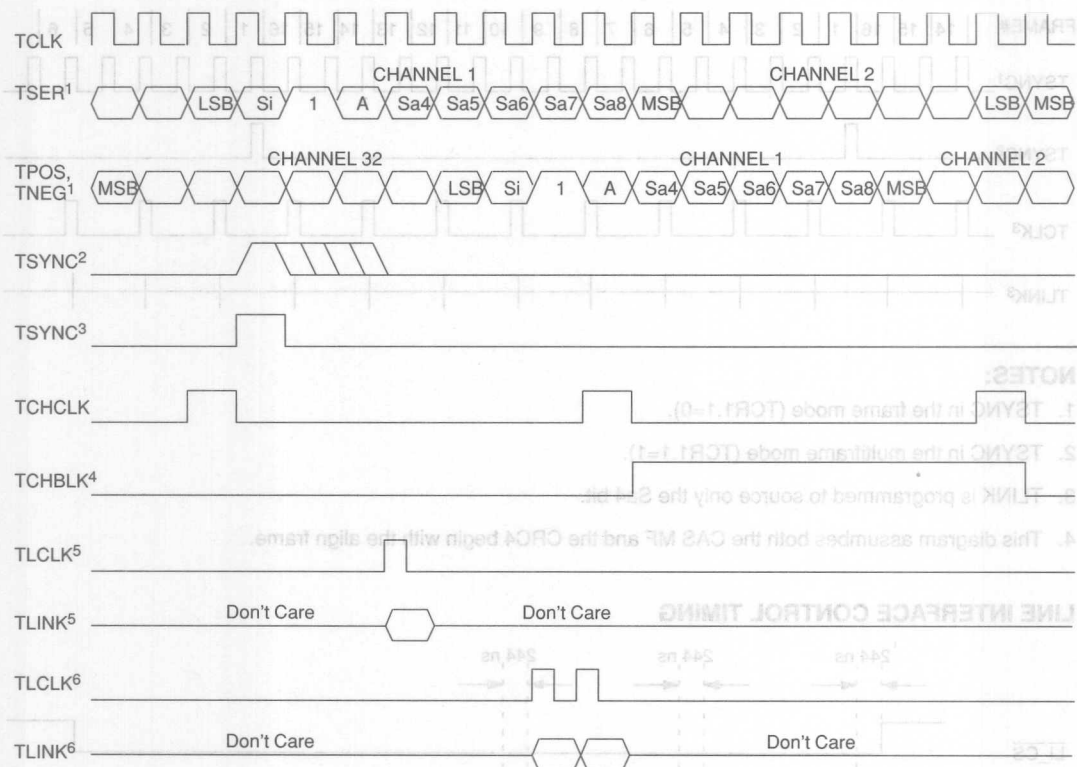
1. There is a 6 RCLK delay from RPOS, RNEG to RSER.
2. RCHBLK is programmed to block channel 2.
3. RLINK is programmed to output the Sa4 bits.
4. RLINK is programmed to output the Sa4 and Sa8 bits.
5. RLINK is programmed to output the Sa5 and Sa7 bits.
6. Shown is a non-align frame boundary.

G.802 TIMING



NOTE:

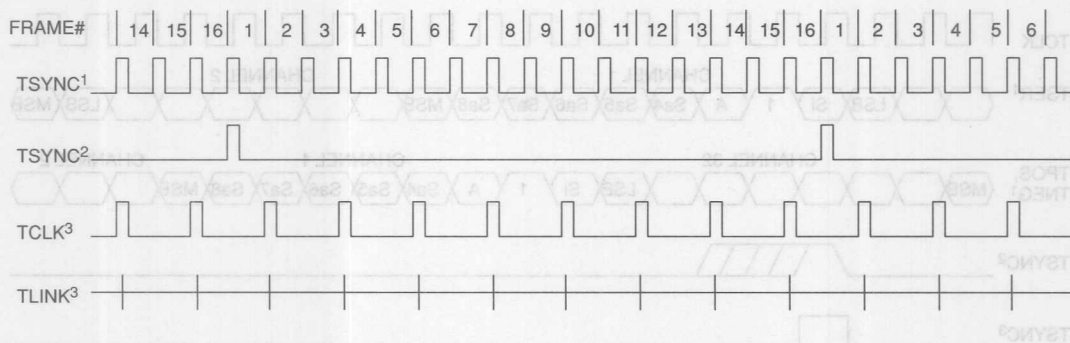
1. RCHBLK/TCHBLK is programmed to pulse high during timeslots 1 to 15, 17 to 25, during bit 1 of timeslot 26.



NOTES:

1. There is a 5 TCLK delay from TSER to TPOS, and TNEG.
2. TSYNC is in the input mode (TCR1.0=0).
3. TSYNC is in the output mode (TCR1.0=1).
4. TCHBLK is programmed to block channel 2.
5. TLINK is programmed to source the Sa4 bits.
6. TLINK is programmed to source the Sa7 and Sa8 bits.
7. Shown is a non-align frame boundary.

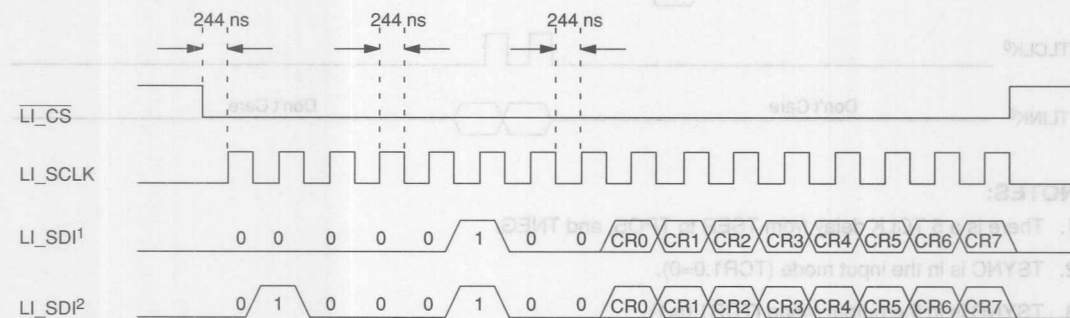
TRANSMIT SIDE TIMING



NOTES:

1. TSYNC in the frame mode (TCR1.1=0).
2. TSYNC in the multiframe mode (TCR1.1=1).
3. TLINK is programmed to source only the Sa4 bit.
4. This diagram assumes both the CAS MF and the CRC4 begin with the align frame.

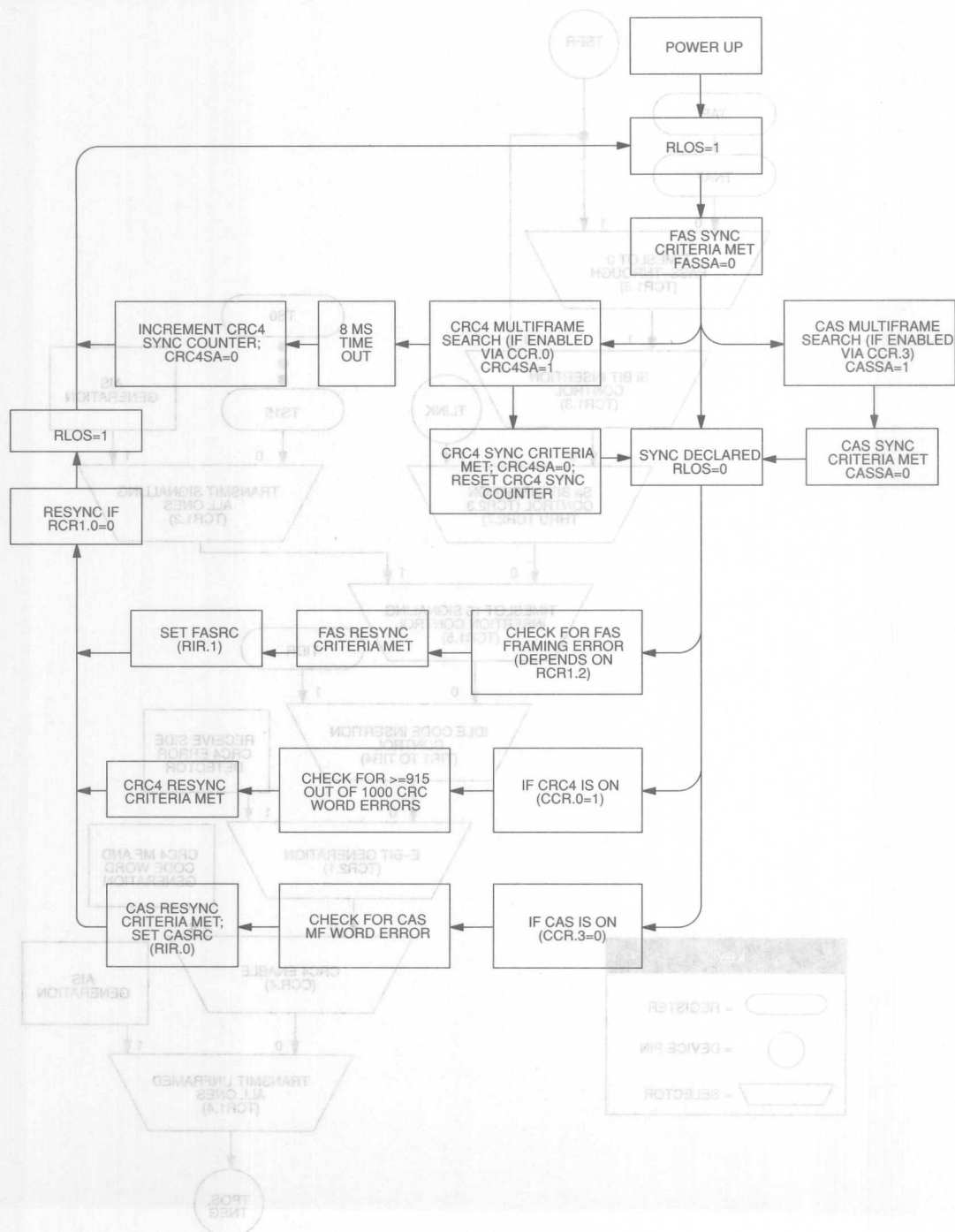
LINE INTERFACE CONTROL TIMING



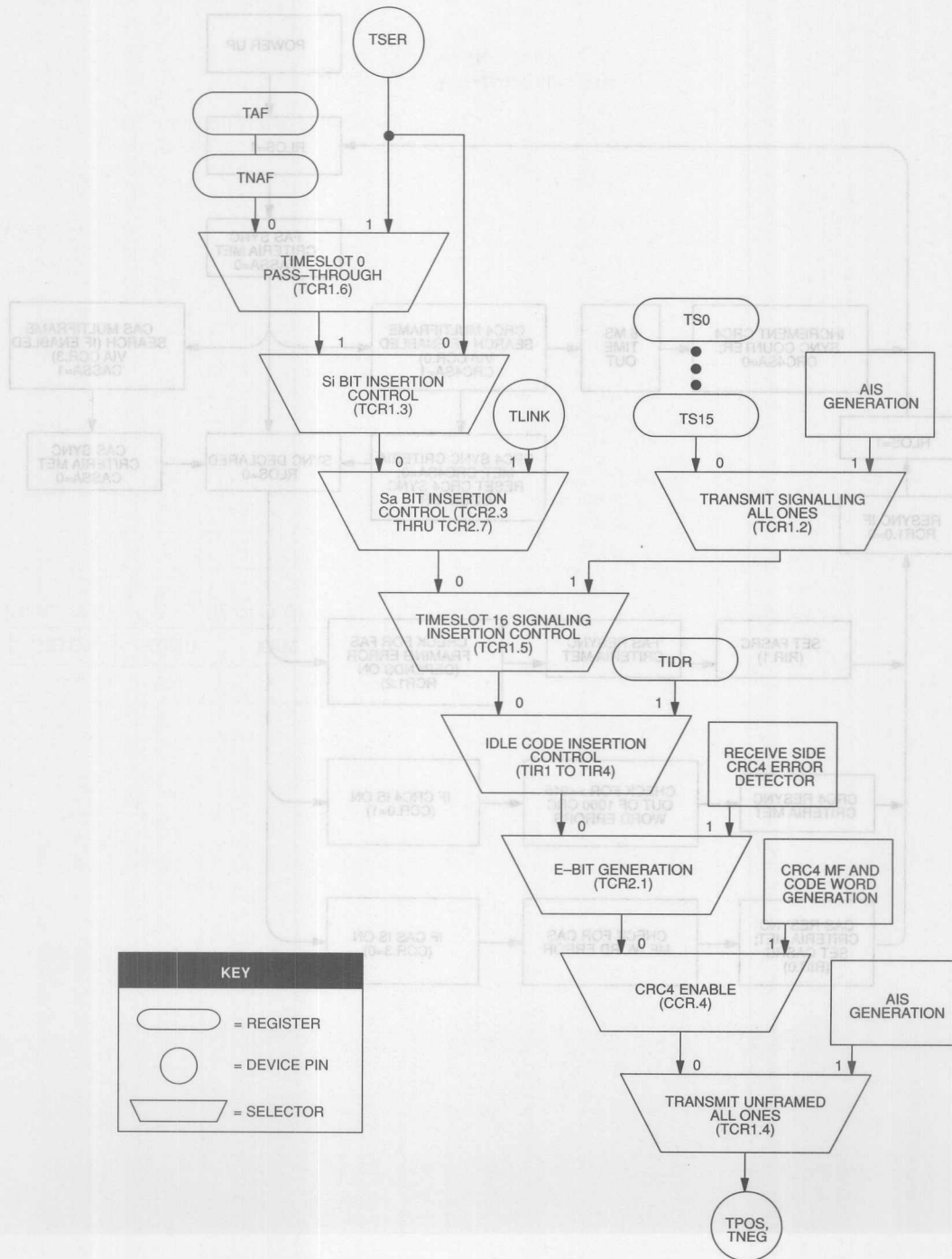
NOTES:

1. A write to CRB1 will cause the DS2143 to output this sequence.
2. A write to CRB2 will cause the DS2143 to output this sequence.
3. Timing numbers are based on RCLK=2.048 MHz with 50% duty cycle.

DS2143 SYNCHRONIZATION FLOWCHART



DS2143 TRANSMIT DATA FLOW



Operating Temperature
Storage Temperature
Soldering Temperature

0°C to +70°C
-55°C to 125°C
260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		10		mA	1
Input Leakage	I_{IL}	-1.0		+1.0	μA	2
Output Leakage	I_{LO}			1.0	μA	3
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

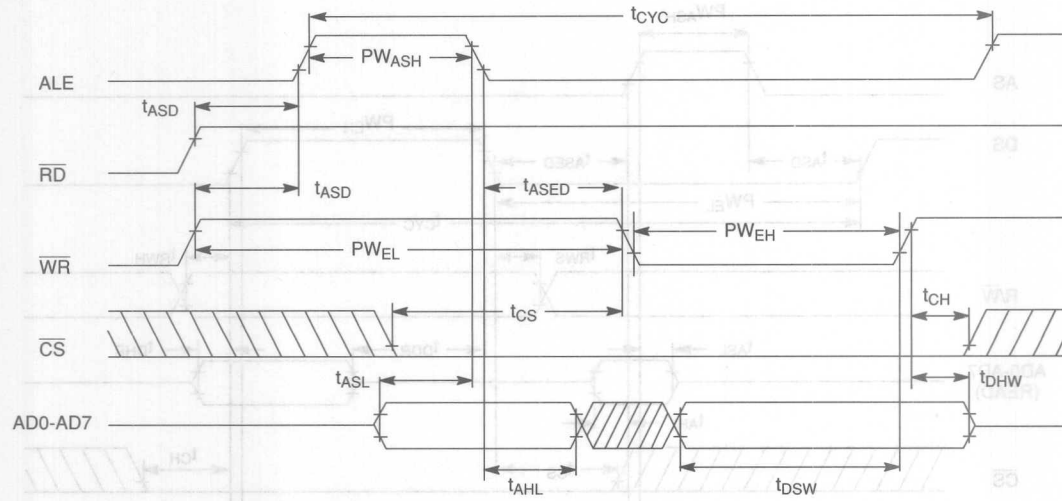
1. $RCLK = TCLK = 2.048 \text{ MHz}$; $V_{DD} = 5.5V$.
2. $0.0V < V_{IN} < V_{DD}$.
3. Applies to $\overline{INT1}$ and $\overline{INT2}$ when 3-stated.

AC CHARACTERISTICS - PARALLEL PORT (0°C to 70°C; V_{DD} = 5V ± 10%)

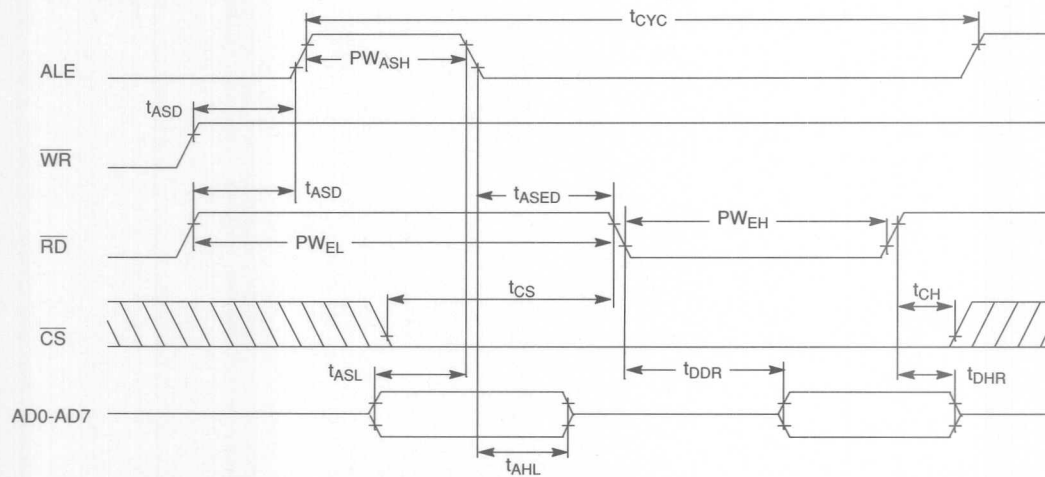
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t _{CYC}	250			ns	
Pulse Width, DS Low or $\overline{\text{RD}}$ High	PW _{EL}	150			ns	
Pulse Width, DS High or $\overline{\text{RD}}$ Low	PW _{EH}	100			ns	
Input Rise/Fall Times	t _R , t _F			30	ns	
R/ $\overline{\text{W}}$ Hold Time	t _{RWH}	10			ns	
R/ $\overline{\text{W}}$ Setup Time Before DS High	t _{RWS}	50			ns	
$\overline{\text{CS}}$ Setup Time Before DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$ active	t _{CS}	20			ns	
$\overline{\text{CS}}$ Hold Time	t _{CH}	0			ns	
Read Data Hold Time	t _{DHR}	10		50	ns	
Write Data Hold Time	t _{DHW}	0			ns	
Muxed Address Valid to AS or ALE fall	t _{ASL}	20			ns	
Muxed Address Hold Time	t _{AHL}	10			ns	
Delay Time DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$ to AS or ALE Rise	t _{ASD}	25			ns	
Pulse Width AS or ALE High	PW _{ASH}	40			ns	
Delay Time, AS or ALE to DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{ASED}	20			ns	
Output Data Delay Time from DS or $\overline{\text{RD}}$	t _{DDR}	20		100	ns	
Data Setup Time	t _{DSW}	80			ns	
	A _m					Output Current (2.4V)
	A _m					Output Current (0.4V)

NOTES:
1. RCLK = TCLK = 2.048 MHz; V_{DD} = 2.5V
2. 0.0V < V_{in} < V_{DD}
3. Applies to INT1 and INT2 when 3-state

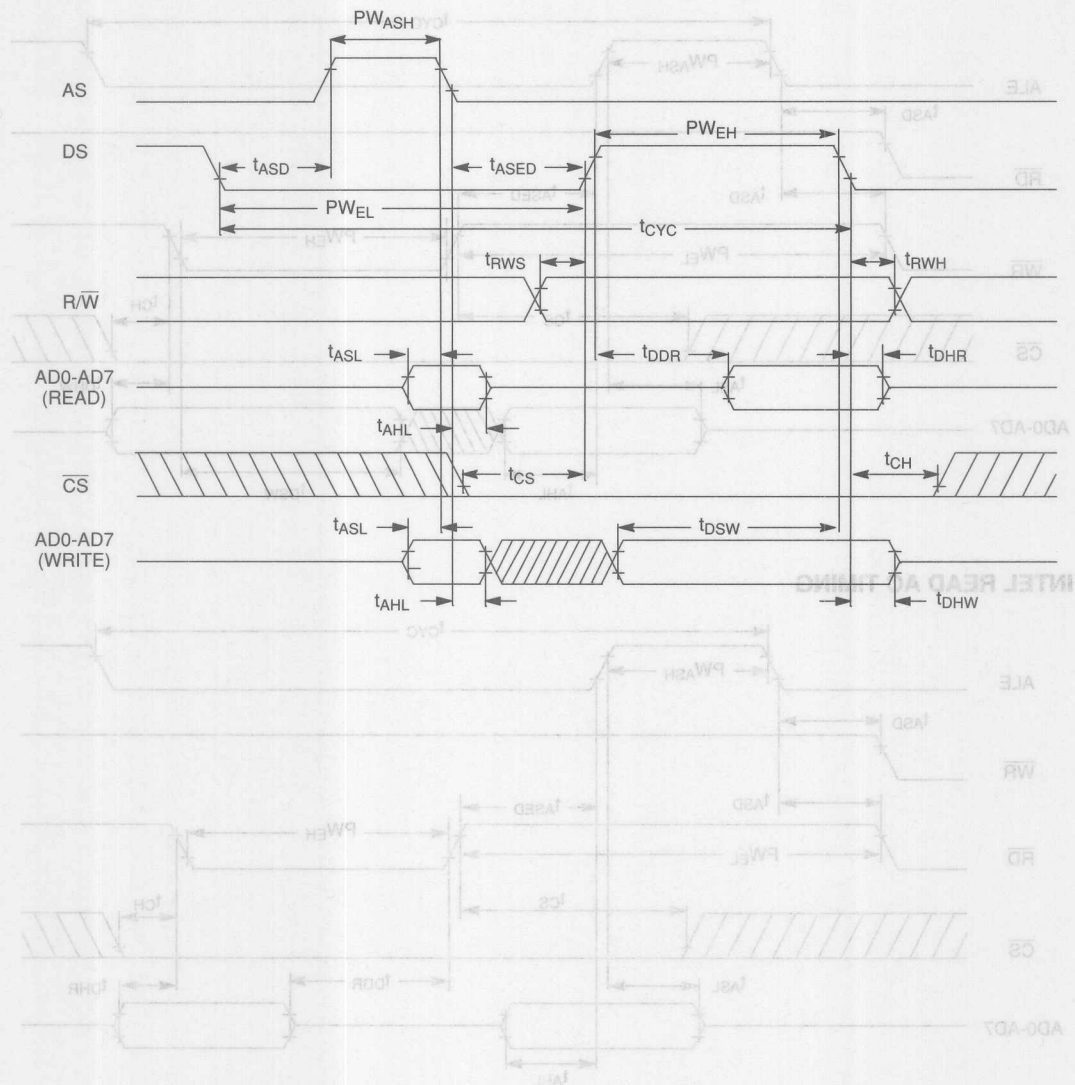
INTEL WRITE AC TIMING



INTEL READ AC TIMING



MOTOROLA AC TIMING



AC CHARACTERISTICS – TRANSMIT SIDE(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P		488		ns	
TCLK Pulse Width	t_{CH}	50			ns	
	t_{CL}	50			ns	
TSER, TSYNC, TLINK Setup to TCLK Falling	t_{SU}	25			ns	
TSER, TSYNC, TLINK Hold from TCLK Falling	t_{HD}	25			ns	
TCLK Rise/Fall Times	t_R, t_F			25	ns	
Data Delay	t_{DD}			50	ns	

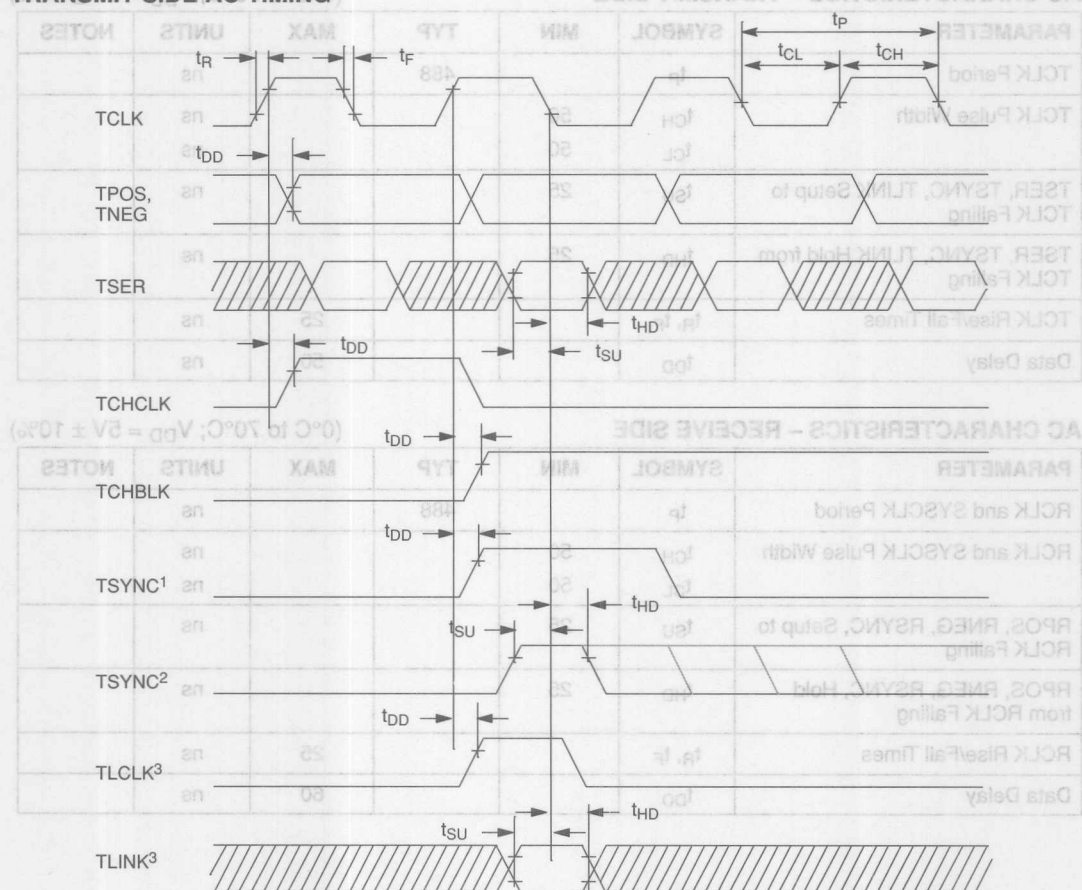
AC CHARACTERISTICS – RECEIVE SIDE(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK and SYSCLK Period	t_P		488		ns	
RCLK and SYSCLK Pulse Width	t_{CH}	50			ns	
	t_{CL}	50			ns	
RPOS, RNEG, RSYNC, Setup to RCLK Falling	t_{SU}	25			ns	
RPOS, RNEG, RSYNC, Hold from RCLK Falling	t_{HD}	25			ns	
RCLK Rise/Fall Times	t_R, t_F			25	ns	
Data Delay	t_{DD}			60	ns	

NOTES:

1. TSYNC is in the output mode (TCR1 0=1).
2. TSYNC is in the input mode (TCR1 0=0).
3. No timing relationship between TSYNC and TCLK/TLINK is implied.

TRANSMIT SIDE AC TIMING

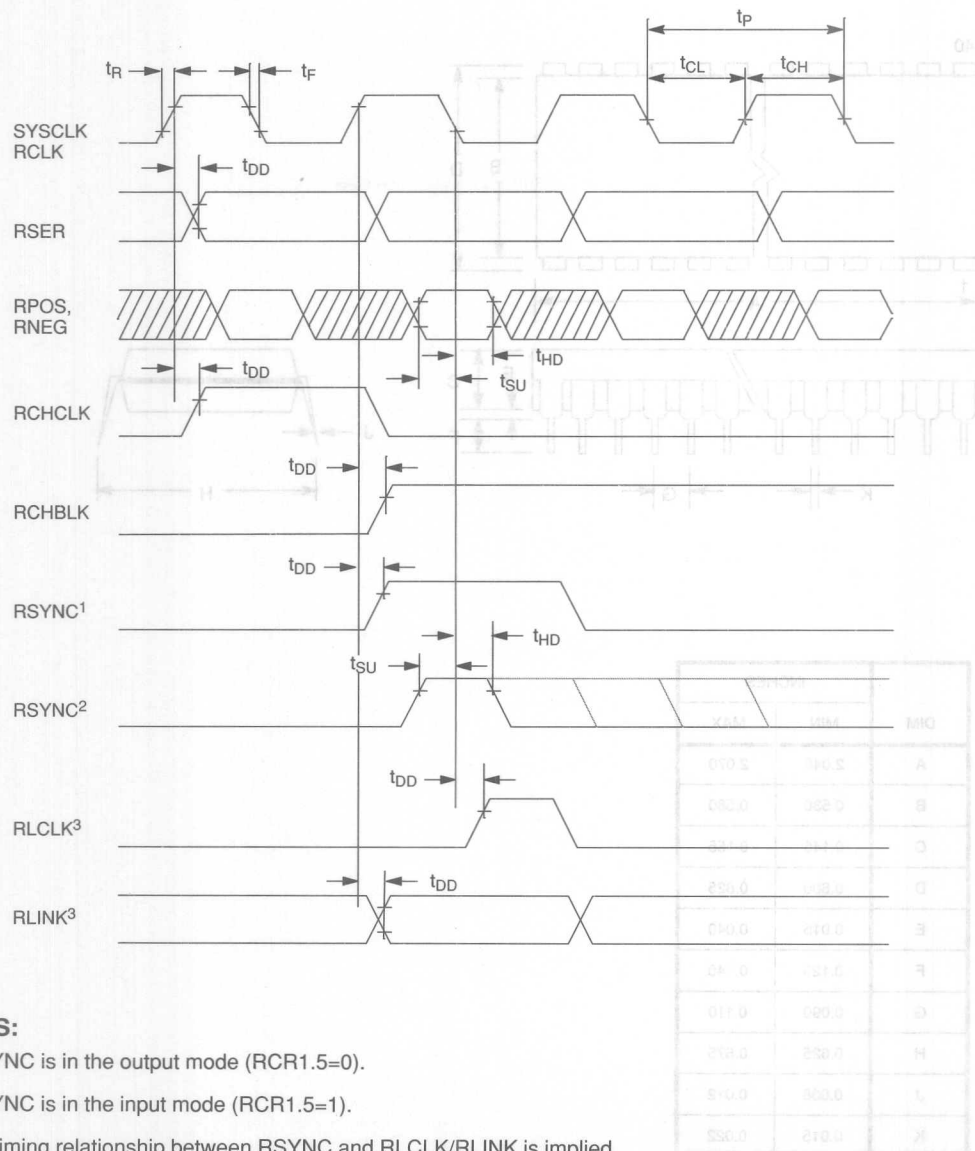


NOTES:

1. TSYNC is in the output mode (TCR1.0=1).
2. TSYNC is in the input mode (TCR1.0=0).
3. No timing relationship between TSYNC and TLCLK/TLINK is implied.

RECEIVE SIDE AC TIMING

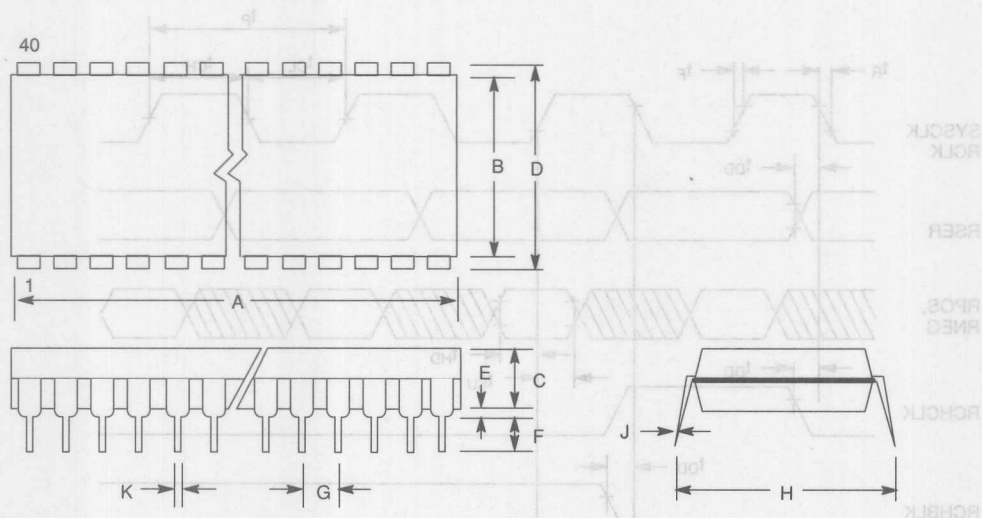
DS2143 E1 CONTROLLER (600 MIL 40-PIN DIP)



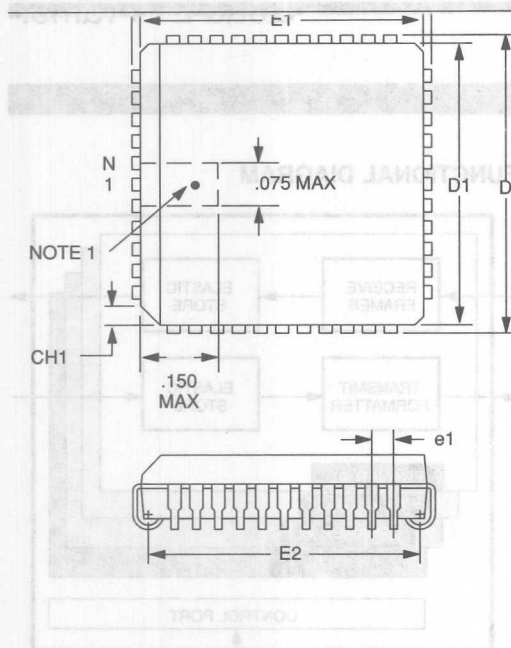
NOTES:

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. No timing relationship between RSYNC and RLCLK/RLINK is implied.

DS2143 E1 CONTROLLER (600 MIL) 40-PIN DIP

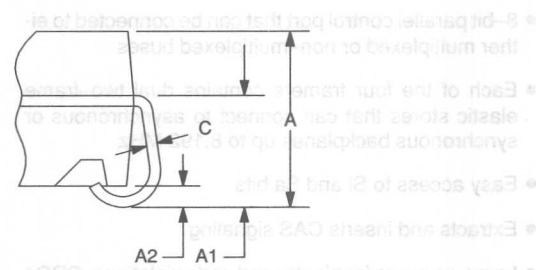
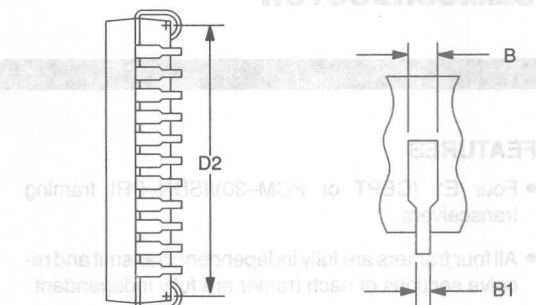


DIM	INCHES	
	MIN	MAX
A	2.040	2.070
B	0.530	0.560
C	0.145	0.155
D	0.600	0.625
E	0.015	0.040
F	0.120	0.140
G	0.090	0.110
H	0.625	0.675
J	0.008	0.012
K	0.015	0.022



NOTE1: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	—



- Available in 128-pin TQFP
- 8V supply low power CMOS
- Pin compatible with DS21C04B Quad T1 Transceiver
- Detects and generates AIS, remote alarm, and remote multistate alarm
- Programmable output clock for fractional E1, per channel lookahead, H0 and H1 applications
- Large counters for digital and code violations, CRC4 code word error, FAR word error, and E-bits
- Extracts and inserts CAS signaling
- Easy access to SI and SD bits
- Synchronous backplane up to 6.75 Mbit/s
- Elastic stores that can connect to synchronous or asynchronous buses
- Each of the four frames can connect to synchronous or asynchronous buses
- 8-bit parallel control port that can be connected to either multiplexed or non-multiplexed buses
- Frames to FAR, CAS, CDS, and CRC4 formats
- All functions are fully independent and retransmission of each frame is independent
- Four E1 channels or PCM-30/23B framing

DESCRIPTION

The DS21C43A combines four of the popular DS2143 E1 Transceivers into a single monolithic device. The "A" designation denotes that some new features are available in the Quad version that were not available in the single E1 device. The added features in the DS21C43A are listed in Section 1. The DS21C43A offers a substantial space savings to applications that require more than one E1 transceiver on a card. The Quad version is only slightly bigger than the single E1 device. All four transceivers are fully independent and retransmission of each frame is independent.

DS21Q43A

Quad E1 Framer

FUNCTIONAL DIAGRAM

-
- The diagram illustrates the Elastic Store architecture. It features a central data path with four main components: a RECEIVE FRAMER, an ELASTIC STORE, another ELASTIC STORE, and a TRANSMIT FORMATTER. Data enters from the left, passes through the RECEIVE FRAMER, then the first ELASTIC STORE, and then the TRANSMIT FORMATTER before exiting to the left. A CONTROL PORT at the bottom has an upward arrow pointing to the first ELASTIC STORE. On the left side, four overlapping gray rectangles represent FRAMER #0, FRAMER #1, FRAMER #2, and FRAMER #3, stacked vertically.

ACTUAL SIZE

Q43A

QUAD
T1
FRAMER

ers in the DS21Q43A are totally independent, they do not share a common framing synchronizer. Also, the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The DS21Q43A meets all of the latest specifications including CCITT/ITU G.704, G.706, G.962, and I.431 as well as ETS 300 011 and ETS 300 233.

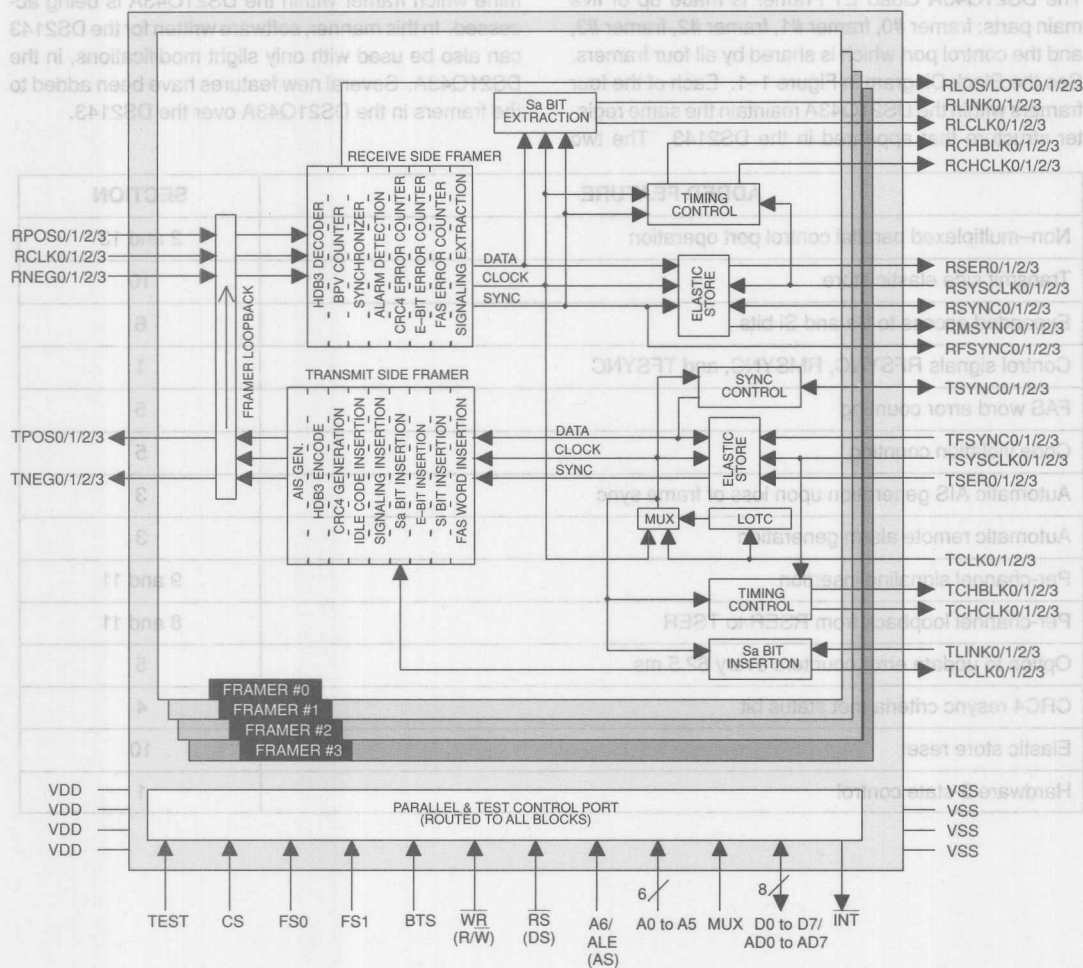
1.0 INTRODUCTION

The DS21Q43A Quad E1 Framer is made up of five main parts: framer #0, framer #1, framer #2, framer #3, and the control port which is shared by all four framers. See the Block Diagram in Figure 1–1. Each of the four framers within the DS21Q43A maintain the same register structure that appeared in the DS2143. The two

framer select inputs (FS0 and FS1) are used to determine which framer within the DS21Q43A is being accessed. In this manner, software written for the DS2143 can also be used with only slight modifications, in the DS21Q43A. Several new features have been added to the framers in the DS21Q43A over the DS2143.

ADDED FEATURE	SECTION
Non-multiplexed parallel control port operation	2 and 13
Transmit side elastic store	10
Expanded access to Sa and Si bits	6
Control signals RFSYNC, RMSYNC, and TFSYNC	1
FAS word error counting	5
Code violation counting	5
Automatic AIS generation upon loss of frame sync	3
Automatic remote alarm generation	3
Per-channel signaling insertion	9 and 11
Per-channel loopback from RSER to TSER	8 and 11
Option to update error counters every 62.5 ms	5
CRC4 resync criteria met status bit	4
Elastic store reset	10
Hardware 3-state control	1

DS21Q43A BLOCK DIAGRAM Figure 1-1

**READER'S NOTE**

This data sheet assumes a particular nomenclature of the E1 operating environment. There are 32 eight-bit timeslots in an E1 systems which are number 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to chan-

nel 1, timeslot 1 is identical to channel 2, and so on. Each timeslot (or channel) is made up of eight bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment	CRC4	Cyclical Redundancy Check
CAS	Channel Associated Signaling	CCS	Common Channel Signaling
MF	Multiframe	Sa	Additional bits
Si	International bits	E-bit	CRC4 Error bits

TRANSMIT PIN LIST Table 1-1

PIN	SYMBOL	TYPE	DESCRIPTION
19	TCLK0	I	Transmit Clock for Framer 0.
53	TCLK1	I	Transmit Clock for Framer 1.
87	TCLK2	I	Transmit Clock for Framer 2.
113	TCLK3	I	Transmit Clock for Framer 3.
126	TSER0	I	Transmit Serial Data for Framer 0.
32	TSER1	I	Transmit Serial Data for Framer 1.
66	TSER2	I	Transmit Serial Data for Framer 2.
92	TSER3	I	Transmit Serial Data for Framer 3.
128	TCHCLK0	O	Transmit Channel Clock from Framer 0.
34	TCHCLK1	O	Transmit Channel Clock from Framer 1.
68	TCHCLK2	O	Transmit Channel Clock from Framer 2.
94	TCHCLK3	O	Transmit Channel Clock from Framer 3.
1	TCHBLK0	O	Transmit Channel Block from Framer 0.
35	TCHBLK1	O	Transmit Channel Block from Framer 1.
69	TCHBLK2	O	Transmit Channel Block from Framer 2.
95	TCHBLK3	O	Transmit Channel Block from Framer 3.
20	TLCLK0	O	Transmit Link Clock from Framer 0.
54	TLCLK1	O	Transmit Link Clock from Framer 1.
88	TLCLK2	O	Transmit Link Clock from Framer 2.
114	TLCLK3	O	Transmit Link Clock from Framer 3.
22	TLINK0	I	Transmit Link Data for Framer 0.
56	TLINK1	I	Transmit Link Data for Framer 1.
90	TLINK2	I	Transmit Link Data for Framer 2.
116	TLINK3	I	Transmit Link Data for Framer 3.
2	TPOS0	O	Transmit Bipolar Data from Framer 0.
36	TPOS1	O	Transmit Bipolar Data from Framer 1.
70	TPOS2	O	Transmit Bipolar Data from Framer 2.
96	TPOS3	O	Transmit Bipolar Data from Framer 3.
3	TNEG0	O	Transmit Bipolar Data from Framer 0.
37	TNEG1	O	Transmit Bipolar Data from Framer 1.
71	TNEG2	O	Transmit Bipolar Data from Framer 2.
97	TNEG3	O	Transmit Bipolar Data from Framer 3.

PIN	SYMBOL	TYPE	DESCRIPTION
21	TSYNC0	I/O	Transmit Sync for Framer 0.
55	TSYNC1	I/O	Transmit Sync for Framer 1.
89	TSYNC2	I/O	Transmit Sync for Framer 2.
115	TSYNC3	I/O	Transmit Sync for Framer 3.
127	TFSYNC0	I	Transmit Sync for Elastic Store in Framer 0.
33	TFSYNC1	I	Transmit Sync for Elastic Store in Framer 1.
67	TFSYNC2	I	Transmit Sync for Elastic Store in Framer 2.
93	TFSYNC3	I	Transmit Sync for Elastic Store in Framer 3.
125	TSYSCLK0	I	Transmit System Clock for Elastic Store in Framer 0.
31	TSYSCLK1	I	Transmit System Clock for Elastic Store in Framer 1.
65	TSYSCLK2	I	Transmit System Clock for Elastic Store in Framer 2.
91	TSYSCLK3	I	Transmit System Clock for Elastic Store in Framer 3.

RECEIVE PIN LIST Table 1–2

PIN	SYMBOL	TYPE	DESCRIPTION
6	RCLK0	I	Receive Clock for Framer 0.
40	RCLK1	I	Receive Clock for Framer 1.
74	RCLK2	I	Receive Clock for Framer 2.
100	RCLK3	I	Receive Clock for Framer 3.
13	RSER0	O	Receive Serial Data from Framer 0.
49	RSER1	O	Receive Serial Data from Framer 1.
83	RSER2	O	Receive Serial Data from Framer 2.
107	RSER3	O	Receive Serial Data from Framer 3.
9	RCHCLK0	O	Receive Channel Clock from Framer 0.
43	RCHCLK1	O	Receive Channel Clock from Framer 1.
77	RCHCLK2	O	Receive Channel Clock from Framer 2.
103	RCHCLK3	O	Receive Channel Clock from Framer 3.
10	RCHBLK0	O	Receive Channel Block from Framer 0.
44	RCHBLK1	O	Receive Channel Block from Framer 1.
80	RCHBLK2	O	Receive Channel Block from Framer 2.
104	RCHBLK3	O	Receive Channel Block from Framer 3.
5	RLCLK0	O	Receive Link Clock from Framer 0.
39	RLCLK1	O	Receive Link Clock from Framer 1.
73	RLCLK2	O	Receive Link Clock from Framer 2.

PIN	SYMBOL	TYPE	DESCRIPTION
99	RLCLK3	O	Receive Link Clock from Framer 3.
4	RLINK0	O	Receive Link Data from Framer 0.
38	RLINK1	O	Receive Link Data from Framer 1.
72	RLINK2	O	Receive Link Data from Framer 2.
98	RLINK3	O	Receive Link Data from Framer 3.
8	RPOS0	I	Receive Bipolar Data for Framer 0.
42	RPOS1	I	Receive Bipolar Data for Framer 1.
76	RPOS2	I	Receive Bipolar Data for Framer 2.
102	RPOS3	I	Receive Bipolar Data for Framer 3.
7	RNEG0	I	Receive Bipolar Data for Framer 0.
41	RNEG1	I	Receive Bipolar Data for Framer 1.
75	RNEG2	I	Receive Bipolar Data for Framer 2.
101	RNEG3	I	Receive Bipolar Data for Framer 3.
12	RSYNC0	I/O	Receive Sync for Framer 0.
48	RSYNC1	I/O	Receive Sync for Framer 1.
82	RSYNC2	I/O	Receive Sync for Framer 2.
106	RSYNC3	I/O	Receive Sync for Framer 3.
17	RFSYNC0	O	Receive Frame Sync from Framer 0.
51	RFSYNC1	O	Receive Frame Sync from Framer 1.
85	RFSYNC2	O	Receive Frame Sync from Framer 2.
109	RFSYNC3	O	Receive Frame Sync from Framer 3.
16	RMSYNC0	O	Receive Multiframe Sync from Framer 0.
50	RMSYNC1	O	Receive Multiframe Sync from Framer 1.
84	RMSYNC2	O	Receive Multiframe Sync from Framer 2.
108	RMSYNC3	O	Receive Multiframe Sync from Framer 3.
11	RSYSCLK0	I	Receive System Clock for Elastic Store in Framer 0.
45	RSYSCLK1	I	Receive System Clock for Elastic Store in Framer 1.
81	RSYSCLK2	I	Receive System Clock for Elastic Store in Framer 2.
105	RSYSCLK3	I	Receive System Clock for Elastic Store in Framer 3.
18	RLOS/LOT0	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 0.
52	RLOS/LOT1	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 1.
86	RLOS/LOT2	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 2.
112	RLOS/LOT3	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 3.

CONTROL PORT/TEST/SUPPLY PIN LIST Table 1–3

PIN	SYMBOL	TYPE	DESCRIPTION
57	TEST	I	3-State Control for all Output and I/O Pins.
60	CS	I	Chip Select.
58	FS0	I	Framer Select 0 for Parallel Control Port.
59	FS1	I	Framer Select 1 for Parallel Control Port.
61	BTS	I	Bus Type Select for Parallel Control Port.
63	WR(R/W)	I	Write Input (Read/Write).
62	$\overline{RS}(\overline{DS})$	I	Read Input (Data Strobe).
23	A0	I	Address Bus Bit 0; LSB.
24	A1	I	Address Bus Bit 1.
25	A2	I	Address Bus Bit 2.
26	A3	I	Address Bus Bit 3.
27	A4	I	Address Bus Bit 4.
28	A5	I	Address Bus Bit 5.
29	A6 OR ALE (AS)	I	Address Bus Bit 6; MSB or Address Latch Enable (Address Strobe).
30	INT	O	Receive Alarm Interrupt for all Four Framers.
64	MUX	I	Non-Multiplexed or Multiplexed Bus select.
117	D0 or AD0	I/O	Data Bus Bit 0 or Address/Data Bus Bit 0; LSB.
118	D1 or AD1	I/O	Data Bus Bit 1 or Address/Data Bus Bit 1.
119	D2 or AD2	I/O	Data Bus Bit 2 or Address/Data Bus Bit 2.
120	D3 or AD3	I/O	Data Bus Bit 3 or Address/Data Bus Bit 3.
121	D4 or AD4	I/O	Data Bus Bit 4 or Address/Data Bus Bit 4.
122	D5 or AD5	I/O	Data Bus Bit 5 or Address/Data Bus Bit 5.
123	D6 or AD6	I/O	Data Bus Bit 6 or Address/Data Bus Bit 6.
124	D7 or AD7	I/O	Data Bus Bit 7 or Address/Data Bus Bit 7; MSB.
15	V _{DD}	–	Positive Supply Voltage.
47	V _{DD}	–	Positive Supply Voltage.
79	V _{DD}	–	Positive Supply Voltage.
111	V _{DD}	–	Positive Supply Voltage.
14	V _{SS}	–	Signal Ground.
46	V _{SS}	–	Signal Ground.
78	V _{SS}	–	Signal Ground.
110	V _{SS}	–	Signal Ground.

DS21Q43A PIN DESCRIPTION Table 1–4

Transmit Clock [TCLK]. 2.048 MHz primary clock. Used to clock data through the transmit side formatter.

Transmit Serial Data [TSER]. Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Transmit Channel Clock [TCHCLK]. 256 KHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data. See Section 11 for timing details.

Transmit Bipolar Data [TPOS and TNEG]. Updated on rising edge of TCLK. Can be programmed to output NRZ data on TPOS via the TCR1.7 control bit.

Transmit Channel Block [TCHBLK]. A user programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384Kbps service (H0), 1920Kbps (H12), or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 11 for timing details.

Transmit System Clock [TSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store.

Transmit Link Clock [TLCLK]. 4 KHz to 20 KHz demand clock for the TLINK input. Controlled by TCR2. See Section 11 for timing details.

Transmit Link Data [TLINK]. If enabled via TCR2, this pin will be sampled on the falling edge of TCLK to insert data into the Sa bit positions. See Section 11 for timing details.

Transmit Sync [TSYNC]. A pulse at this pin will establish either frame or multiframe boundaries for the DS21Q43A. Via TCR1.1, the DS21Q43A can be programmed to output either a frame or multiframe pulse at this pin. See Section 11 for timing details.

Transmit Frame Sync [TFSYNC]. 8 KHz pulse. Only used when the transmit side elastic store is enabled. A pulse at this pin will establish frame boundaries for the DS21Q43A. Should be tied low in applications that do not use the transmit side elastic store. See Section 11 for timing details.

Receive Link Data [RLINK]. Updated with full received E1 data stream on the rising edge of RCLK. See Section 11 for timing details.

Receive Link Clock [RLCLK]. 4 KHz to 20 KHz demand clock for the RLINK output. Controlled by RCR2. See Section 11 for timing details.

Receive Clock [RCLK]. 2.048 MHz primary clock. Used to clock data through the receive side of the framer.

Receive Channel Clock [RCHCLK]. 256 KHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data. See Section 11 for timing details.

Receive Channel Block [RCHBLK]. A user programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with RCLK when the transmit side elastic store is disabled. Synchronous with RSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384Kbps service (H0), 1920Kbps (H12), or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 11 for timing details.

Receive Serial Data [RSER]. Received NRZ serial data. Updated on rising edges of RCLK when the

receive side elastic store is disabled. Updated on the rising edges of RSYCLK when the receive side elastic store is enabled. Should be tied low in applications that do not use the elastic store.

Receive Sync [RSYNC]. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR1.6=0) or multiframe boundaries (RCR1.6=1). If the receive side elastic store is enabled via RCR2.1, then this pin can be enabled to be an input at which a frame boundary pulse is applied. See Section 11 for timing details.

Receive Frame Sync [RFSYNC]. An extracted 8 KHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries. See Section 11 for timing details.

Receive Multiframe Sync [RMSYNC]. Only used when the receive side elastic store is enabled. An extracted pulse, one RSYCLK wide, is output at this pin which identifies either CAS or CRC4 multiframe boundaries. If the receive side elastic store is disabled, then this output should be ignored. See Section 11 for timing details.

Receive Bipolar Data Inputs [RPOS and RNEG]. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.

Receive System Clock [RSYCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store.

Receive Loss of Sync/Loss of Transmit Clock [RLOS/LOTCL]. A dual function output. If CCR1.6=0, then this pin will toggle high when the synchronizer is searching for the E1 frame or multiframe. If TCR2.0=1, then this pin will toggle high the TCLK pin has not been toggled for 5 μ s.

Receive Alarm Interrupt [INT]. Flags host controller during conditions defined in the Status Registers of the four framers. User can poll the Interrupt Status Register (ISR) to determine which status register in which framer is active (if any). Active low, open drain output.

3-State Control [TEST]. Set high to 3-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.

Bus Operation [MUX]. Set low to select non-multiplexed bus operation. Set high to select multiplexed bus operation.

Data Bus [D0 to D7] or Address/Data Bus [AD0 to AD7]. In non-multiplexed bus operation (MUX=0), serves as the data bus. In multiplexed bus operation (MUX=1), serves as a 8-bit multiplexed address/data bus.

Address Bus [A0 to A5]. In non-multiplexed bus operation (MUX=0), serves as the address bus. In multiplexed bus operation (MUX=1), these pins are not used and should be tied low.

Bus Type Select [BTS]. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD(DS), ALE(AS), and WR(R/W) pins. If BTS=1, then these pins assume the function listed in parenthesis.

Read Input [RD] (Data Strobe [DS]).

Framer Selects [FS0 and FS1]. Selects which of the four framers to be accessed.

Chip Selects [CS]. Must be low to read or write any of the four framers.

A6 or Address Latch Enable [ALE] (Address Strobe [AS]). In non-multiplexed bus operation (MUX=0), serves as the upper address bit. In multiplexed bus operation (MUX=1), serves to demultiplex the bus on a positive-going edge.

Write Input [WR] (Read/Write [R/W]).

Positive Supply [VDD]. 5.0 volts \pm 0.5volts.

Signal Ground [VSS]. 0.0 volts.

DS21Q43A FRAMER DECODE Table 1–5

FS1	FS0	FRAMER ACCESSED
0	0	#0
0	1	#1
1	0	#2
1	1	#3

DS21Q43A REGISTER MAP Table 1–6

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
00	R	BPV or Code Violation Count 1	06	R	Status 1.
01	R	BPV or Code Violation Count 2	07	R	Status 2.
02	R	CRC4 Count 1/FAS Error Count 1	08	R/W	Receive Information.
03	R	CRC4 Error Count 2	09 to 0A	–	Not Used.
04	R	E-Bit Count 1/FAS Error Count 2	(2)	R	Interrupt Status Register.
05	R	E-Bit Count 2			
10	R/W	Receive Control 1	20	R/W	Transmit Align Frame.
11	R/W	Receive Control 2	21	R/W	Transmit Non-Align Frame.
12	R/W	Transmit Control 1	22	R/W	Transmit Channel Blocking 1.
13	R/W	Transmit Control 2	23	R/W	Transmit Channel Blocking 2.
14	R/W	Common Control 1	24	R/W	Transmit Channel Blocking 3.
15	R/W	Test 1	25	R/W	Transmit Channel Blocking 4.
16	R/W	Interrupt Mask	26	R/W	Transmit Idle 1.
17	R/W	Interrupt Mask	27	R/W	Transmit Idle 2.
18	R/W	Test 3	28	R/W	Transmit Idle 3.
19	R/W	Test 2	29	R/W	Transmit Idle 4.
1A	R/W	Common Control 2	2A	R/W	Transmit Idle Definition.
1B	R/W	Common Control 3	2B	R/W	Receive Channel Blocking 1.
1C	R/W	Transmit Sa Control Register	2C	R/W	Receive Channel Blocking 2.
1D	–	Not Used	2D	R/W	Receive Channel Blocking 3.
1E	R	Synchronizer Status	2E	R/W	Receive Channel Blocking 4.
1F	R	Receive Non-Align Frame	2F	R/W	Receive Align Frame.
30	R	Receive Signaling 1	40	R/W	Transmit Signaling 1.
31	R	Receive Signaling 2	41	R/W	Transmit Signaling 2.
32	R	Receive Signaling 3	42	R/W	Transmit Signaling 3.

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
33	R	Receive Signaling 4	43	R/W	Transmit Signaling 4.
34	R	Receive Signaling 5	44	R/W	Transmit Signaling 5.
35	R	Receive Signaling 6	45	R/W	Transmit Signaling 6.
36	R	Receive Signaling 7	46	R/W	Transmit Signaling 7.
37	R	Receive Signaling 8	47	R/W	Transmit Signaling 8.
38	R	Receive Signaling 9	48	R/W	Transmit Signaling 9.
39	R	Receive Signaling 10	49	R/W	Transmit Signaling 10.
3A	R	Receive Signaling 11	4A	R/W	Transmit Signaling 11.
3B	R	Receive Signaling 12	4B	R/W	Transmit Signaling 12.
3C	R	Receive Signaling 13	4C	R/W	Transmit Signaling 13.
3D	R	Receive Signaling 14	4D	R/W	Transmit Signaling 14.
3E	R	Receive Signaling 15	4E	R/W	Transmit Signaling 15.
3F	R	Receive Signaling 16	4F	R/W	Transmit Signaling 16.
50	R/W	Transmit Si Bits Align Frame	58	R	Receive Si Bits Align Frame.
51	R/W	Transmit Si Bits Non-Align Frame	59	R	Receive Si Bits Non-Align Frame.
52	R/W	Transmit Remote Alarm Bits	5A	R	Receive Remote Alarm Bits.
53	R/W	Transmit Sa4 Bits	5B	R	Receive Sa4 Bits.
54	R/W	Transmit Sa5 Bits	5C	R	Receive Sa5 Bits.
55	R/W	Transmit Sa6 Bits	5D	R	Receive Sa6 Bits.
56	R/W	Transmit Sa7 Bits	5E	R	Receive Sa7 Bits.
57	R/W	Transmit Sa8 Bits	5F	R	Receive Sa8 Bits.

NOTES:

1. The Test Registers 1, 2, and 3 are used only by the factory; these registers must be cleared (set to all zeros) on power-up initialization to insure proper operation.
2. Any unused register address will allow the status of the interrupts to appear on the bus.

2.0 PARALLEL PORT

The DS21Q43A is controlled via either a non-multiplexed (MUX=0) or multiplexed (MUX=1) bus by an external microcontroller or microprocessor. The DS21Q43A can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the AC Electrical Characteristics for more details.

3.0 CONTROL AND TEST REGISTERS

The operation of the DS21Q43A is configured via a set of seven registers. Typically, the control registers are

only accessed when the system is powered up. Once the DS21Q43A has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and three Common Control Registers (CCR1, CCR2 and CCR3). Each of the seven registers are described in this section.

The Test Registers at addresses 15, 18, and 19 hex are used by the factory in testing the DS21Q43A. On power-up, the Test Registers should be set to 00 hex in order for the DS21Q43A to operate properly.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB)								(LSB)
RSMF	RSM	RSIO	—	—	FRC	SYNCE	RESYNC	
SYMBOL	POSITION	NAME AND DESCRIPTION						
RSMF	RCR1.7	RSYNC Multiframing Function. Only used if the RSYNC pin is programmed in the multiframing mode (RCR1.6=1). 0=RSYNC outputs CAS multiframing boundaries 1=RSYNC outputs CRC4 multiframing boundaries						
RSM	RCR1.6	RSYNC Mode Select. 0=frame mode (see the timing in Section 11) 1=multiframing mode (see the timing in Section 11)						
RSIO	RCR1.5	RSYNC I/O Select. 0=RSYNC is an output (depends on RCR1.6) 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to zero when RCR2.1=0)						
—	RCR1.4	Not Assigned. Should be set to zero when written to.						
—	RCR1.3	Not Assigned. Should be set to zero when written to.						
FRC	RCR1.2	Frame Resync Criteria. 0=resync if FAS received in error 3 consecutive times 1=resync if FAS or bit 2 of non-FAS is received in error 3 consecutive times						
SYNCE	RCR1.1	Sync Enable. 0=auto resync enabled 1=auto resync disabled						
RESYNC	RCR1.0	Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.						

SYNC/RESYNC CRITERIA Table 3–1

FRAME OR MULTI-FRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N+2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non-FAS received	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found and previous timeslot 16 contains code other than all zeros	Two consecutive MF alignment words received in error	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	RBCS	RESE	–
SYMBOL	POSITION	NAME AND DESCRIPTION					
Sa8S	RCR2.7	Sa8 Bit Select. Set to one to report the Sa8 bit at the RLINK pin; set to zero to not report the Sa8 bit.					
Sa7S	RCR2.6	Sa7 Bit Select. Set to one to report the Sa7 bit at the RLINK pin; set to zero to not report the Sa7 bit.					
Sa6S	RCR2.5	Sa6 Bit Select. Set to one to report the Sa6 bit at the RLINK pin; set to zero to not report the Sa6 bit.					
Sa5S	RCR2.4	Sa5 Bit Select. Set to one to report the Sa5 bit at the RLINK pin; set to zero to not report the Sa5 bit.					
Sa4S	RCR2.3	Sa4 Bit Select. Set to one to report the Sa4 bit at the RLINK pin; set to zero to not report the Sa4 bit.					
RBCS	RCR2.2	Receive Side Backplane Clock Select. 0=if RSYSCLK is 1.544 MHz 1=if RSYSCLK is 2.048 MHz					
RESE	RCR2.1	Receive Side Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled					
–	RCR2.0	Not Assigned. Should be set to zero when written to.					

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)				(LSB)			
ODF	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO
SYMBOL	POSITION	NAME AND DESCRIPTION					
ODF	TCR1.7	Output Data Format. 0=bipolar data at TPOS and TNEG 1=NRZ data at TPOS; TNEG=0					
TFPT	TCR1.6	Transmit Timeslot 0 Pass Through. 0=FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1=FAS bits/Sa bits/Remote Alarm sourced from TSER					
T16S	TCR1.5	Transmit Timeslot 16 Data Select. 0=sample timeslot 16 at TSER pin 1=source timeslot 16 from TS0 to TS15 registers					
TUA1	TCR1.4	Transmit Unframed All Ones. 0=transmit data normally 1=transmit an unframed all one's code at TPOS and TNEG					
TSiS	TCR1.3	Transmit International Bit Select. 0=sample Si bits at TSER pin 1=source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)					
TSA1	TCR1.2	Transmit Signaling All Ones. 0=normal operation 1=force timeslot 16 in every frame to all ones					
TSM	TCR1.1	TSYNC Mode Select. 0=frame mode (see the timing in Section 11) 1=CAS and CRC4 multiframe mode (see the timing in Section 11)					
TSIO	TCR1.0	TSYNC I/O Select. 0=TSYNC is an input 1=TSYNC is an output					

NOTE:

1. See Figure 11–9 for more details about how the Transmit Control Registers affect the operation of the DS21Q43A.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)				(LSB)			
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	ODM	AEBE	PF

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	Sa8 Bit Select. Set to one to source the Sa8 bit from the TLINK pin; set to zero to not source the Sa8 bit.
Sa7S	TCR2.6	Sa7 Bit Select. Set to one to source the Sa7 bit from the TLINK pin; set to zero to not source the Sa7 bit.
Sa6S	TCR2.5	Sa6 Bit Select. Set to one to source the Sa6 bit from the TLINK pin; set to zero to not source the Sa6 bit.
Sa5S	TCR2.4	Sa5 Bit Select. Set to one to source the Sa5 bit from the TLINK pin; set to zero to not source the Sa5 bit.
Sa4S	TCR2.3	Sa4 Bit Select. Set to one to source the Sa4 bit from the TLINK pin; set to zero to not source the Sa4 bit.
ODM	TCR2.2	Output Data Mode. 0=pulses at TPOS and TNEG are one full TCLK period wide 1=pulses at TPOS and TNEG are 1/2 TCLK period wide
AEBE	TCR2.1	Automatic E-Bit Enable. 0=E-bits not automatically set in the transmit direction 1=E-bits automatically set in the transmit direction.
PF	TCR2.0	Function of RLOS/LOTC Pin. 0=Receive Loss of Sync (RLOS) 1=Loss of Transmit Clock (LOTC)

CCR1: COMMON CONTROL REGISTER 1 (Address=14 Hex)

(MSB)				(LSB)			
FLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOL	POSITION	NAME AND DESCRIPTION
FLB	CCR1.7	Framer Loopback. 0=loopback disabled 1=loopback enabled
THDB3	CCR1.6	Transmit HDB3 Enable. 0=HDB3 disabled 1=HDB3 enabled
TG802	CCR1.5	Transmit G.802 Enable. See Section 11 for details. 0=do not force TCHBLK high during bit 1 of timeslot 26 1=force TCHBLK high during bit 1 of timeslot 26
TCRC4	CCR1.4	Transmit CRC4 Enable. 0=CRC4 disabled 1=CRC4 enabled
RSM	CCR1.3	Receive Signaling Mode Select. 0=CAS signaling mode 1=CCS signaling mode

RHDB3	CCR1.2	Receive HDB3 Enable. 0=HDB3 disabled 1=HDB3 enabled
RG802	CCR1.1	Receive G.802 Enable. See Section 11 for details. 0=do not force RCHBLK high during bit 1 of timeslot 26 1=force RCHBLK high during bit 1 of timeslot 26
RCRC4	CCR1.0	Receive CRC4 Enable. 0=CRC4 disabled 1=CRC4 enabled

FRAMER LOOPBACK

When CCR1.7 is set to a one, the DS21Q43A will enter a Framers LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS21Q43A will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. data will be transmitted as normal at TPOS and TNEG
2. data at RPOS and RNEG will be ignored
3. the receive side signals become synchronous with TCLK instead of RCLK.

CCR2: COMMON CONTROL REGISTER 2 (Address=1A Hex)

(MSB)				(LSB)			
ECUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	—	—
SYMBOL	POSITION	NAME AND DESCRIPTION					
ECUS	CCR2.7	Error Counter Update Select. 0=update error counters once a second 1=update error counters every 62.5 ms (500 frames)					
VCRFS	CCR2.6	VCR Function Select. 0=count BiPolar Violations (BPVs) 1=count Code Violations (CVs)					
AAIS	CCR2.5	Automatic AIS Generation. 0=disabled 1=enabled					
ARA	CCR2.4	Automatic Remote Alarm Generation. 0=disabled 1=enabled					
RSERC	CCR2.3	RSER Control. 0=allow RSER to output data as received under all conditions 1=force RSER to one under loss of frame alignment conditions					
LOTCMC	CCR2.2	Loss of Transmit Clock Mux Control. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK should fail to transition (see Figure 1–1). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops					
—	CCR2.1	Not Assigned. Should be set to zero when written to.					
—	CCR2.0	Not Assigned. Should be set to zero when written to.					

AUTOMATIC ALARM GENERATION

When either CCR2.4 or CCR2.5 is set to one, the DS21Q43A monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal). If any one

(or more) of the above conditions is present, then the DS21Q43A will either force an AIS alarm (if CCR2.5=1) or a Remote Alarm (CCR2.4=1) to be transmitted via the TPOS and TNEG pins. It is an illegal state to have both CCR2.4 and CCR2.5 set to one at the same time.

CCR3: COMMON CONTROL REGISTER 3 (ADDRESS=1B HEX)

(MSB)		(LSB)				
TESE	TCBFS	TIRFS	ESR	LIRST	—	TBCS
SYMBOL	POSITION	NAME AND DESCRIPTION				
TESE	CCR3.7	Transmit Side Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled				
TCBFS	CCR3.6	Transmit Channel Blocking Registers (TCBR) Function Select. 0=TCBRs define the operation of the TCHBLK output pin 1=TCBRs define which signaling bits are to be inserted				
TIRFS	CCR3.5	Transmit Idle Registers (TIR) Function Select. 0=TIRs define in which channels to insert idle code 1=TIRs define in which channels to insert data from RSER				
ESR	CCR3.4	Elastic Stores Reset. Setting this bit from a one to a zero will force the elastic stores to a known depth. Should be toggled after RSYCLK and TSYCLK have been applied and are stable. Must be set and cleared again for a subsequent reset. Do not leave this bit set high.				
—	CCR3.3	Not Assigned. Should be set to zero when written to.				
—	CCR3.2	Not Assigned. Should be set to zero when written to.				
TBCS	CCR3.1	Transmit Side Backplane Clock Select. 0=if TSYCLK is 1.544 MHz 1=if TSYCLK is 2.048 MHz				
—	CCR3.0	Not Assigned. Should be set to zero when written to.				

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS21Q43A should be configured for operation by writing to all of the internal registers (this includes the Test Registers) since the contents of the internal registers cannot be predicted on power-up. Finally, after the RSYCLK and TSYCLK inputs are stable, the ESR bit should be toggled from a zero to a one and then back to zero (this step can be skipped if the elastic store is not being used).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS21Q43A, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in these registers operate in a latched fashion (except for the SSR).

This means that if an event occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm is still present.

The user will always precede a read of the SR1, SR2, and RIR registers with a write. The byte written to the register will inform the DS21Q43A which bits the user wishes to read and have cleared. The user will write a byte to one of these three registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is nec-

essary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21Q43A with higher-order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this registers with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT}}$ pin. All four of the framers share the $\overline{\text{INT}}$ output. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively. The user can determine which framer has active interrupts by polling the Interrupt Status Register (ISR).

ISR: INTERRUPT STATUS REGISTER (any unused address)

(MSB)								(LSB)
F3SR2	F3SR1	F2SR2	F2SR1	F1SR2	F1SR1	F0SR2	F0SR1	
SYMBOL	POSITION	NAME AND DESCRIPTION						
F3SR2	ISR.7	Status of Interrupt for SR2 in Framer 3. 1=interrupt active.						
F3SR1	ISR.6	Status of Interrupt for SR1 in Framer 3. 1=interrupt active.						
F2SR2	ISR.5	Status of Interrupt for SR2 in Framer 2. 1=interrupt active.						
F2SR1	ISR.4	Status of Interrupt for SR1 in Framer 2. 1=interrupt active.						
F1SR2	ISR.3	Status of Interrupt for SR2 in Framer 1. 1=interrupt active.						
F1SR1	ISR.2	Status of Interrupt for SR1 in Framer 1. 1=interrupt active.						
F0SR2	ISR.1	Status of Interrupt for SR2 in Framer 0. 1=interrupt active.						
F0SR1	ISR.0	Status of Interrupt for SR1 in Framer 0. 1=interrupt active.						

RIR: RECEIVE INFORMATION REGISTER (ADDRESS=08 HEX)

(MSB)				(LSB)			
TESF	TESE	LORC	RESF	RESE	CRCRC	FASRC	CASRC
SYMBOL		POSITION		NAME AND DESCRIPTION			
TESF		RIR.7		Transmit Side Elastic Store Full. Set when the elastic store buffer fills and a frame is deleted.			
TESE		RIR.6		Transmit Side Elastic Store Empty. Set when the elastic store buffer empties and a frame is repeated.			
LORC		RIR.5		Loss of Receive Clock. Set when the RCLK pin has not transitioned for at least 2 μ s (3 μ s \pm 1 μ s).			
RESF		RIR.4		Receive Side Elastic Store Full. Set when the elastic store buffer fills and a frame is deleted.			
RESE		RIR.3		Receive Side Elastic Store Empty. Set when the elastic store buffer empties and a frame is repeated.			
CRCRC		RIR.2		CRC Resync Criteria Met. Set when 915/1000 code words are received in error.			
FASRC		RIR.1		FAS Resync Criteria Met. Set when 3 consecutive FAS words are received in error.			
CASRC		RIR.0		CAS Resync Criteria Met. Set when 2 consecutive CAS MF alignment words are received in error.			

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)				(LSB)			
CSC5	CSC4	CSC3	CSC2	CSC1	FASSA	CASSA	CRC4SA
SYMBOL		POSITION		NAME AND DESCRIPTION			
CSC5		SSR.7		CRC4 Sync Counter Bit 5. MSB of the 6-bit counter.			
CSC4		SSR.6		CRC4 Sync Counter Bit 4.			
CSC3		SSR.5		CRC4 Sync Counter Bit 3.			
CSC2		SSR.4		CRC4 Sync Counter Bit 2.			
CSC1		SSR.3		CRC4 Sync Counter Bit 1. Next to LSB of the 6-bit counter. The LSB is not accessible.			
FASSA		SSR.2		FAS Sync Active. Set while the synchronizer is searching for alignment at the FAS level.			
CASSA		SSR.1		CAS MF Sync Active. Set while the synchronizer is searching for the CAS MF alignment word.			
CRC4SA		SSR.0		CRC4 MF Sync Active. Set while the synchronizer is searching for the CRC4 MF alignment word.			

CRC4 SYNC COUNTER

The CRC4 Sync Counter increments each time the 8 ms CRC4 multiframe search times out. The counter is cleared when the DS21Q43A has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0=0). This counter is useful for determining the

amount of time the DS21Q43A has been searching for synchronization at the CRC4 level. Annex B of ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

SR1: STATUS REGISTER 1 (ADDRESS=06 HEX)

(MSB)				(LSB)			
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION					
RSA1	SR1.7	Receive Signaling All Ones. Set when the contents of timeslot 16 contains less than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.					
RDMA	SR1.6	Receive Distant MF Alarm. Set when bit 6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.					
RSA0	SR1.5	Receive Signaling All Zeros. Set when over a full MF, timeslot 16 contains all zeros.					
RSLIP	SR1.4	Receive Side Elastic Store Slip. Set when the elastic store has either repeated or deleted a frame of data.					
RUA1	SR1.3	Receive Unframed All Ones. Set when an unframed all ones code is received at RPOS and RNEG.					
RRA	SR1.2	Receive Remote Alarm. Set when a remote alarm is received at RPOS and RNEG.					
RCL	SR1.1	Receive Carrier Loss. Set when 255 consecutive zeros have been detected at RPOS and RNEG.					
RLOS	SR1.0	Receive Loss of Sync. Set when the device is not synchronized to the receive E1 stream.					

ALARM CRITERIA Table 4–1

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all ones)	over 16 consecutive frames (one full MF) timeslot 16 contains less than three zeros	over 16 consecutive frames (one full MF) timeslot 16 contains three or more zeros	G.732 4.2
RSA0 (receive signaling all zeros)	over 16 consecutive frames (one full MF) timeslot 16 contains all zeros	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to one for two consecutive MF	bit 6 in timeslot 16 of frame 0 set to zero for a two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all ones)	less than three zeros in two frames (512 bits)	more than two zeros in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non-align frame set to one for three consecutive occasions	bit 3 of non-align frame set to zero for three consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 consecutive zeros received	in 255 bit times, at least 32 ones are received	G.775

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB)				(LSB)			
RMF	RAF	TMF	SEC	TAF	LOT	RCMF	TSLIP
SYMBOL	POSITION	NAME AND DESCRIPTION					
RMF	SR2.7	Receive CAS Multiframe. Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.					
RAF	SR2.6	Receive Align Frame. Set every 250 μ s at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.					
TMF	SR2.5	Transmit Multiframe. Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.					
SEC	SR2.4	One Second Timer. Set on increments of one second based on RCLK. If CCR2.7=1, then this bit will be set every 62.5 ms instead of once a second.					
TAF	SR2.3	Transmit Align Frame. Set every 250 μ s at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.					
LOT	SR2.2	Loss of Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 3.9 μ s). Will force the LOTC pin high if enabled via TCR2.0. Based on RCLK.					
RCMF	SR2.1	Receive CRC4 Multiframe. Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.					
TSLIP	SR2.0	Transmit Elastic Store Slip. Set when the elastic store has either repeated or deleted a frame of data.					

IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)

(MSB)				(LSB)			
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	IMR1.7	Receive Signaling All Ones. 0=interrupt masked 1=interrupt enabled
RDMA	IMR1.6	Receive Distant MF Alarm. 0=interrupt masked 1=interrupt enabled
RSA0	IMR1.5	Receive Signaling All Zeros. 0=interrupt masked 1=interrupt enabled
RSLIP	IMR1.4	Receive Elastic Store Slip Occurrence. 0=interrupt masked 1=interrupt enabled
RUA1	IMR1.3	Receive Unframed All Ones. 0=interrupt masked 1=interrupt enabled
RRA	IMR1.2	Receive Remote Alarm. 0=interrupt masked 1=interrupt enabled
RCL	IMR1.1	Receive Carrier Loss. 0=interrupt masked 1=interrupt enabled
RLOS	IMR1.0	Receive Loss of Sync. 0=interrupt masked 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)				(LSB)			
RMF	RAF	TMF	SEC	TAF	LOT	RCMF	TSZIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	Receive CAS Multiframe. 0=interrupt masked 1=interrupt enabled
RAF	IMR2.6	Receive Align Frame. 0=interrupt masked 1=interrupt enabled
TMF	IMR2.5	Transmit Multiframe. 0=interrupt masked 1=interrupt enabled

SEC	IMR2.4	One Second Timer. 0=interrupt masked 1=interrupt enabled
TAF	IMR2.3	Transmit Align Frame. 0=interrupt masked 1=interrupt enabled
LOTC	IMR2.2	Loss Of Transmit Clock. 0=interrupt masked 1=interrupt enabled
RCMF	IMR2.1	Receive CRC4 Multiframe. 0=interrupt masked 1=interrupt enabled
TSLIP	IMR2.0	Transmit Side Elastic Store Slip. 0=interrupt masked 1=interrupt enabled

5.0 ERROR COUNT REGISTERS

There are a set of four counters in the DS21Q43A that record bipolar or code violations, errors in the CRC4 SMF code words, E-bits as reported by the far end, and word errors in the FAS. Each of these four counters are automatically updated on either one second boundaries (CCR2.7=0) or every 62.5 ms (CCR2.7=1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 100 ms. The user can use the interrupt from the timer to determine when to read these registers. The user has a full second (or 62.5 ms) to read the counters before the data is lost.

5.1 BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a

16-bit counter that records either BiPolar Violations (BPVs) or Code Violations (CVs). If CCR2.6=0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side via CCR1.2, then HDB3 code words are not counted as BPVs. If CCR2.6=1, then the VCR counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the DS21Q43A should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on a E1 line would have to be greater than 10⁻² before the VCR would saturate.

VCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)

VCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address=01 Hex)

(MSB)				(LSB)				
V15	V14	V13	V12	V11	V10	V9	V8	VCR1
V7	V6	V5	V4	V3	V2	V1	V0	VCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
V15	VCR1.7	MSB of the 16-bit bipolar or code violation count .
V0	VCR2.0	LSB of the 16-bit bipolar or code violation count.

10-bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum

count if loss of multiframe sync occurs at the CAS level.

CRCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)

CRCR2: CRC4 COUNT REGISTER 2 (Address=03 Hex)

(MSB)	(LSB)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(LSB)	(MSB)
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	CRC9	CRC8
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCR1	CRCR2

SYMBOL	POSITION	NAME AND DESCRIPTION	POSITION	SYMBOL
CRC9	CRCR1.1	MSB of the 10-bit CRC4 error count.	CRCR1.7	FASR1.7
CRC0	CRCR2.0	LSB of the 10-bit CRC4 error count.	CRCR2.2	FASR2.2

NOTE:

1. The upper six bits of CRCR1 at address 02 are the most significant bits of the 12-bit FAS error counter.

5.3 E-Bit Counter

E-bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 10-bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will

increment once each time the received E-bit is set to zero. Since the maximum E-bit count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

EBCR1: E-BIT COUNT REGISTER 1 (Address=04 Hex)

EBCR2: E-BIT COUNT REGISTER 2 (Address=05 Hex)

(MSB)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(LSB)
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	EB9
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EB8
EBCR1	EBCR2							

SYMBOL	POSITION	NAME AND DESCRIPTION
EB9	EBCR1.1	MSB of the 10-bit E-Bit count.
EB0	EBCR2.0	LSB of the 10-bit E-Bit count.

NOTE:

1. The upper six bits of EBCR1 at address 04 are the least significant bits of the 12-bit FAS error counter.

5.4 FAS Error Counter

FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 12-bit counter that records word errors in the Frame Alignment Signal in timeslot 0. This counter is disabled

during loss of frame synchronization conditions, it is not disabled during loss of synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one second period is 4000, this counter cannot saturate.

FASCR1: FAS BIT COUNT REGISTER 1 (Address=02 Hex)

FASCR2: FAS BIT COUNT REGISTER 2 (Address=04 Hex)

(MSB)			(LSB)			(MSB)		
FAS11	FAS10	FAS9	FAS8	FAS7	FAS6	(note 2)	(note 2)	FASCR1
FAS5	FAS4	FAS3	FAS2	FAS1	FAS0	(note 1)	(note 1)	FASCR2

SYMBOL	POSITION	NAME AND DESCRIPTION	POSITION	SYMBOL
FAS11	FASCR1.7	MSB of the 12-bit FAS error count.	FASCR1.1	CRC3
FAS0	FASCR2.2	LSB of the 12-bit FAS error count.	FASCR2.0	CRC0

NOTES:

1. The lower two bits of FASCR1 at address 02 are the most significant bits of the 10-bit CRC4 error counter.
2. The lower two bits of FASCR2 at address 04 are the most significant bits of the 10-bit E-Bit counter.

6.0 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS21Q43A provides for access to both the Sa and the Si bits via three different methods. The first is via a hardware scheme using the RLINK/RLCLK and TLINK/TLCLK pins. The first method is discussed in Section 6.1. The second involves using the internal RAF/RNAF and TAF/TNAF registers and is discussed in Section 6.2. The third method which is covered in Section 6.3 involves an expanded version of the second method and is one of the features added to the DS21Q43A from the original DS2143 definition.

6.1 Hardware Scheme

On the receive side, all of the received data is reported at the RLINK pin. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits. If RSYNC is programmed to output a frame boundary, it will identify the Si bits. See Section 11 for detailed timing.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (see Section 6.2 for details) or from the external TLINK pin. Via TCR2, the DS21Q43A can be programmed to source any combination of the additional bits from the TLINK

pin. If the user wishes to pass the Sa bits through the DS21Q43A without them being altered, then the device should be set up to source all five Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Si bits can be inserted through the TSER pin via the clearing of the TCR1.3 bit. Please see the timing diagrams and the transmit data flow diagram in Section 11 for examples.

6.2 Internal Register Scheme Based on Doubleframe

On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 μ s to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 μ s to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the DS21Q43A is pro-

grammed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to one (please see Section 6.1 for details). Please see the register descriptions for TCR1 and TCR2 and the Transmit Data Flow diagram in Section 11 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB)				(LSB)			
Si	0	0	1	1	0	1	1
SYMBOL	POSITION	NAME AND DESCRIPTION					
Si	RAF.7	International Bit.					
0	RAF.6	Frame Alignment Signal Bit.					
0	RAF.5	Frame Alignment Signal Bit.					
1	RAF.4	Frame Alignment Signal Bit.					
1	RAF.3	Frame Alignment Signal Bit.					
0	RAF.2	Frame Alignment Signal Bit.					
1	RAF.1	Frame Alignment Signal Bit.					
1	RAF.0	Frame Alignment Signal Bit.					

RNAF: RECEIVE NON-ALIGN FRAME REGISTER (Address=1F Hex)

(MSB)				(LSB)			
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
SYMBOL	POSITION	NAME AND DESCRIPTION					
Si	RNAF.7	International Bit.					
1	RNAF.6	Frame Non-Alignment Signal Bit.					
A	RNAF.5	Remote Alarm.					
Sa4	RNAF.4	Additional Bit 4.					
Sa5	RNAF.3	Additional Bit 5.					
Sa6	RNAF.2	Additional Bit 6.					
Sa7	RNAF.1	Additional Bit 7.					
Sa8	RNAF.0	Additional Bit 8.					

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB)				(LSB)			
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TAF.7	International Bit.
0	TAF.6	Frame Alignment Signal Bit.
0	TAF.5	Frame Alignment Signal Bit.
1	TAF.4	Frame Alignment Signal Bit.
1	TAF.3	Frame Alignment Signal Bit.
0	TAF.2	Frame Alignment Signal Bit.
1	TAF.1	Frame Alignment Signal Bit.
1	TAF.0	Frame Alignment Signal Bit.

TNAF: TRANSMIT NON-ALIGN FRAME REGISTER (Address=21 Hex)

(MSB)				(LSB)			
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TNAF.7	International Bit.
1	TNAF.6	Frame Non-Alignment Signal Bit.
A	TNAF.5	Remote Alarm (used to transmit the alarm).
Sa4	TNAF.4	Additional Bit 4.
Sa5	TNAF.3	Additional Bit 5.
Sa6	TNAF.2	Additional Bit 6.
Sa7	TNAF.1	Additional Bit 7.
Sa8	TNAF.0	Additional Bit 8.

6.3 Internal Register Scheme Based on CRC4 Multiframe

On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the Receive CRC4 Multiframe bit in Status Register 2 (SR2.1). The host can use the SR2.1 bit to know when to read these registers. The user has 2 ms to retrieve the data before it is lost. The MSB of each register is the first received. Please see the register descriptions below and the Transmit Data Flow diagram in Section 11 for more details.

On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that via the Transmit Sa Bit Control Register (TSaCR), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the Transmit Multiframe bit in Status Register 2 (SR2.5). The host can use the SR2.5 bit to know when to update these registers. It has 2 ms to update the data or else the old data will be retransmitted. The MSB of each register is the first bit transmitted. Please see the register descriptions below and the Transmit Data Flow diagram in Section 11 for more details.

REGISTER NAME	ADDRESS (HEX)	FUNCTION
RSiAF	58	The eight Si bits in the align frame.
RSiNAF	59	The eight Si bits in the non-align frame.
RRA	5A	The eight reportings of the receive remote alarm (RA).
RSa4	5B	The eight Sa4 reported in each CRC4 multiframe.
RSa5	5C	The eight Sa5 reported in each CRC4 multiframe.
RSa6	5D	The eight Sa6 reported in each CRC4 multiframe.
RSa7	5E	The eight Sa7 reported in each CRC4 multiframe.
RSa8	5F	The eight Sa8 reported in each CRC4 multiframe.
TSiAF	50	The eight Si bits to be inserted into the align frame
TSiNAF	51	The eight Si bits to be inserted into the non-align frame.
TRA	52	The eight settings of receive remote alarm (RA).
TSa4	53	The eight Sa4 settings in each CRC4 multiframe.
TSa5	54	The eight Sa5 settings in each CRC4 multiframe.
TSa6	55	The eight Sa6 settings in each CRC4 multiframe.
TSa7	56	The eight Sa7 settings in each CRC4 multiframe.
TSa8	57	The eight Sa8 settings in each CRC4 multiframe.

TSACR: TRANSMIT SA BIT CONTROL REGISTER (Address=1C Hex)

(MSB)				(LSB)			
SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8
SYMBOL	POSITION	NAME AND DESCRIPTION					
SiAF	TSaCR.7	International Bit in Align Frame Insertion Control Bit 0=do not insert data from the TSiAF register into the transmit data stream 1=insert data from the TSiAF register into the transmit data stream					
SiNAF	TSaCR.6	International Bit in Non-Align Frame Insertion Control Bit 0=do not insert data from the TSiNAF register into the transmit data stream 1=insert data from the TSiNAF register into the transmit data stream					
RA	TSaCR.5	Remote Alarm Insertion Control Bit 0=do not insert data from the TRA register into the transmit data stream 1=insert data from the TRA register into the transmit data stream					
Sa4	TSaCR.4	Additional Bit 4 Insertion Control Bit 0=do not insert data from the TSa4 register into the transmit data stream 1=insert data from the TSa4 register into the transmit data stream					
Sa5	TSaCR.3	Additional Bit 5 Insertion Control Bit 0=do not insert data from the TSa5 register into the transmit data stream 1=insert data from the TSa5 register into the transmit data stream					

Sa6	TSaCR.2	Additional Bit 6 Insertion Control Bit 0=do not insert data from the TSa6 register into the transmit data stream 1=insert data from the TSa6 register into the transmit data stream
Sa7	TSaCR.1	Additional Bit 7 Insertion Control Bit 0=do not insert data from the TSa7 register into the transmit data stream 1=insert data from the TSa7 register into the transmit data stream
Sa8	TSaCR.0	Additional Bit 8 Insertion Control Bit 0=do not insert data from the TSa8 register into the transmit data stream 1=insert data from the TSa8 register into the transmit data stream

7.0 SIGNALING OPERATION

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS21Q43A. Each of the 30 channels has four signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the channel associated with a

particular signaling bit. The channel numbers have been assigned as described in the ITU/CCITT documents. For example, channel 1 is associated with timeslot 1 and channel 30 is associated with timeslot 31. There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB)				(LSB)				
0	0	0	0	X	Y	X	X	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(31)	B(31)	C(31)	D(31)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(32)	B(32)	C(32)	D(32)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(33)	B(33)	C(33)	D(33)	RS4 (33)
A(4)	B(4)	C(4)	D(4)	A(34)	B(34)	C(34)	D(34)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(35)	B(35)	C(35)	D(35)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(36)	B(36)	C(36)	D(36)	RS7 (36)
A(7)	B(7)	C(7)	D(7)	A(37)	B(37)	C(37)	D(37)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(38)	B(38)	C(38)	D(38)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(39)	B(39)	C(39)	D(39)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(40)	B(40)	C(40)	D(40)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(41)	B(41)	C(41)	D(41)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(42)	B(42)	C(42)	D(42)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(43)	B(43)	C(43)	D(43)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(44)	B(44)	C(44)	D(44)	RS15(3E)
A(15)	B(15)	C(15)	D(15)	A(45)	B(45)	C(45)	D(45)	RS16(3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	Spare Bits.
Y	RS1.2	Remote Alarm Bit (integrated and reported in SR1.6).
A(1)	RS2.7	Signaling Bit A for Channel 1
D(30)	RS16.0	Signaling Bit D for Channel 30.

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling bits from two timeslots. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all

conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)				(LSB)				
0	0	0	0	X	Y	X	X	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	Spare Bits.
Y	TS1.2	Remote Alarm Bit.
A(1)	TS2.7	Signaling Bit A for Channel 1.
D(30)	TS16.0	Signaling Bit D for Channel 30.

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the DS21Q43A will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the

device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSR's before the old data will be retransmitted.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper nibble must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.5 bit should be set to a one. If no alarm is to be transmitted, then the TS1.5 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to one. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be informed when the signaling registers need to be loaded with data. The user has 2 ms to load the data before the old data will be retransmitted. Via the CCR3.6 bit, the user has the option to use the Transmit Channel

Blocking Registers (TCBRs) to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBRs=0). See the Transmit Data Flow diagram in Section 11 for more details.

8.0 TRANSMIT IDLE REGISTERS

There is a set of five registers in the DS21Q43A that can be used to custom tailor the data that is to be transmitted onto the E1 line, on a channel by channel basis. Each of the 32 E1 channels can be forced to have a user defined idle code inserted into them.

TIR1/TIR2/TIR3/TIR4: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TIR4.7	Transmit Idle Registers. 0=do not insert the Idle Code into this channel 1=insert the Idle Code into this channel
CH1	TIR1.0	

NOTE:

If CCR3.5=1, then a zero in the TIRs implies that channel data is to be sourced from TSER and a one implies that channel data is to be sourced from the RSER pin.

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)				(LSB)			
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0
SYMBOL	POSITION	NAME AND DESCRIPTION					
TIDR7	TIDR.7	MSB of the Idle Code .					
TIDR0	TIDR.0	LSB of the Idle Code.					

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represent a timeslot in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). In the TIDR, the MSB is transmitted first. Via the CCR3.5 bit,

the user has the option to use the TIRs to determine on a channel by channel basis, if data from the RSER pin should be substituted for data from the TSER pin. In this mode, if the corresponding bit in the TIRs is set to one, then data will be sourced from the RSER pin. If the corresponding bit in the TIRs is set to zero, then data for

that channel will sourced from the TSER pin. See the Transmit Data Flow diagram in Section 11 for more details.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Register (RCBR1/RCBR2/RCBR3/RCBR4) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user programmable outputs that can be forced either high or low during individual channels. These outputs can be used to

block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 11 for an example. The TCBRs have alternate mode of use. Via the CCR3.6 bit, the user has the option to use the TCBRs to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBR=0). See the Transmit Data Flow diagram in Section 11 for more details.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS

(Address=2B to 2E Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	RCBR4.7	Receive Channel Blocking Registers. 0=force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1=force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS

(Address=22 to 25 Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TCBR4.7	Transmit Channel Blocking Registers. 0=force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1=force the TCHBLK pin high during this channel time

NOTE:

If CCR3.6=1, then a zero in the TCBRs implies that signaling data is to be sourced from TSER and a one implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See definition below.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6=1

(MSB)				(LSB)				
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4

*=CH1 and CH17 should be set to one to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

10.0 ELASTIC STORES OPERATION

Each framer within the DS21Q43A contains dual two-frame (512 bits) elastic stores, one for the receive direction, and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the E1 data stream to 1.544Mbps (or a multiple of 1.544Mbps) which is the T1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the E1 data stream and an asynchronous (i.e. not frequency locked) backplane clock (which can be 1.544 MHz or 2.048 MHz or a multiple thereof up to 8.192 MHz). Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.4). Toggling the CCR3.4 bit forces the read and write pointers into opposite frames. Both elastic stores within the DS21Q43A are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544 MHz or 2.048 MHz backplane without regard to the backplane rate the other elastic store is interfacing to.

10.1 Receive Side

If the receive side elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2=0) or 2.048 MHz (RCR2.2=1) clock at the RSYCLK pin. The user has the option of either providing a frame sync at the RSYNC pin (RCR1.5=1) or having the RSYNC pin provide a pulse on frame boundaries (RCR1.5=0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to zero and if the user wishes to have pulses occur at the multi-frame boundary, then RCR1.6 must be set to one. The

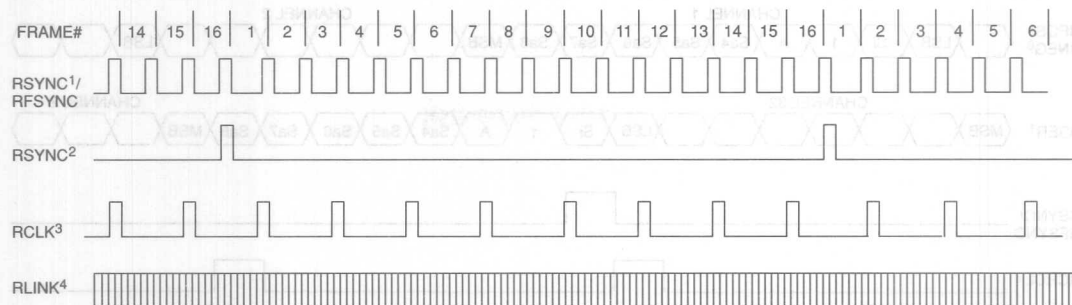
DS21Q43A will always indicate frame boundaries via the RFSYNC output whether the elastic store is enabled or not. If the elastic store is enabled, then either CAS (RCR1.7=0) or CRC4 (RCR1.7=1) multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 1.544 MHz clock to the RSYCLK pin, then every fourth channel of the received E1 data will be deleted and a F-bit position (which will be forced to one) will be inserted. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted from the received E1 data stream. Also, in 1.544 MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). See Section 11 for more details. If the 512-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

10.2 Transmit Side

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR3.7. A 1.544 MHz (CCR3.1=0) or 2.048 MHz (CCR3.1=1) clock can be applied to the TSYCLK input. If the user selects to apply a 1.544 MHz clock to the TSYCLK pin, then the data sampled at TSER will be ignored every fourth channel. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be ignored. The user must supply a 8 KHz frame sync pulse to the TFSYNC input. See Section 11 for more details. Controlled slips in the transmit elastic store are reported in the SR2.0 bit and the direction of the slip is reported in the RIR.6 and RIR.7 bits.

11.0 TIMING DIAGRAMS/SYNCHRONIZATION FLOWCHART/TRANSMIT DATA FLOW DIAGRAM

RECEIVE SIDE TIMING Figure 11–1

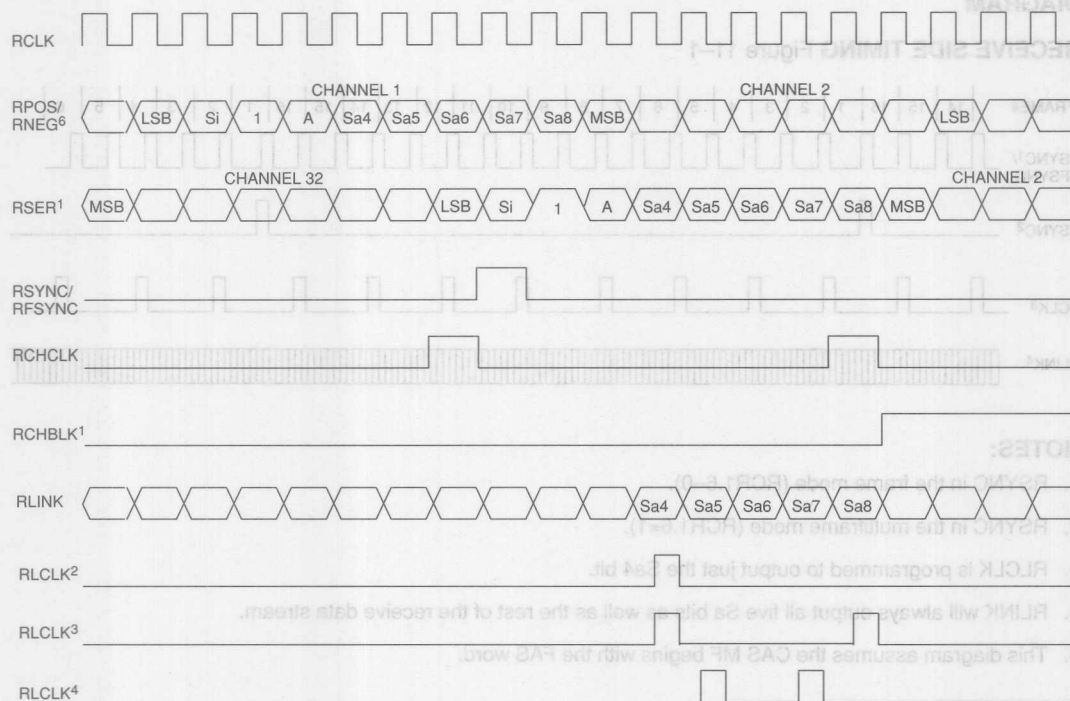


NOTES:

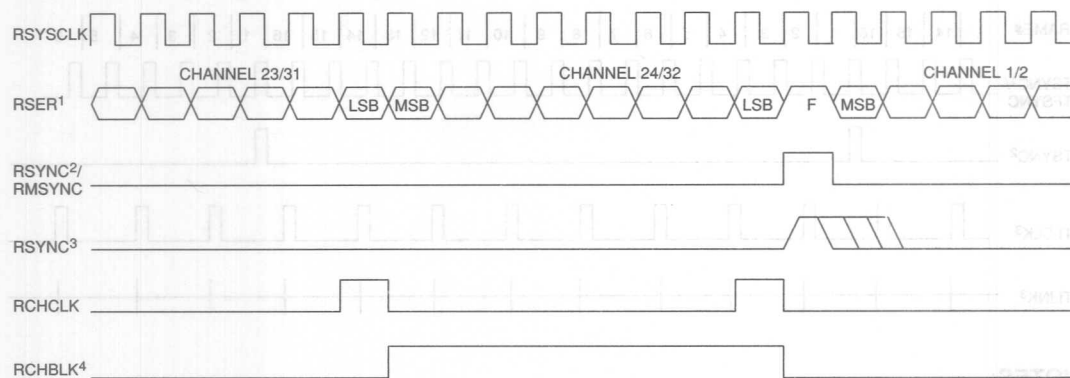
1. RSYNC in the frame mode (RCR1.6=0).
2. RSYNC in the multiframe mode (RCR1.6=1).
3. RLCLK is programmed to output just the Sa4 bit.
4. RLINK will always output all five Sa bits as well as the rest of the receive data stream.
5. This diagram assumes the CAS MF begins with the FAS word.

NOTES:

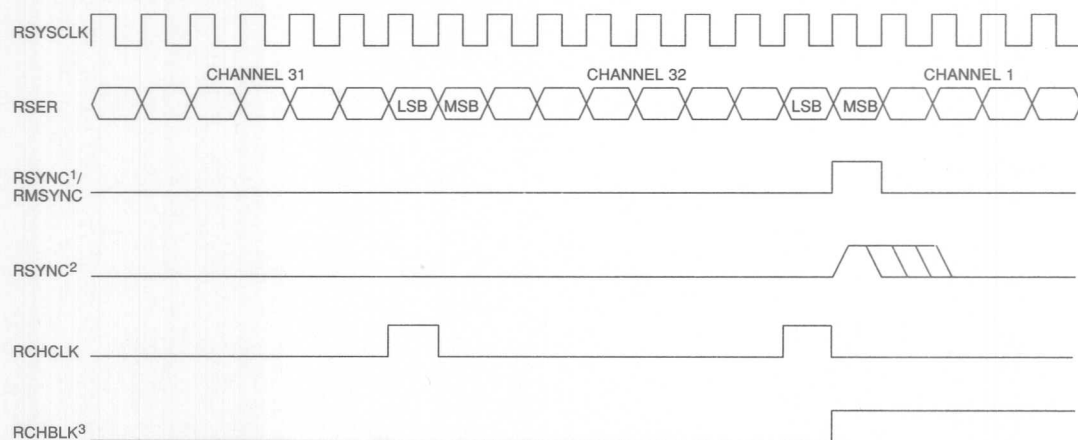
1. RCLK3 is programmed to output the Sa4 bit.
2. RLINK is programmed to output the Sa4 bit.
3. RLINK is programmed to output the Sa4 and Sa5 bits.
4. RLINK is programmed to output the Sa4 and Sa5 bits.
5. Shown is a non-align frame boundary.
6. There is a RCLK delay from RFSYNC to RFSYNC.

RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED) Figure 11-2**NOTES:**

1. RCHBLK is programmed to block channel 2.
2. RLINK is programmed to output the Sa4 bits.
3. RLINK is programmed to output the SA4 and SA8 bits.
4. RLINK is programmed to output the Sa5 and Sa7 bits.
5. Shown is a non-align frame boundary.
6. There is a 6 RCLK delay from RPOS/RNEG to RSER.

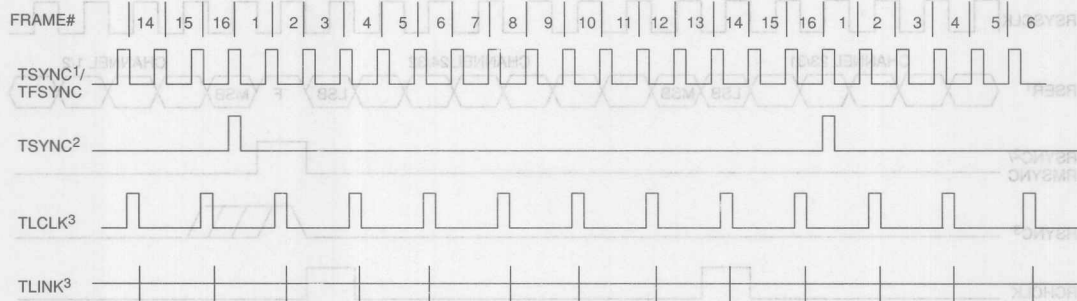
RECEIVE SIDE 1.544 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 11–3**NOTES:**

1. Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to one).
2. RSYNC is in the output mode (RCR1.5=0).
3. RSYNC is in the input mode (RCR1.5=1).
4. RCHBLK is programmed to block channel 24.

RECEIVE SIDE 2.048 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 11–4**NOTES:**

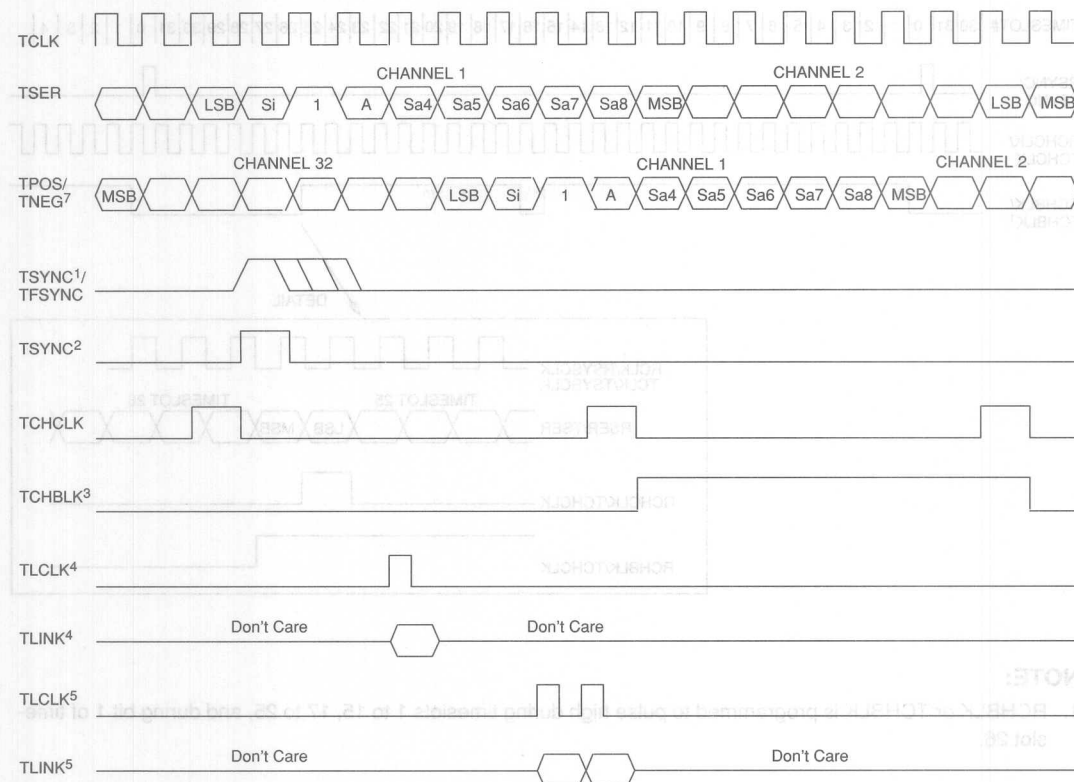
1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RCHBLK is programmed to block channel 1.

TRANSMIT SIDE TIMING Figure 11-5



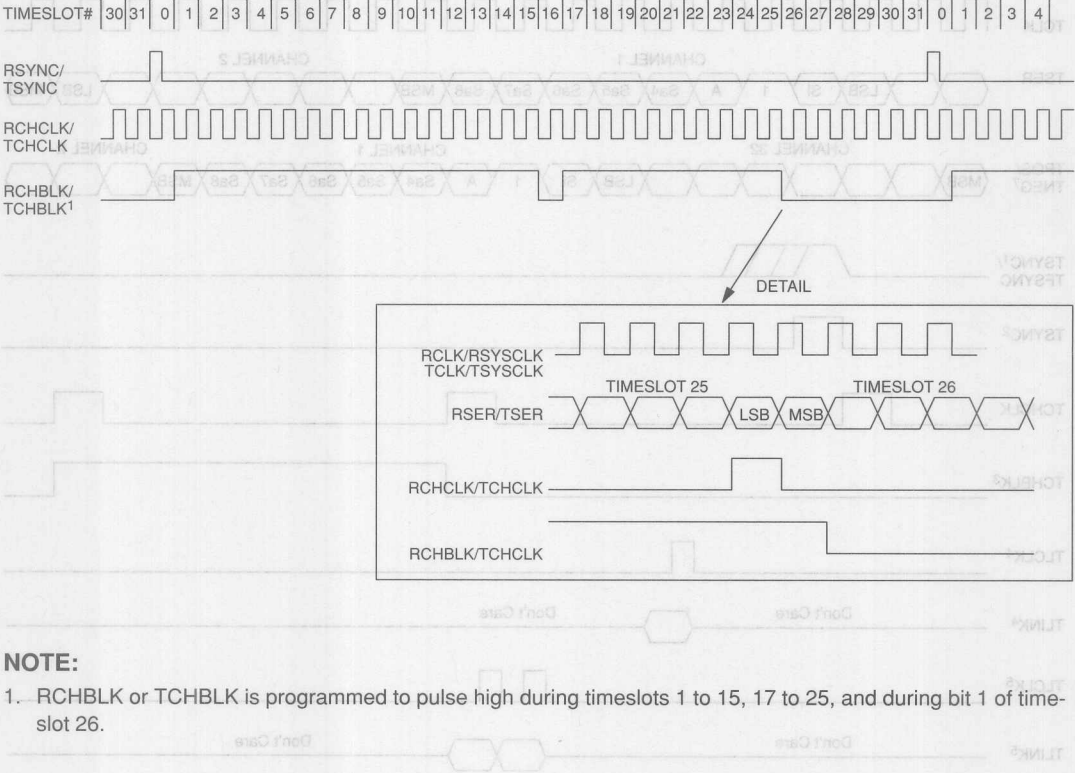
NOTES:

1. TSYNC in the frame mode (TCR1.1=0).
2. TSYNC in the multiframe mode (TCR1.1=1).
3. TLINK is programmed to source only the Sa4 bit
4. This diagram assumes both the CAS MF and the CRC4 begin with the align frame.

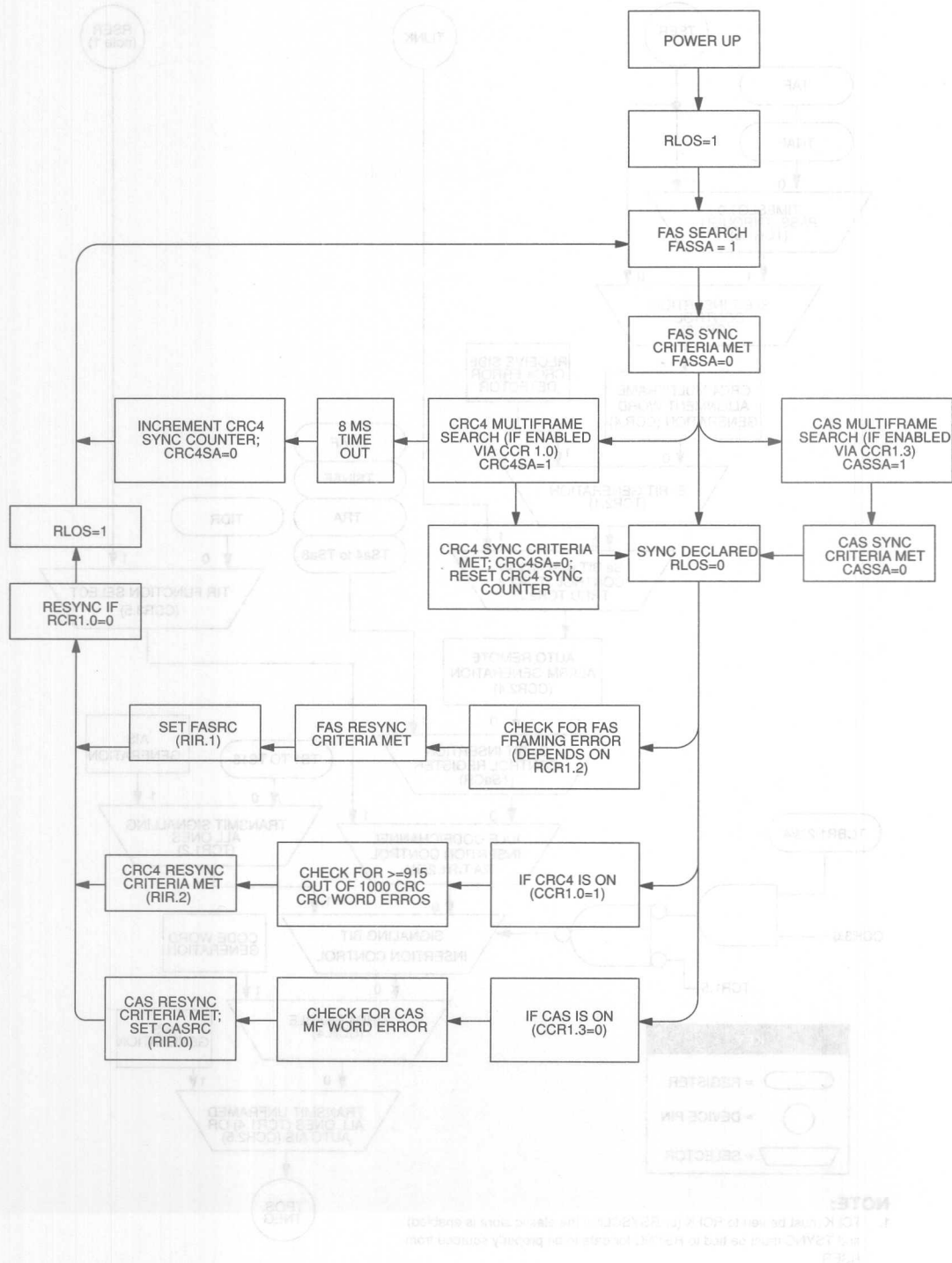
TRANSMIT SIDE BOUNDARY TIMING Figure 11–6**NOTES:**

1. TSYNC is in the input mode (TCR1.0=0).
2. TSYNC is in the output mode (TCR1.0=1).
3. TCHBLK is programmed to block channel 2.
4. TLINK is programmed to source the Sa4 bits.
5. TLINK is programmed to source the Sa7 and Sa8 bits.
6. Shown is a non-align frame boundary.
7. There is a 5 TCLK delay from TSER to TPOS/TNEG.

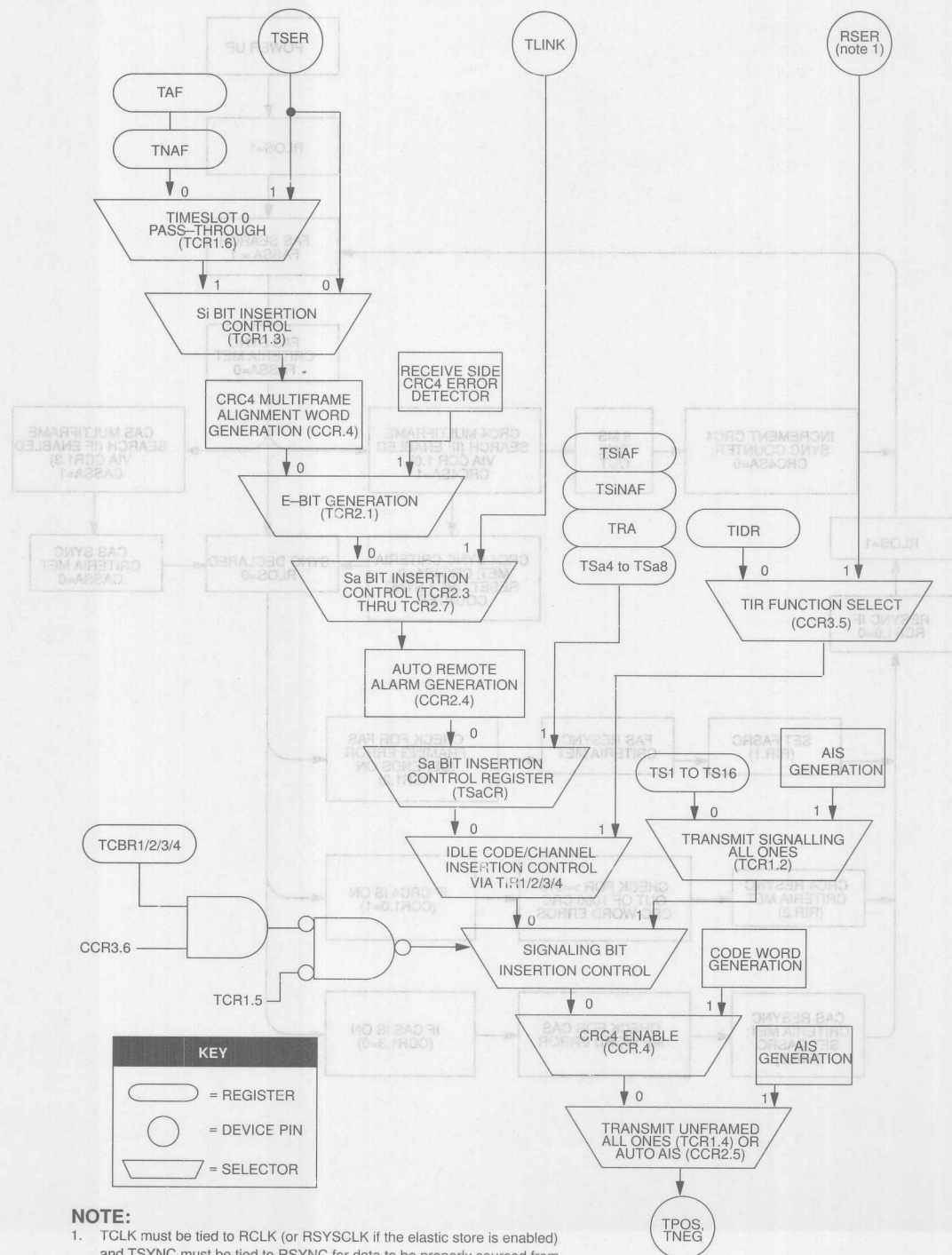
G.802 TIMING Figure 11-7



DS21Q43A SYNCHRONIZATION FLOWCHART Figure 11–8



DS21Q43A TRANSMIT DATA FLOW Figure 11-9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

-1.0V to +7.0V

Operating Temperature

0°C to 70°C

Storage Temperature

-55°C to +125°C

Soldering Temperature

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.50		5.50	V	1

CAPACITANCE(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		32		mA	1
Input Leakage	I_{IL}	-1.0		+1.0	μA	2
Output Leakage	I_{LO}			1.0	μA	3
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. TCLK=RCLK=TSYSCLK=RSYSCLK=2.048 MHz; outputs open circuited.
2. $0.0V < V_{IN} < V_{DD}$.
3. Applied to \overline{INT} when 3-stated.

AC CHARACTERISTICS – MULTIPLEXED PARALLEL PORT (MUX=1)

(0°C to 70°C; V_{DD}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t _{CYC}	200			ns	
Pulse Width, DS low or \overline{RD} high	PW _{EL}	100			ns	
Pulse Width, DS high or \overline{RD} low	PW _{EH}	100			ns	
Input Rise/Fall times	t _R , t _F			20	ns	
R/W Hold Time	t _{RWH}	10			ns	
R/W Set Up time before DS high	t _{RWS}	50			ns	
\overline{CS} , FS0, FS1 Set Up time before DS, \overline{WR} or \overline{RD} active	t _{CS}	20			ns	
\overline{CS} , FS0, FS1 Hold time	t _{CH}	0			ns	
Read Data Hold time	t _{DHR}	10		50	ns	
Write Data Hold time	t _{DHW}	0			ns	
Muxed Address valid to AS or ALE fall	t _{ASL}	15			ns	
Muxed Address Hold time	t _{AHL}	10			ns	
Delay time DS, \overline{WR} or \overline{RD} to AS or ALE rise	t _{ASD}	20			ns	
Pulse Width AS or ALE high	PW _{ASH}	30			ns	
Delay time, AS or ALE to DS, \overline{WR} or \overline{RD}	t _{ASED}	10			ns	
Output Data Delay time from DS or \overline{RD}	t _{DDR}	20		80	ns	
Data Set Up time	t _{DSW}	50			ns	

See Figures 12–1 to 12–3 for details.

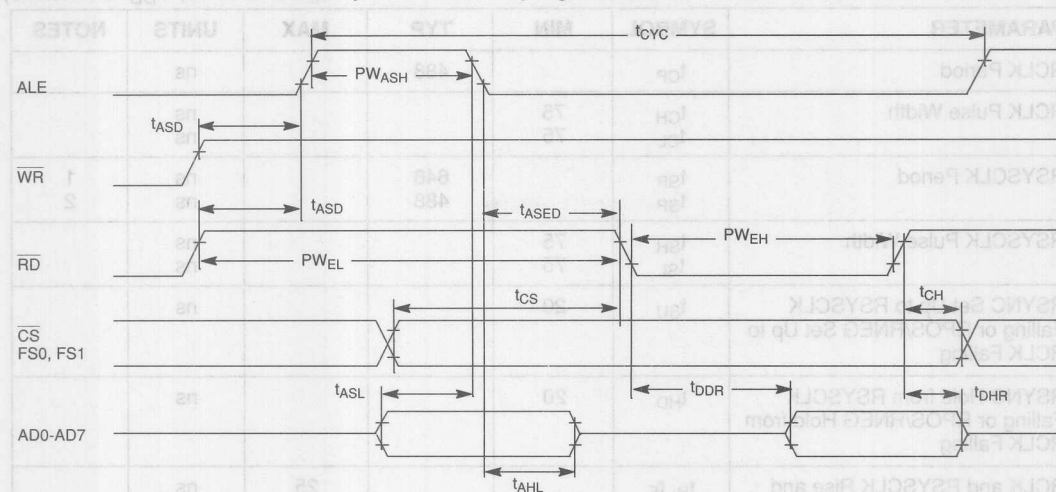
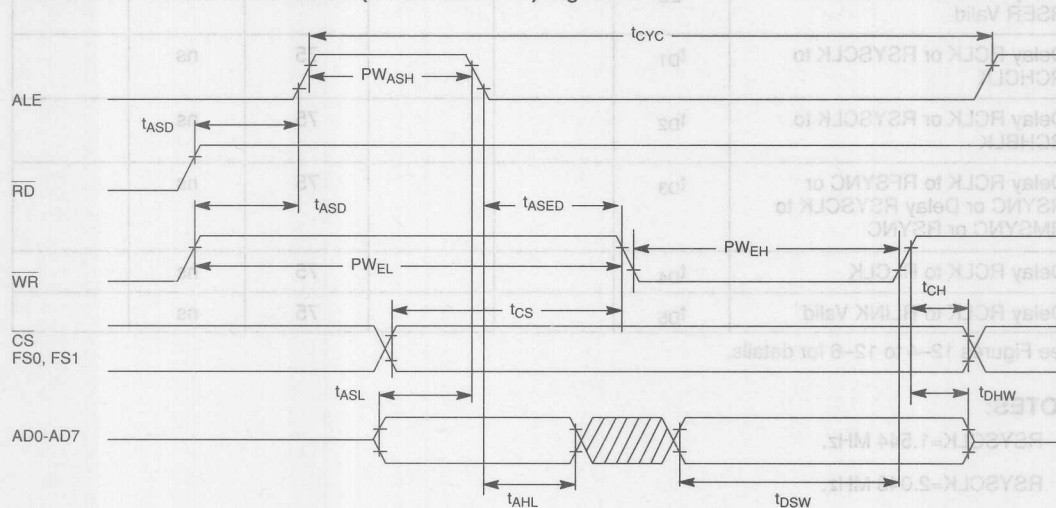
AC CHARACTERISTICS – RECEIVE SIDE (0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{CP}		488		ns	
RCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
RSYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	1 2
RSYSCLK Pulse Width	t_{SH} t_{SL}	75 75			ns ns	
RSYNC Set Up to RSYCLK Falling or RPOS/RNEG Set Up to RCLK Falling	t_{SU}	20			ns	
RSYNC Hold from RSYCLK Falling or RPOS/RNEG Hold from RCLK Falling	t_{HD}	20			ns	
RCLK and RSYCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay RCLK or RSYCLK to RSER Valid	t_{D0}			50	ns	
Delay RCLK or RSYCLK to RCHCLK	t_{D1}			75	ns	
Delay RCLK or RSYCLK to RCHBLK	t_{D2}			75	ns	
Delay RCLK to RFSYNC or RSYNC or Delay RSYCLK to RMSYNC or RSYNC	t_{D3}			75	ns	
Delay RCLK to RLCLK	t_{D4}			75	ns	
Delay RCLK to RLINK Valid	t_{D5}			75	ns	

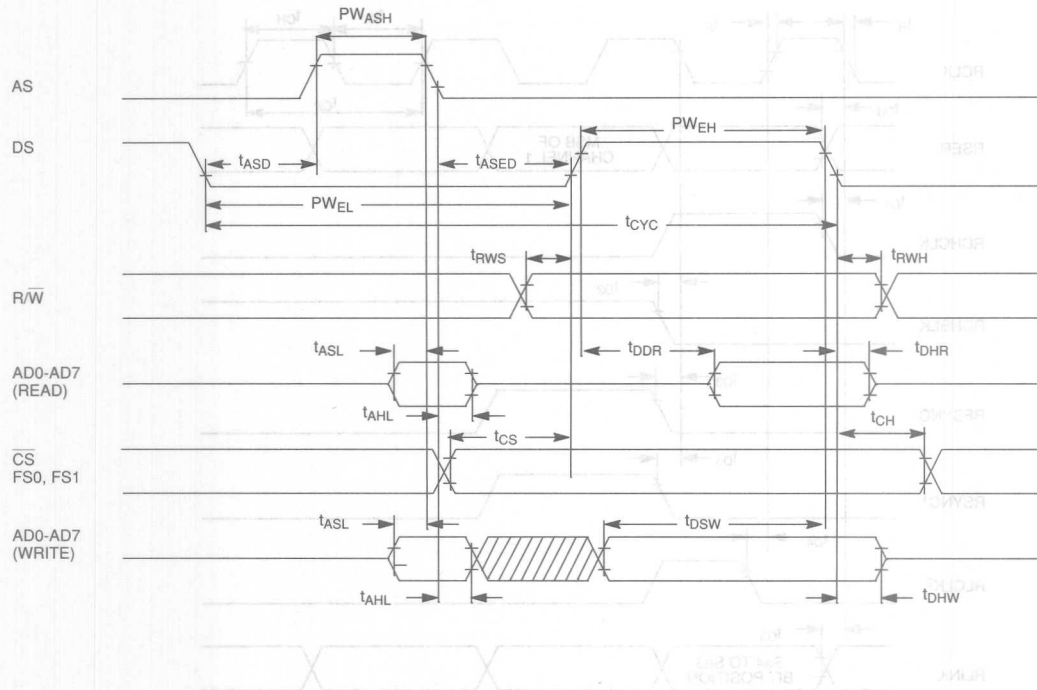
See Figures 12–4 to 12–6 for details.

NOTES:

1. RSYCLK=1.544 MHz.
2. RSYCLK=2.048 MHz.

INTEL BUS READ AC TIMING (BTS=0/MUX=1) Figure 12-1**INTEL BUS WRITE AC TIMING (BTS=0/MUX=1) Figure 12-2**

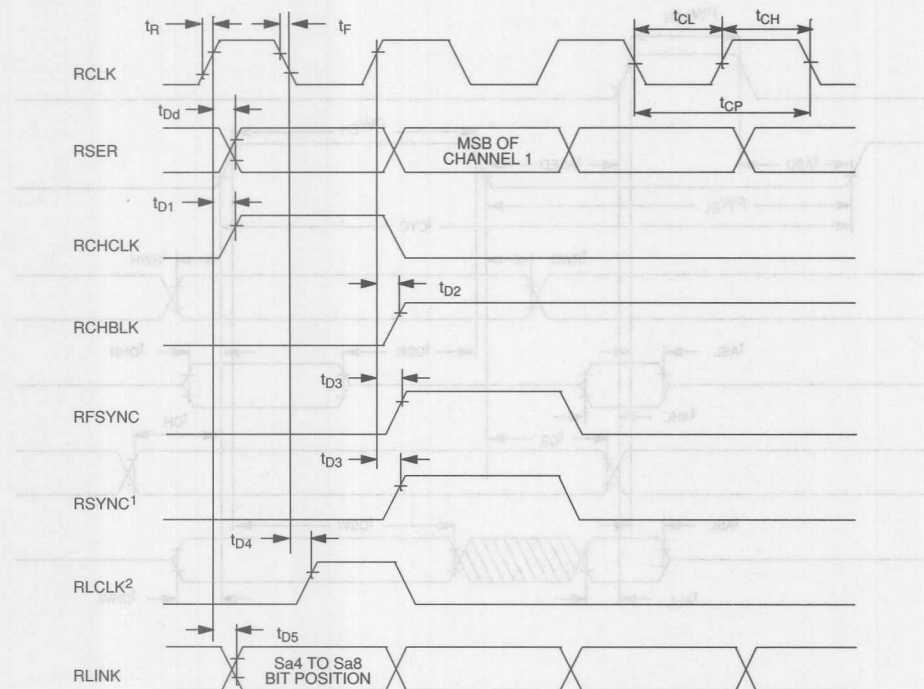
MOTOROLA BUS AC TIMING (BTS=1/MUX=1) Figure 12-3



NOTES:

1. R/W is in the output mode (RCH=0).
2. R/W will only pulse high during 32-bit locations as defined in RCHS; no relationship between R/W and R/W is implied.

RECEIVE SIDE AC TIMING Figure 12-4

**NOTES:**

1. RSYNC is in the output mode (RCR1.5=0).
2. RLCLK will only pulse high during Sa bit locations as defined in RCR2; no relationship between RLCLK and RFSYNC is implied.

AC CHARACTERISTICS – TRANSMIT SIDE (0°C to 70°C; V_{DD}=5V ± 10%)

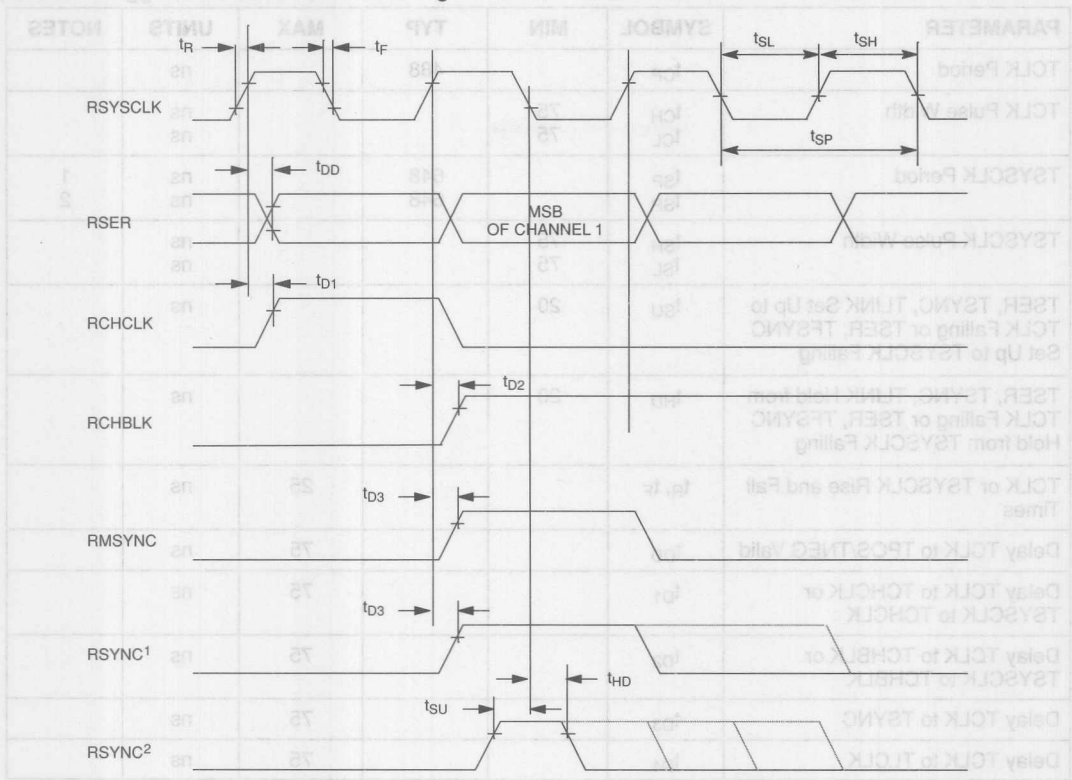
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t _{CP}		488		ns	
TCLK Pulse Width	t _{CH} t _{CL}	75 75			ns ns	
TSYSCLK Period	t _{SP} t _{SP}		648 648		ns ns	1 2
TSYSCLK Pulse Width	t _{SH} t _{SL}	75 75			ns ns	
TSER, TSYNC, TLINK Set Up to TCLK Falling or TSER, TFSYNC Set Up to TSYSCLK Falling	t _{SU}	20			ns	
TSER, TSYNC, TLINK Hold from TCLK Falling or TSER, TFSYNC Hold from TSYSCLK Falling	t _{HD}	20			ns	
TCLK or TSYSCLK Rise and Fall Times	t _R , t _F			25	ns	
Delay TCLK to TPOS/TNEG Valid	t _{DD}			75	ns	
Delay TCLK to TCHCLK or TSYSCLK to TCHCLK	t _{D1}			75	ns	
Delay TCLK to TCHBLK or TSYSCLK to TCHBLK	t _{D2}			75	ns	
Delay TCLK to TSYNC	t _{D3}			75	ns	
Delay TCLK to TLCLK	t _{D4}			75	ns	

See Figures 12–7 to 12–9 for details.

NOTES:

- 1. TSYSCLK=1.544 MHz.
- 2. TSYSCLK=2.048 MHz.

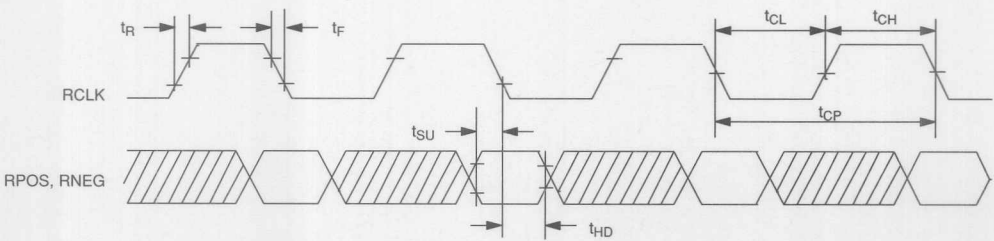
RECEIVE SYSTEM SIDE AC TIMING Figure 12-5



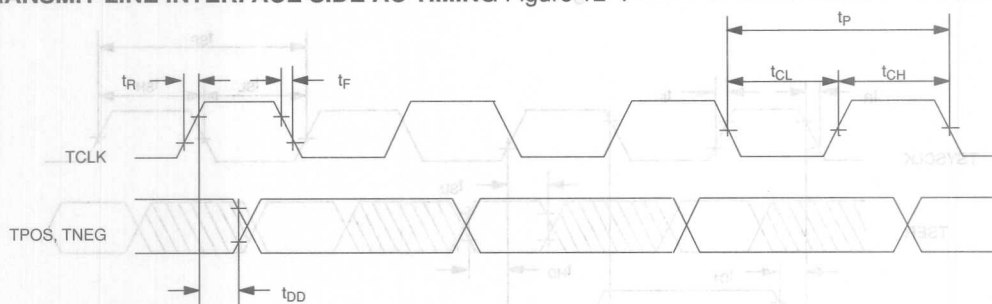
NOTES:

1. RSYNC is in the output mode (RCR 1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).

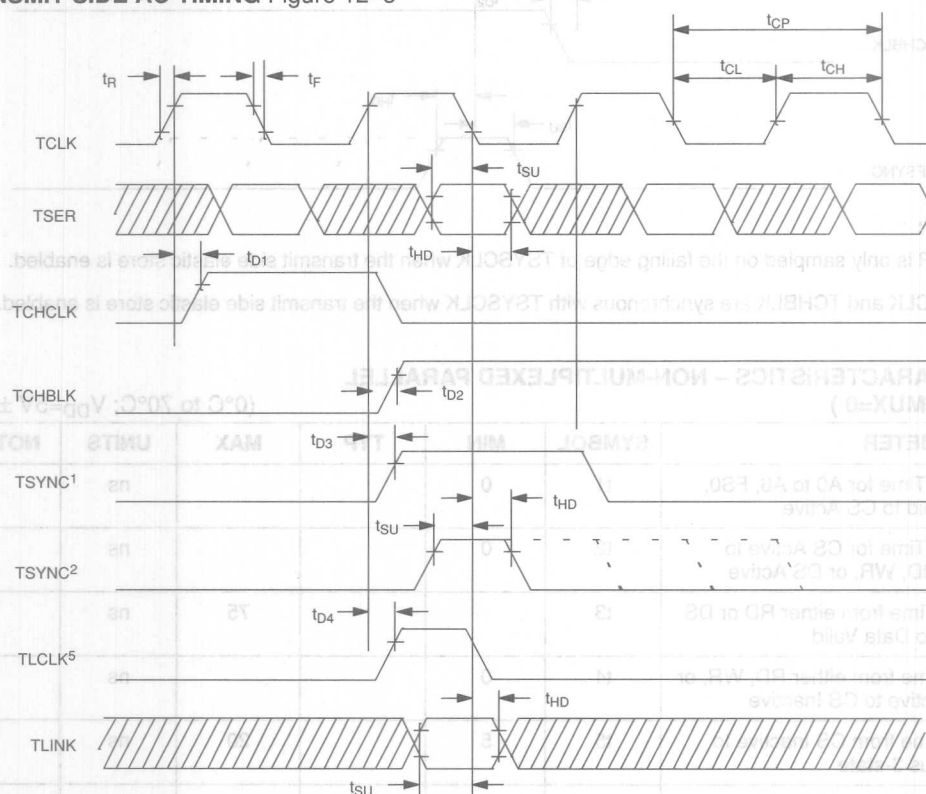
RECEIVE LINE INTERFACE AC TIMING Figure 12-6



TRANSMIT LINE INTERFACE SIDE AC TIMING Figure 12-7

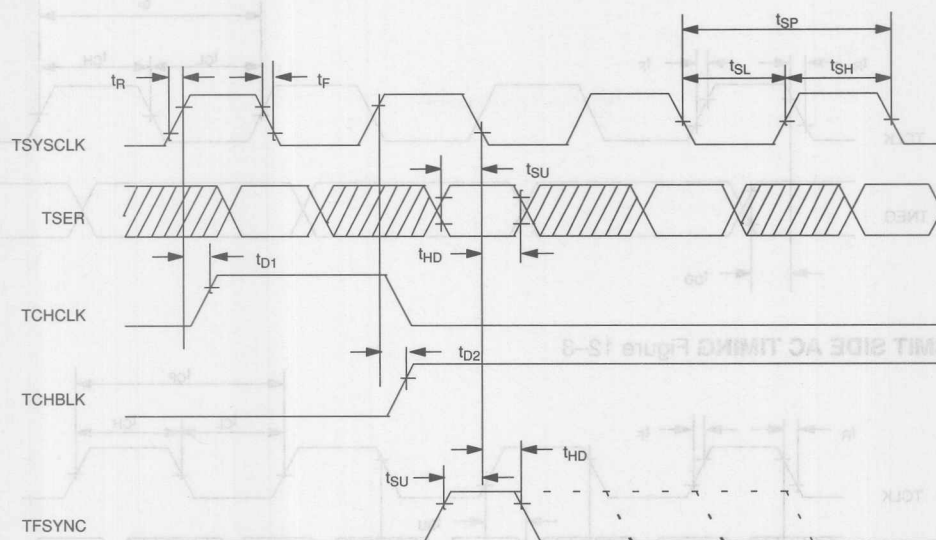


TRANSMIT SIDE AC TIMING Figure 12-8



NOTES:

1. TSYNC is in the output mode (TCR1.0=1).
2. TSYNC is in the input mode (TCR1.0=0).
3. TSER is sampled on the falling edge of TCLK when the transmit side elastic store is disabled.
4. TCHCLK and TCHBLK are synchronous with TCLK when the transmit side elastic store is disabled.
5. TLINK is only sampled during Sa bit locations as defined in TCR2; no relationship between TLCLK/TLINK and TSYNC is implied.

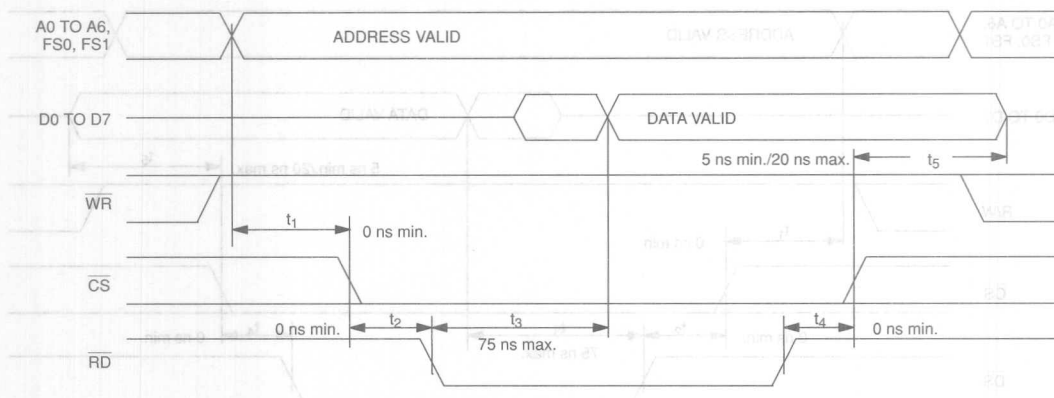
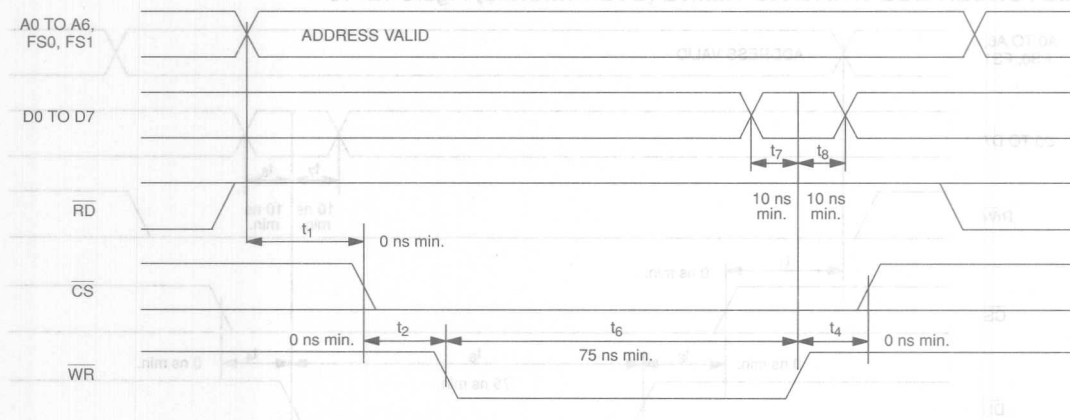
TRANSMIT SYSTEM SIDE AC TIMING Figure 12–9**NOTES:**

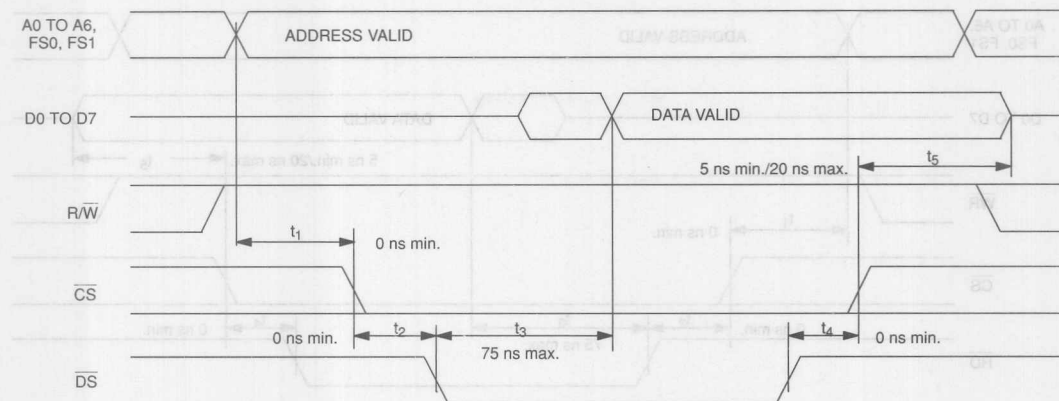
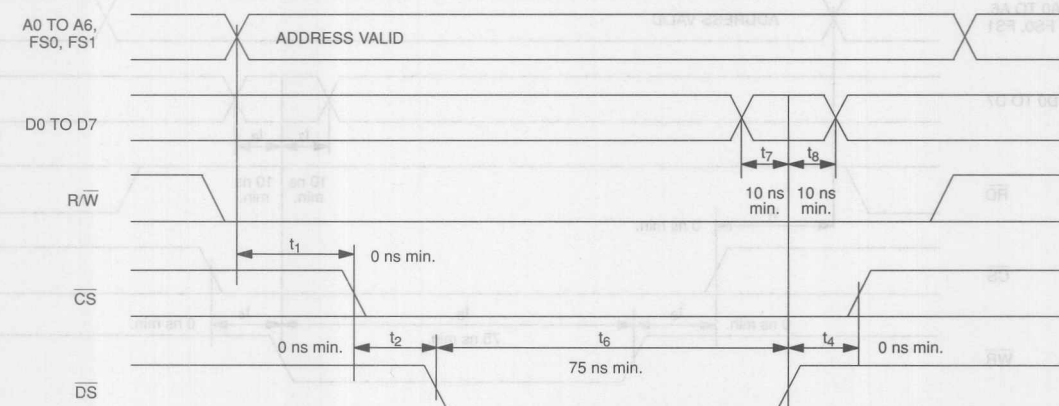
1. TSER is only sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
2. TCHCLK and TCHBLK are synchronous with TSYSCLK when the transmit side elastic store is enabled.

AC CHARACTERISTICS – NON-MULTIPLEXED PARALLEL PORT (MUX=0)(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

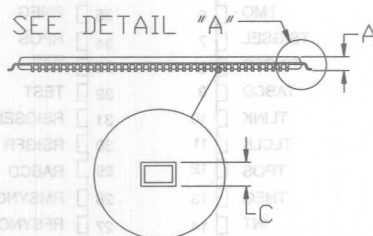
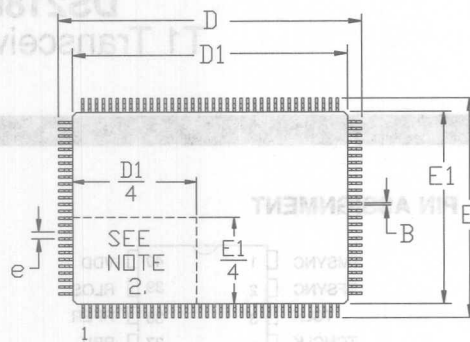
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A6, FS0, FS1 Valid to CS Active	t1	0			ns	
Set Up Time for CS Active to either RD, WR, or DS Active	t2	0			ns	
Delay Time from either RD or DS Active to Data Valid	t3			75	ns	
Hold Time from either RD, WR, or DS Inactive to CS Inactive	t4	0			ns	
Hold Time from CS Inactive to Data Bus 3-state	t5	5		20	ns	
Wait Time from either WR or DS Active to Latch Data	t6	75			ns	
Data Set Up Time to either WR or DS Inactive	t7	10			ns	
Data Hold Time from either WR or DS Inactive	t8	10			ns	

See Figures 12–10 to 12–13 for details.

INTEL BUS READ AC TIMING (BTS=0/MUX=0) Figure 12-10

INTEL BUS WRITE AC TIMING (BTS=0/MUX=0) Figure 12-11


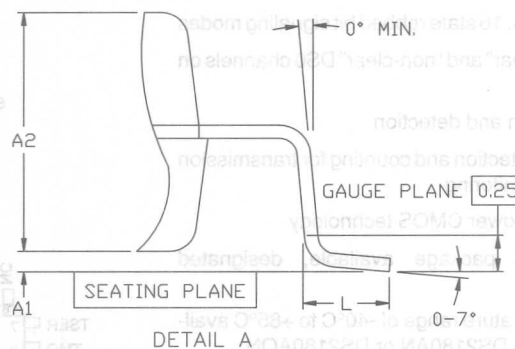
MOTOROLA BUS READ AC TIMING (BTS=1/MUX=0) Figure 12-12

MOTOROLA BUS WRITE AC TIMING (BTS=1/MUX=0) Figure 12-13


DS21Q43A 128 PIN TQFP



NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.



DETAIL A

DIMENSIONS ARE IN MILLIMETERS

PKG	128-PIN	
DIM	MIN	MAX
A	—	1.60
A1	0.05	—
A2	1.35	1.45
B	0.17	0.27
C	0.09	0.20
D	21.80	22.20
D1	20.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75

56-G4011-001

DALLAS

SEMICONDUCTOR

DS2180A

T1 Transceiver

FEATURES

- Single chip DS1 rate transceiver
- Supports common framing standards
 - 12 frames/superframe "193S"
 - 24 frames/superframe "193E"
- Three zero suppression modes
 - B7 stuffing
 - B8ZS
 - Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low-power CMOS technology
- Surface mount package available, designated DS2180AQ
- Industrial temperature range of -40°C to +85°C available, designated DS2180AN or DS2180AQN
- Compatible to DS2186 Transmit Line Interface, DS2187 Receive Line Interface, DS2188 Jitter Attenuator, DS2175 T1/CEPT Elastic Store, DS2290 T1 Isolation Stik, and DS2291 T1 Long Loop Stik

DESCRIPTION

The DS2180A is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

PIN ASSIGNMENT

TMSYNC	1	40	VDD
TFSYNC	2	39	RLOS
TCLK	3	38	RFER
TCHCLK	4	37	RBV
TSER	5	36	RCL
TMO	6	35	RNEG
TSIGSEL	7	34	RPOS
TSIGFR	8	33	RST
TABCD	9	32	TEST
TLINK	10	31	RSIGSEL
TLCLK	11	30	RSIGFR
TPOS	12	29	RABCD
TNEG	13	28	RMSYNC
INT	14	27	RFSYNC
SDI	15	26	RSER
SDO	16	25	RCHCLK
CS	17	24	RCLK
SCLK	18	23	RLCLK
SPS	19	22	RLINK
VSS	20	21	RYEL

40-Pin DIP (600 MIL)

NC	6	TCHCLK	5	TCLK	4	NC	3	TFSYNC	2	TMSYNC	1	VDD	40	RLOS	39	RFER	38	RBV	37	RCL	36	RNEG	35	RPOS	34	RST	33	TEST	32	RSIGSEL	31	RSIGFR	30	RABCD	29	RMSYNC	28	RFSYNC	27	RSER	26	RCHCLK	25	RCLK	24	RLCLK	23	RLINK	22	RYEL	21	VSS	20	SPS	19	SCLK	18	CS	17	SDO	16	SDI	15	INT	14	TNEG	13	TPOS	12	TLCLK	11	TABCD	10	TSIGFR	9	TSIGSEL	8	TMO	7	TSER	6	NC
NC	41	RCL	40	RBV	39	RFER	38	RLOS	37	VDD	36	TMSYNC	35	TFSYNC	34	TCLK	33	TCHCLK	32	NC	31	TSER	30	TMO	29	TSIGSEL	28	TSIGFR	27	TABCD	26	TLINK	25	TLCLK	24	TPOS	23	TNEG	22	INT	21	RSER	20	RCHCLK	19	RMSYNC	18	RABCD	17	RSIGFR	16	RSIGSEL	15	RPOS	14	RNEG	13	RYEL	12	RLINK	11	RLCLK	10	RCLK	9	NC	8	NC	7	NC	6	NC	5	NC	4	NC	3	NC	2	NC	1	NC

44-PIN PLCC

transmit frame/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

The receive synchronizer establishes frame and multi-frame boundaries by identifying frame signaling bits, extracts signaling data, reports alarms and transmission errors, and provides output clocks useful for data conditioning and decoding.

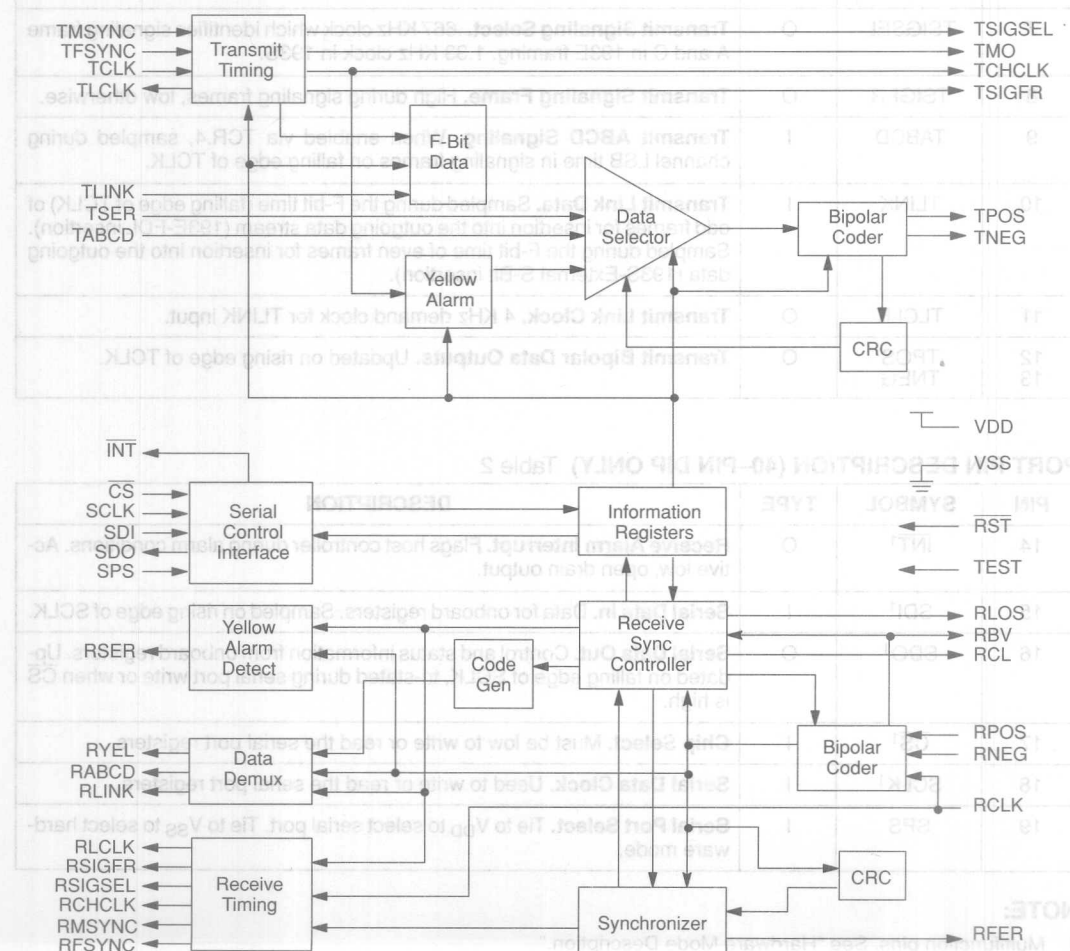
The control block is shared between transmit and receive sides. This block determines the frame, zero sup-

the control block is by one of two means.

In the processor mode, pins 14 through 18 are a micro-processor/microcontroller-compatible serial port which can be used for device configuration, control and status monitoring.

In the hardware mode, no offboard processor is required. Pins 14 through 18 are reconfigured into "hard-wired" select pins. Features such as selection "clear" DS0 channels, insertion of idle code and alteration of sync algorithm are unavailable in the hardware mode.

DS2180A BLOCK DIAGRAM Figure 1



TRANSMIT PIN DESCRIPTION (40-PIN DIP ONLY) Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TMSYNC	I	Transmit Multiframe Sync. May be pulsed high at multiframe boundaries to reinforce multiframe alignment or tied low, which allows internal multiframe counter to free run.
2	TFSYNC	I	Transmit Frame Sync. Rising edge identifies frame boundary; may be pulsed every frame to reinforce internal frame counter or tied low (allowing TMSYNC to establish frame and multiframe alignment).
3	TCLK	I	Transmit Clock. 1.544 MHz primary clock.
4	TCHCLK	O	Transmit Channel Clock. 192 KHz clock which identifies time slot (channel) boundaries. Useful for parallel-to-serial conversion of channel data.
5	TSER	I	Transmit Serial Data. NRZ data input, sample on falling edge of TCLK.
6	TMO	O	Transmit Multiframe Out. Output of internal multiframe counter indicates multiframe boundaries. 50% duty cycle.
7	TSIGSEL	O	Transmit Signaling Select. .667 KHz clock which identifies signaling frame A and C in 193E framing. 1.33 KHz clock in 193S.
8	TSIGFR	O	Transmit Signaling Frame. High during signaling frames, low otherwise.
9	TABCD	I	Transmit ABCD Signaling. When enabled via TCR.4, sampled during channel LSB time in signaling frames on falling edge of TCLK.
10	TLINK	I	Transmit Link Data. Sampled during the F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-Bit insertion).
11	TLCLK	O	Transmit Link Clock. 4 KHz demand clock for TLINK input.
12 13	TPOS TNEG	O	Transmit Bipolar Data Outputs. Updated on rising edge of TCLK.

PORT PIN DESCRIPTION (40-PIN DIP ONLY) Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
14	INT ¹	O	Receive Alarm Interrupt. Flags host controller during alarm conditions. Active low, open drain output.
15	SDI ¹	I	Serial Data In. Data for onboard registers. Sampled on rising edge of SCLK.
16	SDO ¹	O	Serial Data Out. Control and status information from onboard registers. Updated on falling edge of SCLK, tri-stated during serial port write or when CS is high.
17	CS ¹	I	Chip Select. Must be low to write or read the serial port registers.
18	SCLK ¹	I	Serial Data Clock. Used to write or read the serial port registers.
19	SPS	I	Serial Port Select. Tie to V _{DD} to select serial port. Tie to V _{SS} to select hardware mode.

NOTE:

1. Multifunction pins. See "Hardware Mode Description."

POWER AND TEST PIN DESCRIPTION (40-PIN DIP ONLY) Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
20	V _{SS}	—	Signal Ground. 0.0 volts.
32	TEST	I	Test Mode. Tie to V _{SS} for normal operation.
40	V _{DD}	—	Positive Supply. 5.0 volts.

RECEIVE PIN DESCRIPTION (40-PIN DIP ONLY) Table 4

PIN	SYMBOL	TYPE	DESCRIPTION
21	RYEL	O	Receive Yellow Alarm. Transitions high when yellow alarm detected, goes low when alarm clears.
22	RLINK	O	Receive Link Data. Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	RLCLK	O	Receive Link Clock. 4 KHz demand clock for RLINK.
24	RCLK	I	Receive Clock. 1.544 MHz primary clock.
25	RCHCLK	O	Receive Channel Clock. 192 KHz clock identifies time slot (channel) boundaries.
26	RSER	O	Receive Serial Data. Received NRZ serial data, updated on rising edges of RCLK.
27	RFSYNC	O	Receive Frame Sync. Extracted 8 KHz clock, one RCLK wide, indicates F-Bit position in each frame.
28	RMSYNC	O	Receive Multiframe Sync. Extracted multiframe sync; edge indicates start of multiframe, 50% duty cycle.
29	RABCD	O	Receive ABCD Signaling. Extracted signaling data output, valid for each channel time in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
30	RSIGFR	O	Receive Signaling Frame. High during signaling frames, low during resync and non-signaling frames.
31	RSIGSEL	O	Receive Signaling Select. In 193E framing a .667 KHz clock which identifies signaling frames A and C. A 1.33 KHz clock in 193S.
33	RST	I	Reset. A high-low transition clears all internal registers and resets receive side counters. A high-low-high transition will initiate a receive resync.
34 35	RPOS RNEG	I	Receive Bipolar Data Inputs. Samples on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
36	RCL	O	Receive Carrier Loss. High if 32 consecutive 0's appear at RPOS and RNEG; goes low after next 1.
37	RBV	O	Receive Bipolar Violation. High during accused bit time at RSER if bipolar violation detected, low otherwise.
38	RFER	O	Receive Frame Error. High during F-Bit time when F _T or F _S errors occur (193S) or when FPS or CRC errors occur (193E). Low during resync.
39	RLOS	O	Receive Loss of Sync. Indicates sync status; high when internal resync is in progress, low otherwise.

REGISTER SUMMARY Table 5

REGISTER	ADDRESS	T/R ¹	DESCRIPTION/FUNCTION
RSR	0000	R ²	Receive Status Register. Reports all receive alarm conditions.
RIMR	0001	R	Receive Interrupt Mask Register. Allows masking of individual alarm-generated interrupts.
BVCR	0010	R	Bipolar Violation Count Register. 8-bit presetable counter which records individual bipolar violations.
ECR	0011	R	Error Count Register. Two independent 4-bit counters which record OOF occurrences and individual frame bit or CRC errors.
CCR ³	0100	T/R	Common Control Register. Selects device operating characteristics common to receive and transmit sides.
RCR ³	0101	R	Receive Control Register. Programs device operating characteristics unique to the receive side.
TCR ³	0110	T	Transmit Control Register. Selects additional transmit side modes.
TIR1	0111	T	Transmit Idle Registers. Designate which outgoing channels are to be substituted with idle code.
TIR2	1000	T	
TIR3	1001	T	
TTR1	1010	T	Transmit Transparent Registers. Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
TTR2	1011	T	
TTR3	1100	T	
RMR1	1101	R	Receive Mark Registers. Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control of RCR).
RMR2	1110	R	
RMR3	1111	R	

NOTES:

1. Transmit or receive side register.
2. RSR is a read only register; all other registers are read/write.
3. Reserved bit locations in the control registers should be programmed to 0 to maintain compatibility with future transceiver products.

SERIAL PORT INTERFACE

Pins 14 through 18 of the DS2180A serve as a microprocessor/microcontroller-compatible serial port. Sixteen onboard registers allow the user to update operational characteristics and monitor device status via host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads and/or writes by the host.

ADDRESS/COMMAND

Reading or writing the control, configuration or status registers requires writing one address command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. The following 4-bit nibble identifies regis-

ter address. The next two bits are reserved and must be set to 0 for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. *Data is written to and read from the transceiver LSB first.*

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the \overline{CS} input low. Input data is latched on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held on the next falling edge. All data transfers are terminated if the \overline{CS} input transitions high. Port control logic is disabled and SDO is tri-stated when \overline{CS} is high.

DATA I/O

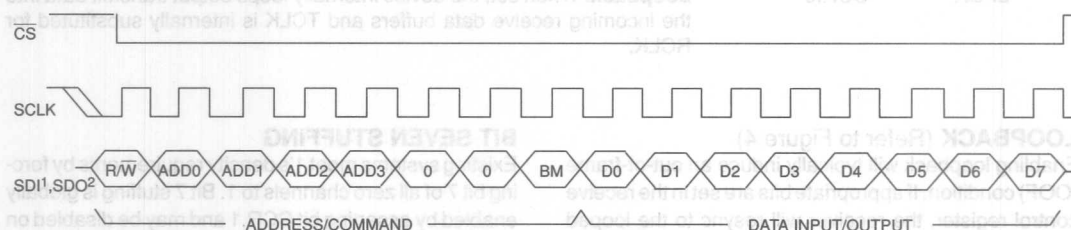
Following the eight SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edges of the next eight SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next eight SCLK cycles. The SDO pin is tri-stated during device write and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE

The burst mode allows all onboard registers to be consecutively read and written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power-up or system reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. Burst is terminated by a low-high transition on CS.

ACB: ADDRESS COMMAND BYTE Figure 2

(MSB)				(LSB)			
BM	—	—	ADD3	ADD2	ADD1	ADD0	R/W
SYMBOL	POSITION	NAME AND DESCRIPTION					
BM	ACB.7	Burst Mode. If set (and ACB.1 through ACB.4=0) burst read or write is enabled.					
—	ACB.6	Reserved, must be 0 for proper operation.					
—	ACB.5	Reserved, must be 0 for proper operation.					
ADD3	ACB.4	MSB of register address.					
ADD0	ACB.1	LSB of register address.					
R/W	ACB.0	Read/Write Select. 0 = write addressed register. 1 = read addressed register.					

SERIAL PORT READ/WRITE Figure 3**NOTES:**

- SDI sampled on rising edge of SCLK.
- SDO updated on falling edge of SCLK.

COMMON CONTROL REGISTER Figure 4

(MSB)		(LSB)	
SYMBOL	POSITION	NAME AND DESCRIPTION	
—	CCR.7	Reserved, must be 0 for proper operation.	
FRSR2	CCR.6	Function of REC Status Register 2. 0 = Detected B8ZS code words reported at RSR.2. 1 = COFA (Change-of-Frame Alignment) reported at RSR.2 when last re-sync resulted in change of frame or multiframe alignment.	
EYELMD	CCR.5	193E Yellow Mode Select. 0 = Yellow alarm is a repeating pattern set of 00 hex and FF hex. 1 = Yellow alarm is a 0 in the bit 2 position of all channels.	
FM	CCR.4	Frame Mode Select. 0 = D4 (193S, 12 frames/superframe). 1 = Extended (193E, 24 frames/superframe).	
SYELMD	CCR.3	193S Yellow Mode Select. Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a 1 in the S-bit position of frame 12; if cleared, yellow alarm is a 0 in bit 2 of all channels. Does not affect 193E yellow alarm operation.	
B8ZS	CCR.2	Bipolar eight zero substitution. 0 = No B8ZS. 1 = B8ZS enabled. (Note: This bit must be set to 0 when CCR.1=1)	
B7	CCR.1	Bit seven zero suppression. If CCR.1=1, channels with an all zero content will be transmitted with bit 7 forced to 1. If CCR.1=0, no bit 7 stuffing occurs. (Note: This bit must be set to 0 when CCR.2=1)	
LPBK	CCR.0	Loopback. When set, the device internally loops output transmit data into the incoming receive data buffers and TCLK is internally substituted for RCLK.	

LOOPBACK (Refer to Figure 4)

Enabling loopback will typically induce an out-of-frame (OOF) condition. If appropriate bits are set in the receive control register, the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit unframed all 1's. All operating modes (B8ZS, alarm, signaling, etc.) except for blue alarm transmission are available in loopback.

BIT SEVEN STUFFING

Existing systems meet 1's density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is globally enabled by asserting bit CCR.1 and may be disabled on an individual channel basis by setting appropriate bits in TTR1–TTR3. Bit 7 stuffing and B8ZS modes should not be enabled simultaneously. Enabling both results in LOS.

B8ZS

The DS2180A supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system 1's density requirements without disturbing data integrity as required in emerging clear channel

applications. B8ZS coding replaces eight consecutive outgoing 0's with a B8ZS code word. Any received B8ZS code word is replaced with all 0's. B8ZS and bit 7 stuffing modes should not be enabled simultaneously. Enabling both results in LOS.

TCR: TRANSMIT CONTROL REGISTER Figure 5

(MSB)				(LSB)			
ODF	TFPT	TCP	RBSE	TIS	193SI	TBL	TYEL
SYMBOL		POSITION	NAME AND DESCRIPTION				
ODF		TCR.7	Output Data Format. 0 = Bipolar data at TPOS and TNEG. 1 = NRZ data at TPOS; TNEG=0.				
TFPT		TCR.6	Transmit Framing Pass-through. 0 = FT/FPS sourced internally. 1 = FT/FPS sampled at TSER during F-bit time.				
TCP		TCR.5	Transmit CRC Pass-through. 0 = Transmit CRC code internally generated. 1 = TSER sampled at CRC F-bit time for external CRC insertion.				
RBSE		TCR.4	Robbed Bit Signaling Enable. 1 = Signaling inserted in all channels during signaling frames. 0 = No signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DS0 channels.)				
TIS		TCR.3	Transmit Idle Code Select. Determines idle code format to be inserted into channels marked by the TIR registers. 0 = Insert 7F (Hex) into marked channels. 1 = Insert FF (Hex) into marked channels.				
193SI		TCR.2	193S S-bit Insertion. Determines source of transmitted S-bit. 0 = Internal S-bit generator. 1 = External (sampled at TLINK input).				
TBL		TCR.1	Transmit Blue Alarm. 0 = Disabled. 1 = Enabled.				
TYEL		TCR.0	Transmit Yellow Alarm. 0 = Disabled. 1 = Enabled.				

TRANSMIT BLUE ALARM

The blue alarm (also known as the AIS, Alarm Indication Signal) is an unframed, all 1's sequence enabled by asserting TCR.1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR.1. Use of the TIR registers allows a framed, all 1's alarm transmission if required by the network.

TRANSMIT YELLOW ALARM

In 193E framing, a yellow alarm is a repeating pattern set of FF(Hex) and 00 (Hex) on the 4 KHz facility data link (FDL). In 193S framing the yellow alarm format is dependent on the state of bit CCR.3. In all modes, yellow alarm is enabled by asserting TCR.0 and disabled by clearing TCR.0.

TRANSMIT SIGNALING

When enabled (via TCR.4) channel signaling is inserted in frames 6 and 12 (193S) or in frames 6, 12, 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge

of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allows external multiplexing of separate serial links for A, B or A, B, C, D signaling sources.

TTR1–TTR3: TRANSMIT TRANSPARENCY REGISTERS Figure 6

(MSB)						(LSB)		
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3

SYMBOL POSITION

CH24 TTR3.7
CH1 TTR1.0

NAME AND DESCRIPTION

Transmit Transparent Registers. Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel is transparent.

TIR1–TIR3: TRANSMIT IDLE REGISTERS Figure 7

(MSB)						(LSB)		
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3

SYMBOL POSITION

CH24 TIR3.7
CH1 TIR1.0

NAME AND DESCRIPTION

Transmit Idle Registers. Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR.2.

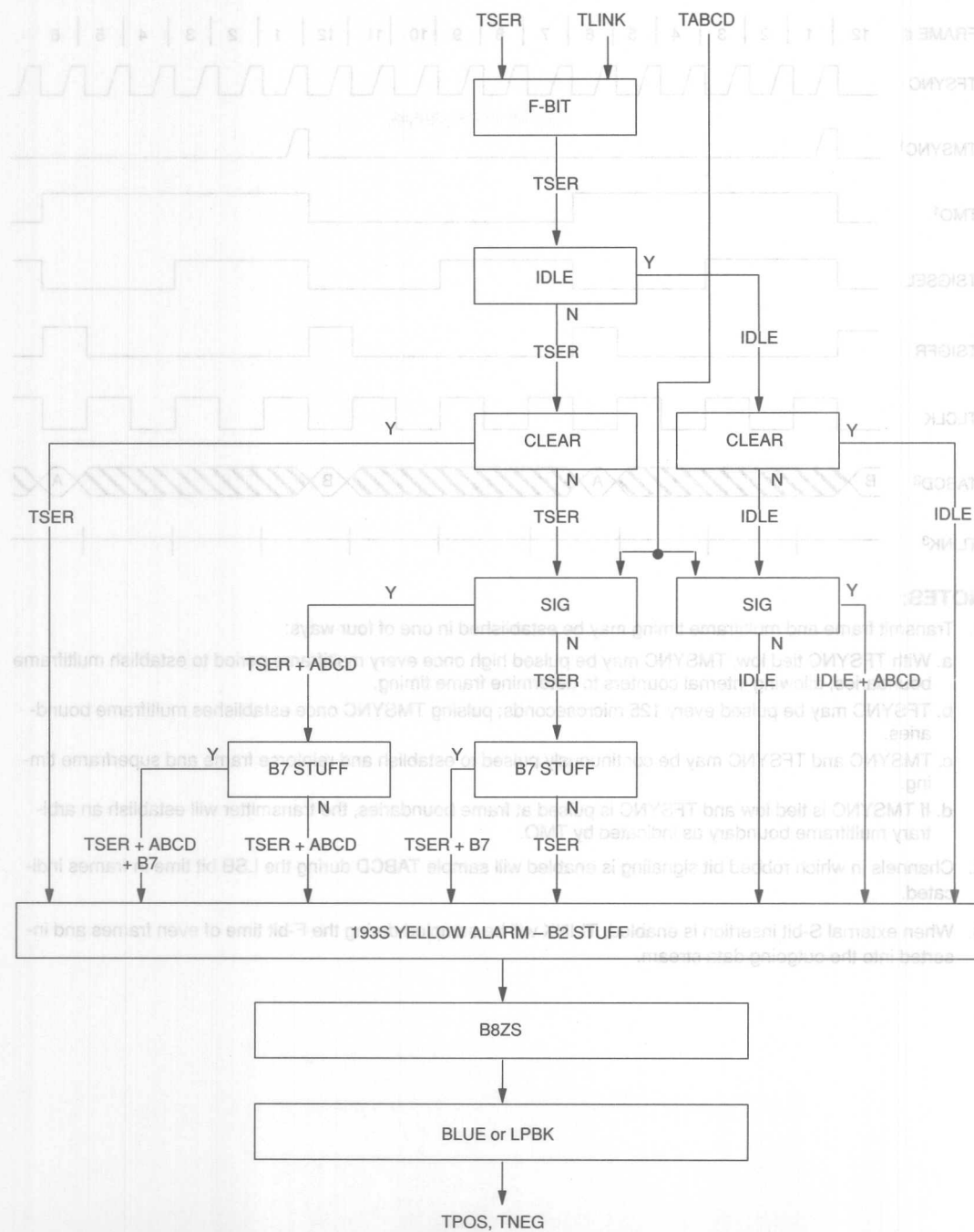
TRANSMIT CHANNEL TRANSPARENCY

Individual DS0 channels in the T1 frame may be programmed clear (no inserted robbed bit signaling and no bit 7 zero suppression) by setting the appropriate bits in the transmit transparency registers. Channel transparency is required in mixed voice/data or data-only environments such as ISDN, where data integrity must be maintained.

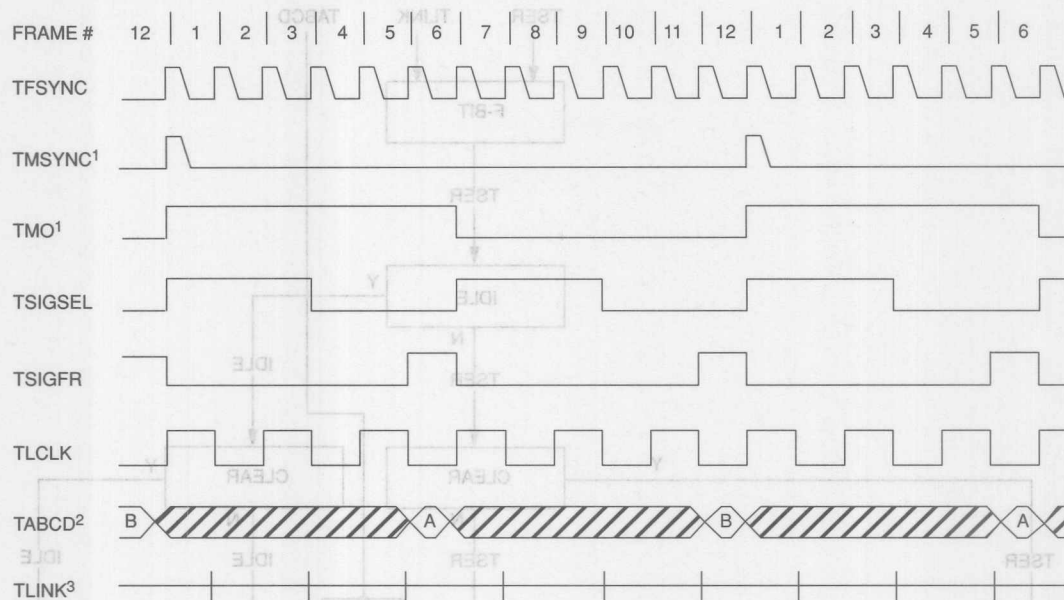
TRANSMIT IDLE CODE INSERTION

Individual outgoing channels in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR.3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates external hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream.

TRANSMIT INSERTION HIERARCHY Figure 8

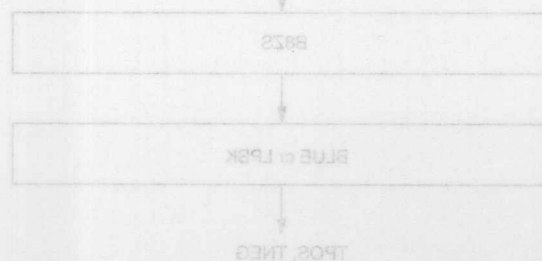


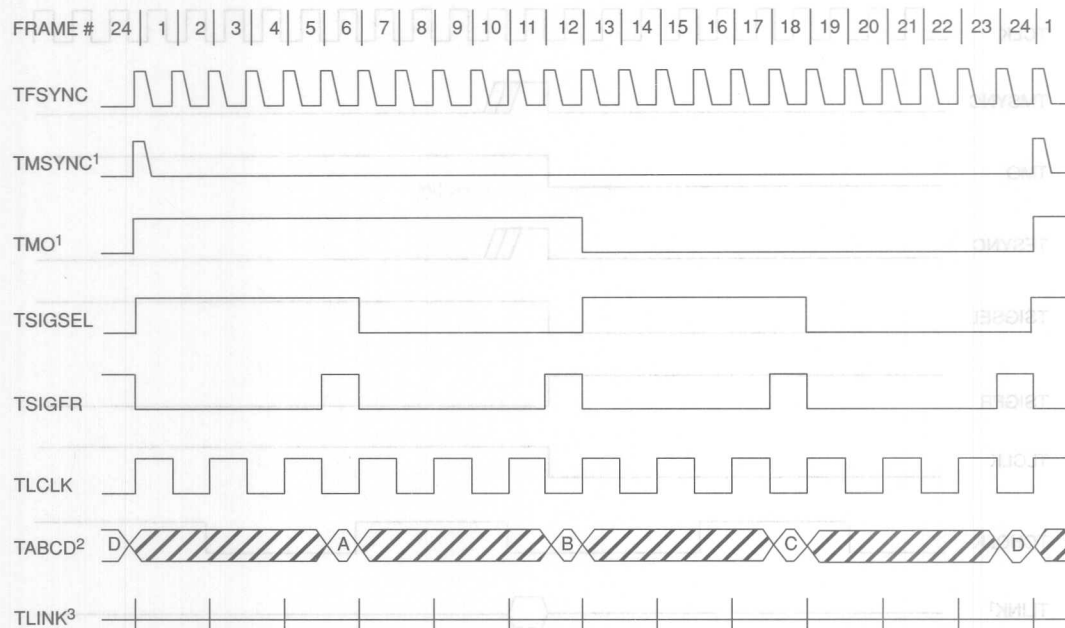
193S TRANSMIT MULTIFRAME TIMING Figure 8



NOTES:

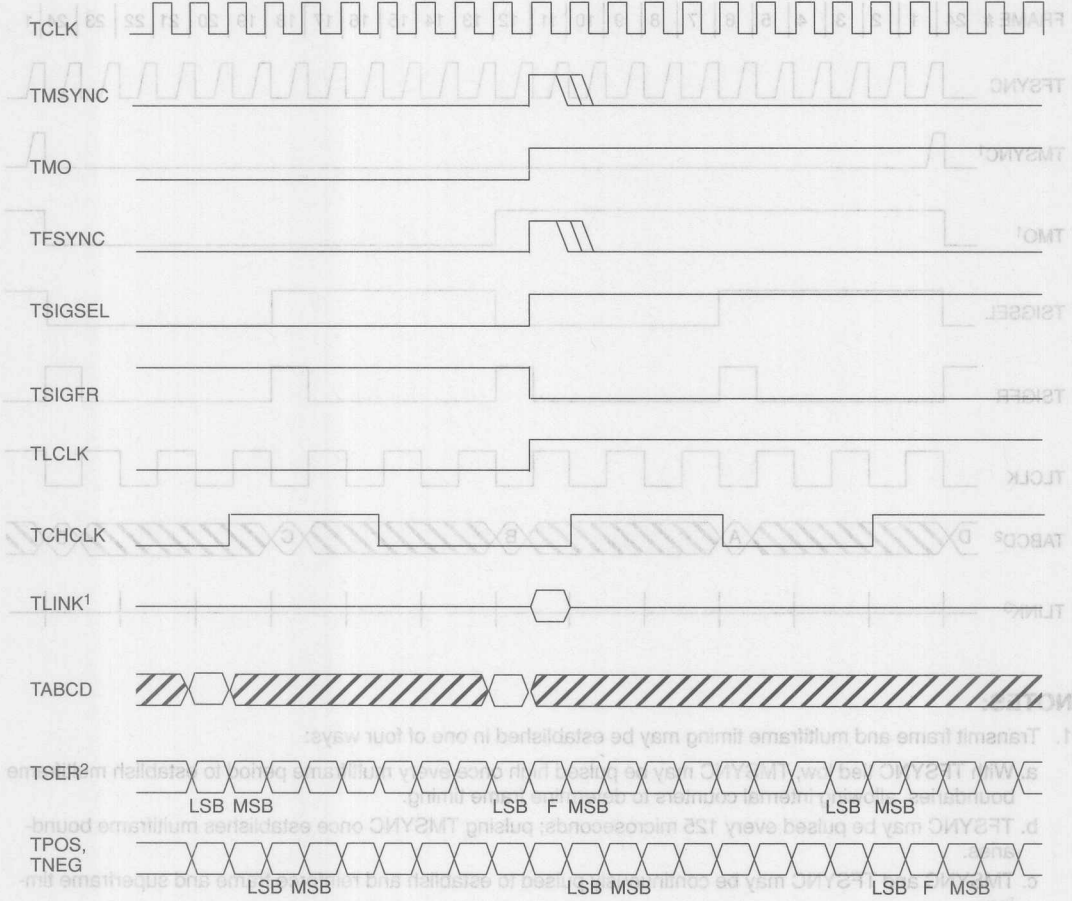
1. Transmit frame and multiframe timing may be established in one of four ways:
 - a. With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
 - b. TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
 - c. TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
 - d. If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. When external S-bit insertion is enabled, TLINK will be sampled during the F-bit time of even frames and inserted into the outgoing data stream.



193E TRANSMIT MULTIFRAME TIMING Figure 10**NOTES:**

1. Transmit frame and multiframe timing may be established in one of four ways:
 - a. With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
 - b. TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
 - c. TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
 - d. If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. TLINK is sampled during the F-bit time of odd frames and inserted into the outgoing data stream (FDL data).

TRANSMIT MULTIFRAME BOUNDARY TIMING Figure 11



NOTES:

1. TLINK timing shown is for 193E framing; in 193E framing, TLINK is sampled as indicated for insertion into F-bit position of odd frames. When S-bit insertion is enabled in 193S, TLINK is sampled during even frames.
2. If TCR.5=1, TSER is sampled during the F-bit time of CRC frames for insertion into the outgoing data stream (193E framing only).

RECEIVE CONTROL REGISTER Figure 12

(MSB)							(LSB)
ARC	OOF	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC
SYMBOL	POSITION	NAME AND DESCRIPTION					
ARC	RCR.7	Auto Resync Criteria. 0 = Resync on OOF or RCL event. 1 = Resync on OOF only.					
OOF	RCR.6	Out-of-frame (OOF) Condition Detection. 0 = 2 of 4 framing bits in error. 1 = 2 of 5 framing bits in error.					
RCI	RCR.5	Receive Code Insert. When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.					
RCS	RCR.4	Receive Code Select. 0 = Idle code (7F Hex). 1 = Digital milliwatt.					
SYNCC	RCR.3	Sync Criteria. Determines the type of algorithm utilized by the receive synchronizer and differs for each frame mode. 193S Framing (CCR.4=0). 0 = Synchronize to frame boundaries using F_T pattern, then search for multiframe by using F_S . 1 = Cross couple F_T and F_S patterns in sync algorithm. 193E Framing (CCR.4=1). 0 = Normal sync (utilizes FPS only). 1 = Validate new alignment with CRC before declaring sync.					
SYNCT	RCR.2	Sync Time. If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.					
SYNCE	RCR.1	Sync Enable. If clear, the transceiver will automatically begin a resync if two of the previous four or five framing bits were in error or if carrier loss is detected. If set, no auto resync occurs.					
RESYNC	RCR.0	Resync. When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.					

RECEIVE CODE INSERTION

Incoming receive channels can be replaced with idle (7F Hex) or digital milliwatt (μ -LAW format) codes. The receive mark registers indicate which channels are inserted. When set, bit RCR.5 serves as a "global" enable for marked channels and bit RCR.4 selects inserted code format: 0 = idle code, 1 = digital milliwatt.

RECEIVE SYNCHRONIZER

Bits RCR.0 through RCR.3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate qualify testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

RECEIVE SIGNALING

Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

coming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

RMR1–RMR3: RECEIVE MARK REGISTERS Figure 13

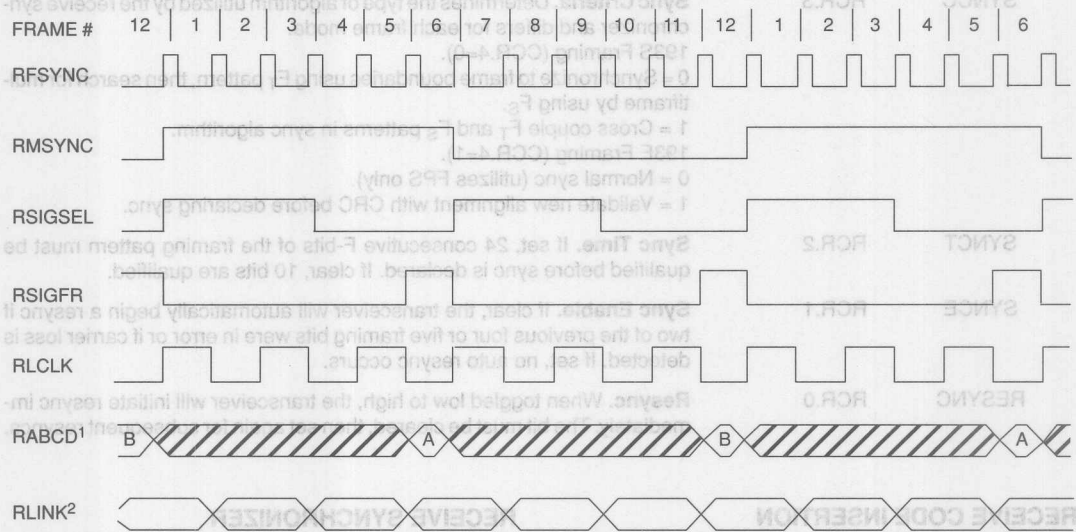
(MSB)						(LSB)		
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3

SYMBOL **POSITION** **NAME AND DESCRIPTION**

CH24 RMR3.7 **Receive Mark Registers.** Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set, the corresponding channel will output codes determined by RCR.4 and RCR.5.

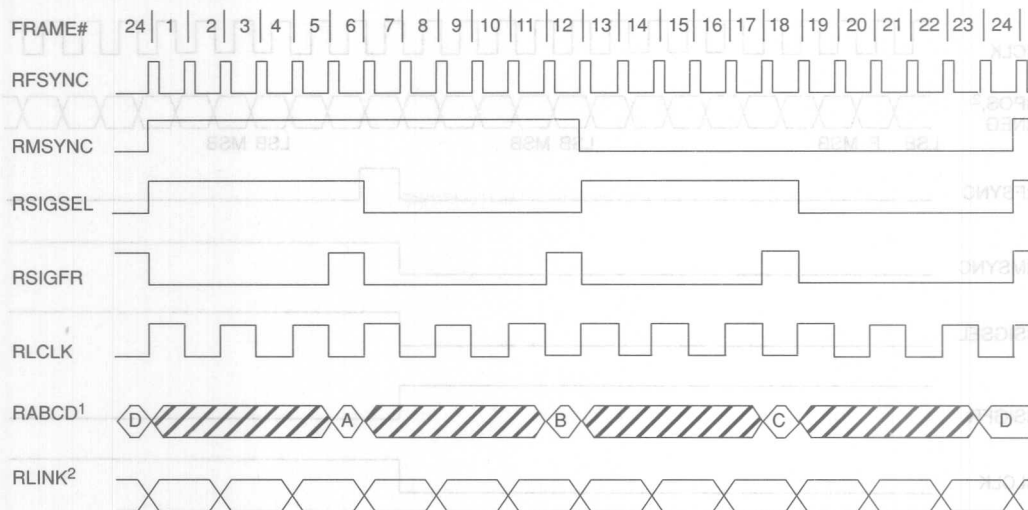
CH1 RMR1.0

193S RECEIVE MULTIFRAME TIMING Figure 14



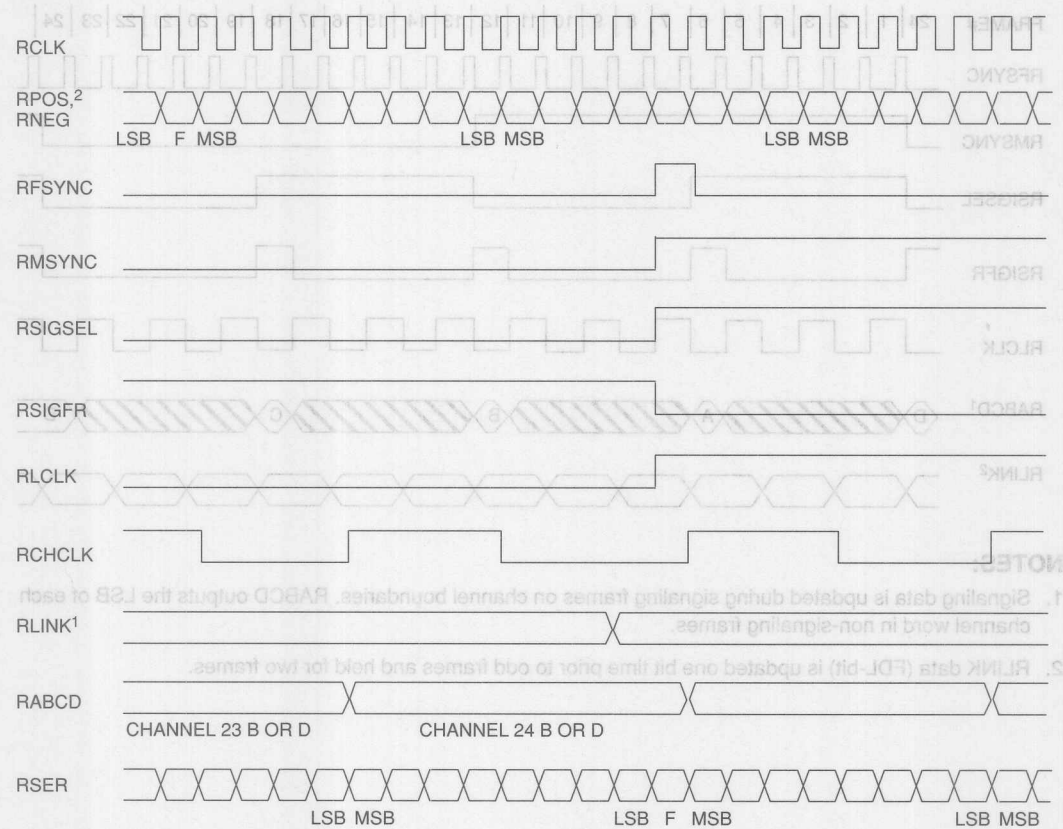
NOTES:

1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

193E RECEIVE MULTIFRAME TIMING Figure 15**NOTES:**

1. Signaling data is updated during signaling frames on channel boundaries. RABCD outputs the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit time prior to odd frames and held for two frames.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 16



NOTES:

1. RLINK timing is shown for 193E; in 193S, RLINK is updated on even frame boundaries and is held across multiframe edges.
2. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.

BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION					
BVCS	RSR.7	Bipolar Violation Count Saturation. Set when the 8-bit counter at BVCR saturates.					
ECS	RSR.6	Error Count Saturation. Set when either of the 4-bit counters at ECR saturates.					
RYEL	RSR.5	Receive Yellow Alarm. Set when yellow alarm detected. (Detected yellow alarm format determined by CCR.4 and CCR.3.)					
RCL	RSR.4	Receive Carrier Loss. Set when 32 consecutive 0's appear at RPOS and RNEG.					
FERR	RSR.3	Frame Bit Error. Set when F_T (193S) or F_P (193E) bit error occurs.					
B8ZSD	RSR.2	Bipolar Eight Zero Substitution Detect. Set when B8ZS code word detected.					
RBL	RSR.1	Receive Blue Alarm. Set when two consecutive frames have less than three 0's (total) in the data stream (F-bit positions not tested).					
RLOS	RSR.0	Receive Loss of Sync. Set when resync is in process; if RCR.1=0, RLOS transitions high on an OOF event or carrier loss indicating auto resync.					

RECEIVE ALARM REPORTING

Incoming serial data is monitored by the transceiver for alarm occurrences. Alarm conditions are reported in two ways: via transitions on the alarm output pins and registered interrupt, in which the host controller reads the RSR in response to an alarm-driven interrupt. Interrupts may be direct, in which the transceiver demands service for a real-time alarm, or count-overflow triggered, in which an onboard alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register (RIMR).

ALARM SERVICING

The host controller must service the transceiver in order to clear an interrupt condition. Clearing appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupt (those driven from real-time alarms) will be cleared when the RSR is directly read unless the alarm condition still exists. Count-overflow interrupts (BVCS, ECS) are not cleared by a direct read of the RSR. They will be cleared only when the user presets the appropriate count register to a value other than all 1's. A burst read of the RSR will not clear an interrupt condition.

RIMR: RECEIVE INTERRUPT MASK REGISTER Figure 18

(MSB)				(LSB)			
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION		POSITION	SYMBOL		
BVCS	RIMR.7	Bipolar Violation Count Saturation Mask. 1 = Interrupt masked. 0 = Interrupt masked.			BVCS		
ECS	RIMR.6	Error Count Saturation Mask. 1 = Interrupt enabled. 0 = Interrupt masked.			ECS		
RYEL	RIMR.5	Receive Yellow Alarm Mask. 1 = Interrupt enabled. 0 = Interrupt masked.			RYEL		
RCL	RIMR.4	Receive Carrier Loss Mask. 1 = Interrupt enabled. 0 = Interrupt masked.			RCL		
FERR	RIMR.3	Frame Bit Error Mask. 1 = Interrupt enabled. 0 = Interrupt masked.			FERR		
B8ZSD	RIMR.2	B8ZS Detect Mask. 1 = Interrupt enabled. 0 = Interrupt masked.			B8ZSD		
RBL	RIMR.1	Receive Blue Alarm Mask. 1 = Interrupt enabled. 0 = Interrupt masked.			RBL		
RLOS	RIMR.0	Receive Loss of Sync Mask. 1 = Interrupt enabled. 0 = Interrupt masked.			RLOS		

ALARM COUNTERS

The three onboard alarm event counters allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presettable by the user establishing an event count interrupt threshold. As each counter saturates, the next error event occurrence will set a bit in the RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

OOF EVENTS AND ERRORED SUPERFRAMES

Out of frame is declared when at least two of four (or five) consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S; the FPS bits are tested in 193E. OOF events are recorded by the 4-bit OOF counter in the error counter register. In the 193E framing mode, the OOF event is logically OR'ed with an on-chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4-bit ESF error counter in the error count register. In the 193S framing mode, the 4-bit ESF error counter records individual F_T and F_S errors when RCR.3=1 or F_T errors only when RCR.3=0.

BVCR: BIPOLAR VIOLATION COUNT REGISTER Figure 19

(MSB)				(LSB)			
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0
SYMBOL	POSITION	NAME AND DESCRIPTION					
BVD7	BVCR.7	MSB of bipolar count.					
BVD0	BVCR.0	LSB of bipolar count.					

This 8-bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation once saturated (RIMR.7=1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "up" to saturation

from the preset value and may be read at any time. Counter increments occur at all times and are not disabled by resync. If B8ZS is enabled (CCR.2=1) bipolar violations are not counted for B8ZS code words.

ECR: ERROR COUNT REGISTER Figure 20

(MSB)				(LSB)			
OOFD3	OOFD2	OOFD1	OOFD0	ESFD3	ESFD2	ESFD1	ESFD0
← ERROR COUNT →				← ESF ERROR COUNT →			
SYMBOL	POSITION	NAME AND DESCRIPTION					
OOFD3	ECR.7	MSB of OOF event count.					
OOFD0	ECR.4	LSB of OOF event count.					
ESFD3	ECR.3	MSB of extended superframe error count.					
ESFD0	ECR.0	LSB of extended superframe error count.					

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF error event after saturation (RIMR.6=1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counters will count "up" to saturation from the preset value and may be read at any time. These counters share the same register address and must be written to or read from simultaneously.

The OOF counter records out-of-frame events in both 193S and 193E. The ESF error counter records errored superframes in 193E. In 193S, the ESF counter records individual F_T and F_S errors when RCR.3=1; F_T errors only when RCR.3=0. ECR counter increments are disabled when resync is in progress (RLOS high).

ALARM OUTPUTS

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the onboard alarm logic.

RLOS OUTPUT

The receive loss of sync output indicates the status of the receiver synchronizer circuitry; when high, an off-line resynchronization is in progress and a high-low transition indicates resync is complete. The RLOS bit (RSR.0) is a "latched" version of the RLOS output. If the auto-resync mode is selected (RCR.1=0), RLOS is a real time indication of a carrier loss or OOF event occurrence.

RYEL OUTPUT

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR.5) is a "latched" version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 (Hex) and FF (Hex) received at RLINK. In 193S, framing the yellow alarm format is dependent on CCR.3; if CCR.3=0, the RYEL output transitions high if bit 2 of 256 or more consecutive channels is 0; if CCR.3=1, yellow alarm is declared when the S-bit received in frame 12 is 1.

RBV OUTPUT

The bipolar violation output transitions high when an accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

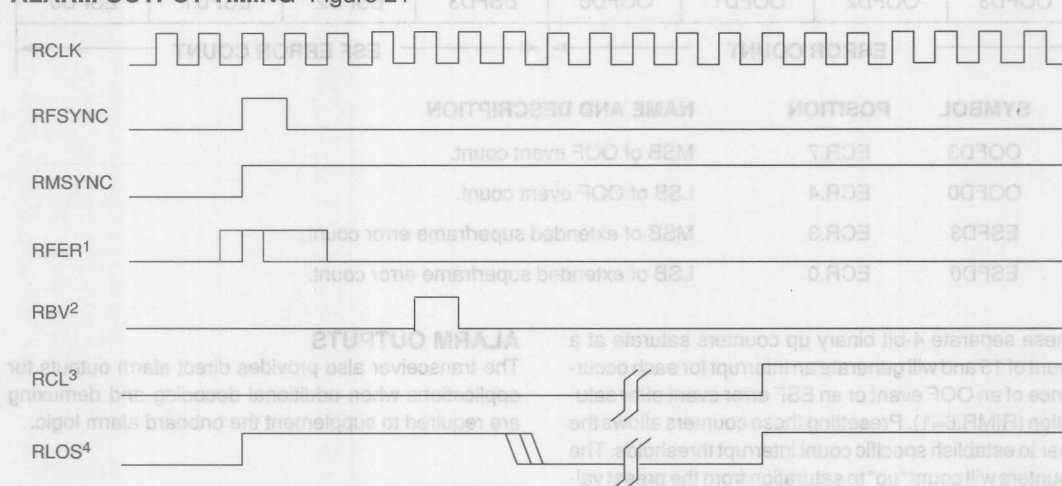
RFER OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S framing, F_T and F_S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low-high-low transition (one bit period wide) one half RCLK period before a low-high transition on RMSYNC.

RESET

A high-low transition on \overline{RST} clears all registers and forces immediate receive resync when \overline{RST} returns high. This reset has no effect on transmit frame multi-frame or channel counters. \overline{RST} must be held low on system power-up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

ALARM OUTPUT TIMING Figure 21



NOTES:

1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if CCR.3=1). Also, in 193E, RFER transitions 1/2 bit time before the rising edge of RMSYNC to indicate a CRC error for the previous multiframe.
2. RBV indicates received bipolar violation and transitions high when an accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high (during 32nd bit time) when 32 consecutive bits received are 0; RCL transitions low when the next 1 is received.
4. RLOS transitions high during the F-bit time that caused an OOF event (any two of four consecutive F_T or FPS bits are in error) if auto-resync mode is selected (RCR.1=0). Resync will also occur when loss of carrier is detected (RCL=1). When RCR.1=1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR.0 transitions low-to-high or the \overline{RST} pin transitions high-low-high.

HARDWARE MODE

For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying SPS to V_{SS} disables the serial port, clears all internal registers except CCR and TCR and redefines pins 14 through 18 as mode control inputs. The hardware mode allows device retrofit into existing applications where mode control and alarm conditioning hardware is often designed with discrete logic.

HARDWARE COMMON CONTROL

In the hardware mode bits TCR.2, CCR.4, TCR.0, CCR.1 and CCR.2 map to pins 14 through 18. The loop-

back feature (bit CCR.0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched as when both pins are taken high, preserving the current zero suppression mode). Robbed bit signaling (bit TCR.4) is enabled for all channels. The user may tie TSE to TABCD externally to disable signaling if so desired. Bit CCR.3 is forced to 0 which selects bit 2 yellow alarm in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR are cleared in the hardware mode. The \overline{RST} input may be used to force immediate receiver resync and has no effect on transmit.

HARDWARE MODE Table 6

PIN NUMBER	REGISTER BIT LOCATION	NAME AND DESCRIPTION
14 (16)	TCR-D2	193S – S-bit insertion³ 1 = external; 0 = internal
15 (17)	CCR-D4	Framing Mode Select. 1 = 193E; 0 = 193S
16 (18)	TCR-D0	Transmit Yellow Alarm^{2,3} 1 = enabled; 0 = disabled
17 (19)	CCR-D1	Zero Suppression¹ 1 = bit 7 stuffing 0 = transparent
18 (20)	CCR-D2	B8ZS¹. 1 = enabled; 0 = disabled

NOTES:

1. Tying pins 17 and 18 high enables loopback in the hardware mode.
2. Bit 2 (193S) and data link (193E) yellow alarms are supported.
3. S-bit yellow alarm (193S) is not internally supported; however, the user may elect to insert external S bits for alarm purposes.
4. Pin numbers for PLCC package are listed in parenthesis.

T1 OVERVIEW

Framing Standards

The DS2180A is compatible with the existing Bell System D4 framing standard described in ATT PUB 43801 and the new extended superframe format (ESF) as described in ATT C.B. #142. In this document, D4 framing is referred to as 193S and ESF (also known as Fe) is referred to as 193E. Programmable features of the DS2180A allow support of other framing standards which are derivatives of 193E and 193S. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position. In 193S, 12 frames make up a superframe, in 193E, 24. A frame consists of 24 channels (timeslots) of 8-bit data preceded by an F-bit. Channel data is transmitted and received MSB first.

F-Bits

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F_T-bits) which provides frame alignment information and the signaling framing pattern (known as F_S-bits) which provides multiframe alignment information. In 193E framing, the F-bit position is shared by the framing pattern sequence

(FPS) which provides frame and multiframe alignment information, a 4 KHz data link known as FDL (Facility Data Link), and CRC (Cyclic Redundancy Check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK) and the CRC bits are an indicator of link quality and may be monitored by the user to establish error performance.

Signaling

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted. In 193E, A and B data is inserted into frames 6 and 12 and C and D data is inserted into frames 18 and 24. This allows a maximum of four signaling states to be transmitted per superframe in 193S and 16 states in 193E.

Alarms

The DS2180A supports all alarm pattern generation and detection required in typical Bell System applications. These alarm modes are explained in ATT PUB 43801, ATT C.B. #142 and elsewhere in this document.

NAME AND DESCRIPTION	REGISTER BIT LOCATION	PIN NUMBER
Zero Suppression 1 = bit 7 stuffing 0 = transparent	CCR-D1	17 (19)
Backdoor 1 = enabled; 0 = disabled	CCR-D2	18 (20)
Transmit Yellow Alarm 1 = enabled; 0 = disabled	CCR-D3	18 (18)
Transmit Yellow Alarm 1 = enabled; 0 = disabled	CCR-D3	18 (18)
Transmit Yellow Alarm 1 = enabled; 0 = disabled	CCR-D3	18 (18)

NOTES:

1. Typing pins 17 and 18 high enables feedback in the hardware mode.
2. Bit 2 (193S) and data link (193E) yellow alarm are supported.
3. 2-bit yellow alarm (193S) is not internally supported; however, the user may elect to insert external 2 bits for alarm purposes.
4. Pin numbers for PLCC package are listed in parentheses.

193E FRAMING FORMAT Table 7

FRAME NUMBER	F-BIT USE			BIT USE IN EACH CHANNEL		SIGNALING-BIT USE		
	FPS ¹	FDL ²	CRC ³	DATA	SIGNALING	2 STATE	4 STATE	16 STATE
1	—	M	—	BITS 1–8	—	—	—	—
2	—	—	C1	BITS 1–8	—	—	—	—
3	—	M	—	BITS 1–8	—	—	—	—
4	0	—	—	BITS 1–8	—	—	—	—
5	—	M	—	BITS 1–8	—	—	—	—
6	—	—	C2	BITS 1–7	BIT 8	A	A	A
7	—	M	—	BITS 1–8	—	—	—	—
8	0	—	—	BITS 1–8	—	—	—	—
9	—	M	—	BITS 1–8	—	—	—	—
10	—	—	C3	BITS 1–8	—	—	—	—
11	—	M	—	BITS 1–8	—	—	—	—
12	1	—	—	BITS 1–7	BIT 8	A	B	B
13	—	M	—	BITS 1–8	—	—	—	—
14	—	—	C4	BITS 1–8	—	—	—	—
15	—	M	—	BITS 1–8	—	—	—	—
16	0	—	—	BITS 1–8	—	—	—	—
17	—	M	—	BITS 1–8	—	—	—	—
18	—	—	C5	BITS 1–7	BIT 8	A	A	C
19	—	M	—	BITS 1–8	—	—	—	—
20	1	—	—	BITS 1–8	—	—	—	—
21	—	M	—	BITS 1–8	—	—	—	—
22	—	—	C6	BITS 1–8	—	—	—	—
23	—	M	—	BITS 1–8	—	—	—	—
24	1	—	—	BITS 1–7	BIT 8	A	B	D

NOTES:

1. FPS – Framing Pattern Sequence.
2. FDL – 4 KHz Facility Data Link; M = message bits.
3. CRC – Cyclic Redundancy Check bits. The CRC code will be internally generated by the device when TCR.5=0. When TCR.5=1, externally supplied CRC data will be sampled at TSER during the F-bit time of frames 2, 6, 10, 14, 18, 22.
4. The user may program any individual channels clear, in which case bit 8 will be used for data, not signaling.
5. Depending on application, the user can support 2-state, 4-state or 16-state signaling by the appropriate decodes of TMO, TSIGFR, TSIGSEL (Transmit Side) and RMSYNC, RSIGFR and RSIGSEL (Receive Side).

193S FRAMING FORMAT Table 8

FRAME NUMBER	F-BIT USE		BIT USE IN EACH CHANNEL		SIGNALLING-BIT USE	
	F _T ¹	F _S ²	DATA	SIGNALING ⁴		
1	1	—	BITS 1–8	—	M	1
2	—	0	BITS 1–8	—	—	2
3	0	—	BITS 1–8	—	M	3
4	—	0	BITS 1–8	—	—	4
5	1	—	BITS 1–8	—	M	5
6	—	1	BITS 1–7	BIT 8	—	A
7	0	—	BITS 1–8	—	M	7
8	—	1	BITS 1–8	—	—	8
9	1	—	BITS 1–8	—	M	9
10	—	1	BITS 1–8	—	—	10
11	0	—	BITS 1–8	—	M	11
12	—	0 ³	BITS 1–7	BIT 8	—	B

NOTES:

- 1. F_T (terminal framing) bits provide frame alignment information.
- 2. F_S (signaling frame) bits provide multiframe alignment information.
- 3. The S-bit in frame 12 may be used for yellow alarm transmission and detection in some applications.
- 4. The user may program any individual channels clear, in which case bit 8 will be used for data, not signaling.

Line Coding

T1 line data is transmitted in a bipolar alternative mark inversion line format; 1's are transmitted as alternating negative and positive pulses and 0's are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a 1's density constraint to keep clock extraction circuitry functioning which is usually met by forcing bit 7 of any channel consisting of all 0's to 1. The use of Bipolar Eight Zero Substitution (B8ZS) satisfies all the 1's density requirement while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in ATT C.B. #144. When the B8ZS fea-

ture is enabled, any outgoing stream of eight consecutive 0's is replaced with a B8ZS code word. If the last 1 transmitted was positive, the inserted code is 000+-0+-; if negative, the code word inserted is 000-+0+- . Bipolar violations occur in the fourth and seventh bit positions which are ignored by the DS2180A error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all 0's if B8ZS is enabled. Also, the receive status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR.2.

TRANSMIT SIDE OVERVIEW

The transmit side of the DS2180A is made up of six major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC. The timing and clock generation circuit develops all onboard and output clocks to the system from inputs TCLK, TFSYNC, and TMSYNC. The yellow alarm circuitry generates mode-dependent yellow alarms. The CRC block generates checksum results utilized in 193E framing. F-bit data provides mode-dependent framing patterns and allows insertion of link or S-bit data externally. All of these blocks feed into the data selector where, under control of the CCR, TCR, TIRs and TTRs, the contents of the outgoing data stream are established by bit selection and insertion. The bipolar coder formats the output of the data selector to make it compatible with bipolar transmission techniques and inserts zero suppression codes. The bipolar coder also supports the onboard loopback feature. Input-to-output delay of the transmitter is 10 TCLK cycles.

RECEIVE SIDE OVERVIEW

Synchronizer

The heart of the receiver is the synchronizer monitor. This circuit serves two purposes: 1) monitoring the incoming data stream for loss of frame or multiframe alignment, and 2) searching for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR which is forced low during resync. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR allow tailoring of the resync algorithm by the user. These bits are described below.

Sync Time (RCR.2)

Bit RCR.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR.2=1, the algorithm will validate 24 bits; if RCR.2=0, 10 bits are validated. 24-bit testing results in superior false framing protection, while 10-bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

Resync (RCR.0)

A zero-to-one transition of RCR.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

Sync Enable (RCR.1)

When RCR.1 is cleared, the receiver will initiate automatic resync if any of the following events occur: 1) an OOF event ("out-of-frame"), or 2) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or F_S bits are in error. When RCR.1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR.0 to 1 or externally via a low-high transition on RST. Note that using RST to initiate resync resets the receive output timing while RST is low; use of RCR.1 does not affect output timing until the new alignment is located.

Sync Criteria (RCR.3)

193E

Bit RCR.3 determines which sync algorithm is utilized when resync is in progress (RLOS=1). In 193E framing, when RCR.3=0, the synchronizer will lock only to the F_S pattern and will move to the new frame and multiframe alignment after the move to the new alignment. When RCR.3=1, the new alignment is further tested by a CRC code match. RLOS will transition low after a CRC match occurs. If no CRC match occurs in three attempts (three multiframes), the algorithm will reset and a new search for the framing pattern begins. It takes 9 ms for the synchronizer to check the first CRC code after the new alignment has been loaded. Each additional CRC test takes 3 ms. Regardless of the state of RCR.3, if more than one candidate exists after about 24 ms, the synchronizer will begin eliminating emulators by testing their CRC codes online in order to find the true framing candidate.

193S

In 193S framing, when RCR.3=1, the synchronizer will cross check the F_T pattern with the F_S pattern to help eliminate false framing candidates such as digital milliwatts. The F_S patterns are compared to the repeating pattern ...00111000111000...(00111X0 if CCR.3=YELMD—is equal to a 1). In this mode, F_T and F_S patterns must be correctly identified by the synchro-

nizer before sync is declared. Clearing RCR.3 causes the synchronizer to search for F_T patterns (101010...) without cross-coupling the F_S pattern. Frame sync will be established using the F_T information, while multiframe sync will be established only if valid F_S information is present. If no valid F_S pattern is identified, the synchronizer will move to the F_T alignment, RLOS will go

low, and a false multiframe position may be indicated by RMSYNC. RFER will indicate when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode will be used in applications where non-standard S-bit patterns exist. In such applications, multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

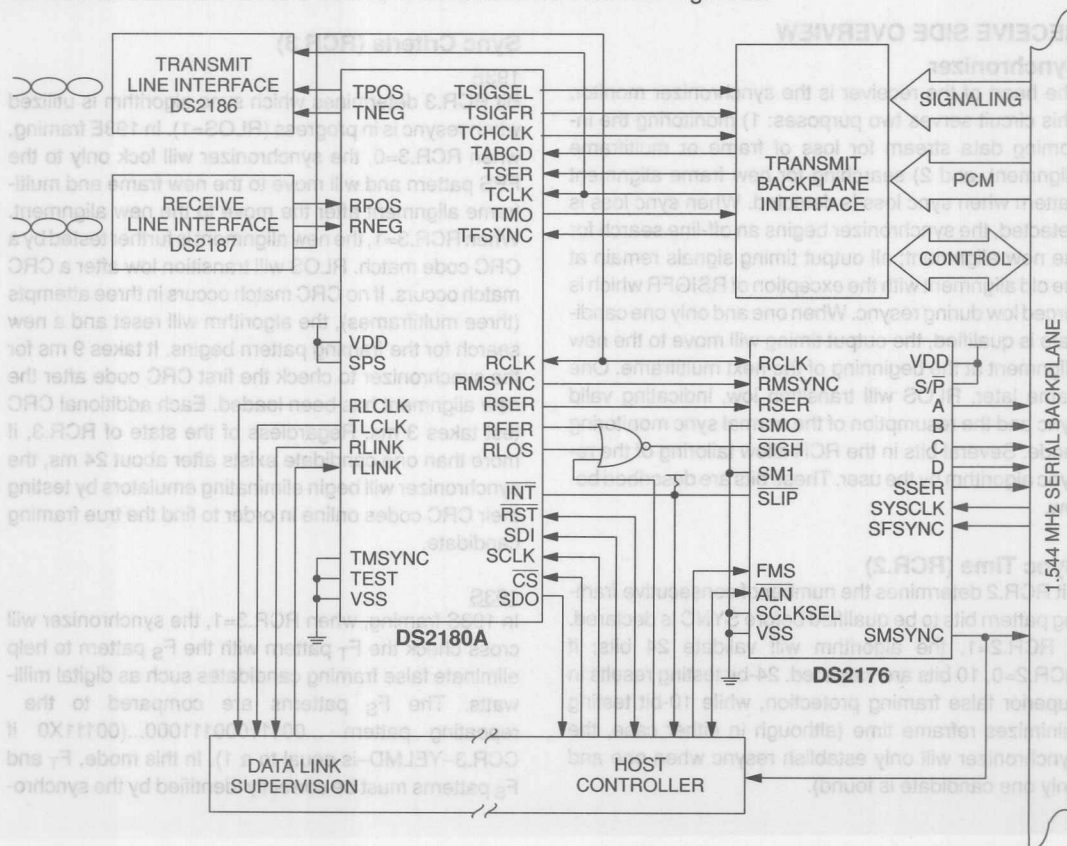
AVERAGE REFRAME TIME¹ Table 9

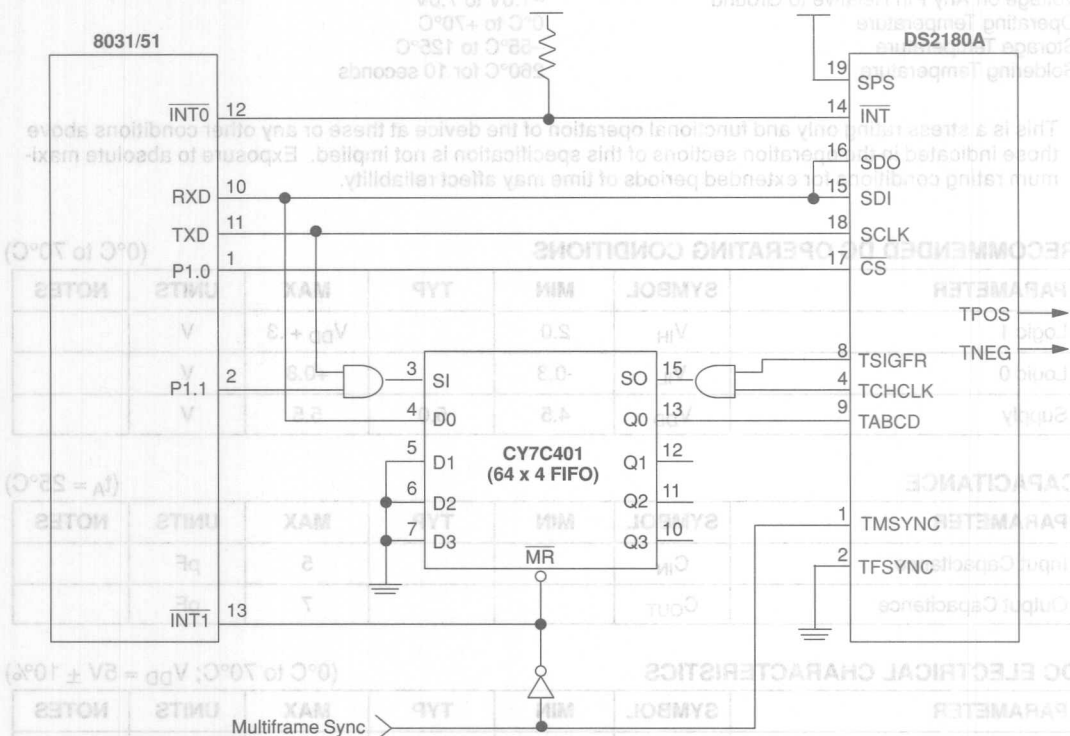
FRAME MODE	RCR.2=0			RCR.2=1			UNITS
	MIN	AVG	MAX	MIN	AVG	MAX	
193S	3.0	3.75	4.5	6.5	7.25	8.0	ms
193E	6.0	7.5	9.0	13.0	14.5	16.0	

NOTE:

1. Average Reframe Time is defined here as the average time it takes from the start of sync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

BACKPLANE INTERFACE USING DS2180A AND DS2176 Figure 22





Many robbed-bit signaling applications utilize a micro-processor to insert transmit signaling data into the outgoing data stream. The circuit shown in Figure 23 “decouples” the processor timing from that of the DS2180A by use of a small FIFO memory. The processor writes to the FIFO (six bytes are written: three for A data, three for

B data) only when signaling updates are required. The system is interrupt-driven from the transmit multiframe sync input; the processor must update the FIFO prior to Frame 6 (625 μ s after interrupt) to prevent data corruption. The application circuit shown supports 193S framing. Additional hardware is required for 193E applications.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

-1.0V to 7.0V

Operating Temperature

0°C to +70°C

Storage Temperature

-55°C to 125°C

Soldering Temperature

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + .3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5	5.0	5.5	V	

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		3	10	mA	1,2
Input Leakage	I_{IL}			1	μA	
Output Leakage	I_{LO}			1	μA	3
Output Current @ 2.4V	I_{OH}	-1			mA	4
Output Current @ .4V	I_{OL}	+4			mA	5

NOTES:

1. TCLK = RCLK = 1.544 MHz.
2. Outputs open.
3. Applies to SDO when tri-stated.
4. All outputs except \overline{INT} , which is open collector.
5. All outputs.

AC ELECTRICAL CHARACTERISTICS

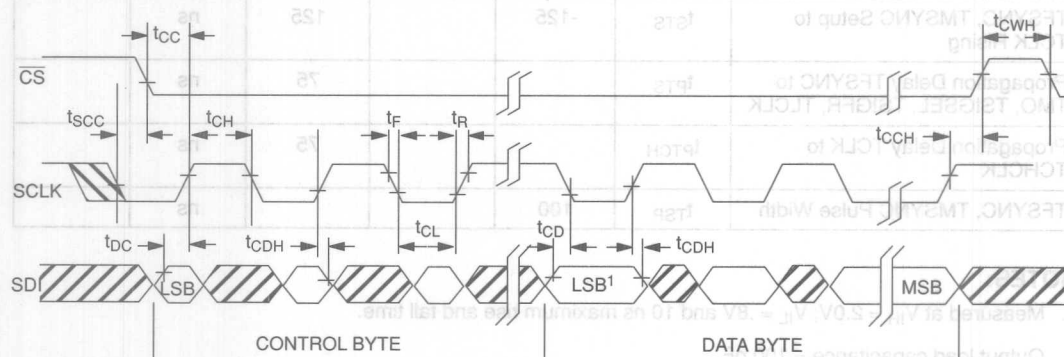
(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t_{DC}	50			ns	
SCLK to SDI Hold	t_{CDH}	50			ns	
SDI to SCLK Falling Edge	t_{CD}	50			ns	
SCLK Low Time	t_{CL}	250			ns	
SCLK High Time	t_{CH}	250			ns	
SCLK Rise & Fall Time	t_R, t_F			500	ns	
\overline{CS} to SCLK Setup	t_{CC}	50			ns	
SCLK to \overline{CS} Hold	t_{CCH}	50			ns	
\overline{CS} Inactive Time	t_{CWH}	250			ns	
SCLK to SDO Valid ²	t_{CDV}			200	ns	
\overline{CS} to SDO High Z	t_{CDZ}			75	ns	
SCLK Setup to \overline{CS} Falling	t_{SCC}	50			ns	

NOTES:

1. Measured at $V_{IH}=2.0V$; $V_{IL}=.8V$ and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

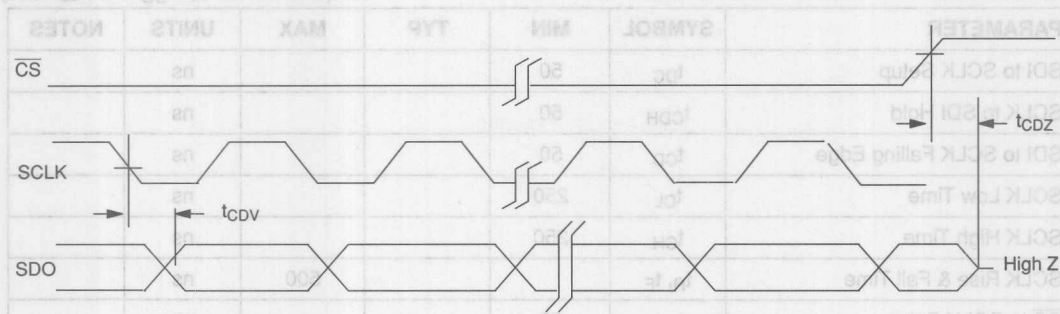
SERIAL PORT WRITE AC TIMING DIAGRAM



NOTES:

1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.
2. Shaded regions indicate "don't care" states of input data.

SERIAL PORT READ AC TIMING

**NOTE:**

1. Serial port write must precede a port read to provide address information.

AC ELECTRICAL CHARACTERISTICS¹ – TRANSMIT(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P	250	648		ns	
TCLK Pulse Width	t_{WL}, t_{WH}	125	324		ns	
TCLK, RCLK Rise & Fall Times	t_F, t_R		20		ns	
TSER, TABCD, TLINK Setup to TCLK Falling	t_{STD}	50			ns	
TSER, TABCD, TLINK Hold from TCLK Falling	t_{HTD}	50			ns	
TFSYNC, TMSYNC Setup to TCLK Rising	t_{STS}	-125		125	ns	
Propagation Delay TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}			75	ns	
Propagation Delay TCLK to TCHCLK	t_{PTCH}			75	ns	
TFSYNC, TMSYNC Pulse Width	t_{TSP}	100			ns	

NOTES:

1. Measured at $V_{IH} = 2.0V$; $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

AC ELECTRICAL CHARACTERISTICS¹ – RECEIVE(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

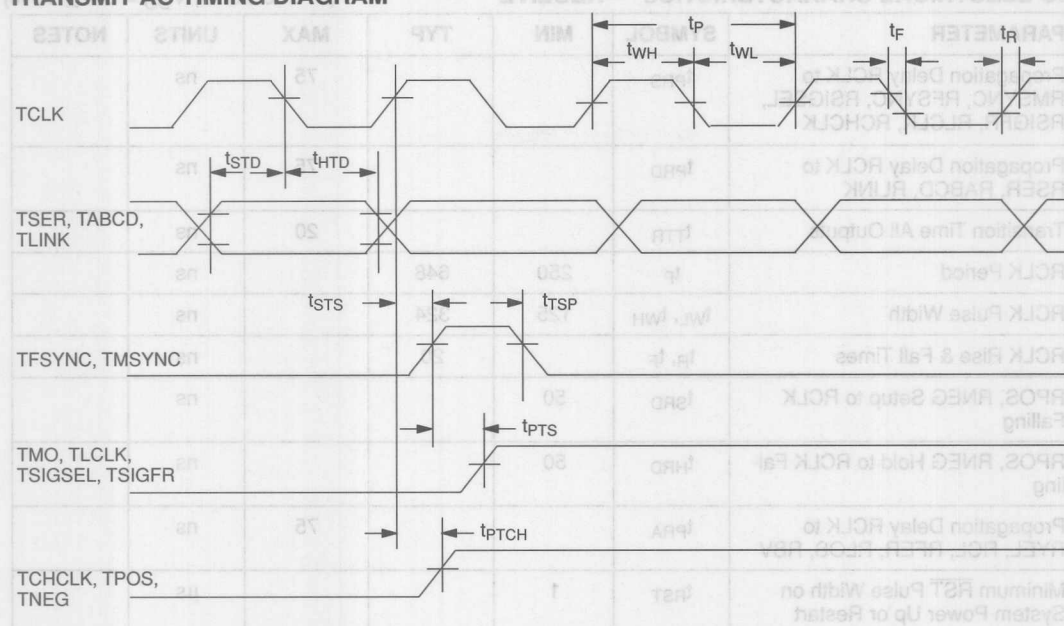
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay RCLK to RMSYNC, RFSYNC, RSIGSEL, RSIGFR, RLCLK, RCHCLK	t_{PRS}			75	ns	
Propagation Delay RCLK to RSER, RABCD, RLINK	t_{PRD}			75	ns	
Transition Time All Outputs	t_{TTR}			20	ns	
RCLK Period	t_P	250	648		ns	
RCLK Pulse Width	t_{WL}, t_{WH}	125	324		ns	
RCLK Rise & Fall Times	t_R, t_F		20		ns	
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50			ns	
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns	
Propagation Delay RCLK to RYEL, RCL, RFER, RLOS, RBV	t_{PRA}			75	ns	
Minimum \overline{RST} Pulse Width on System Power Up or Restart	t_{RST}	1			μs	

NOTES:

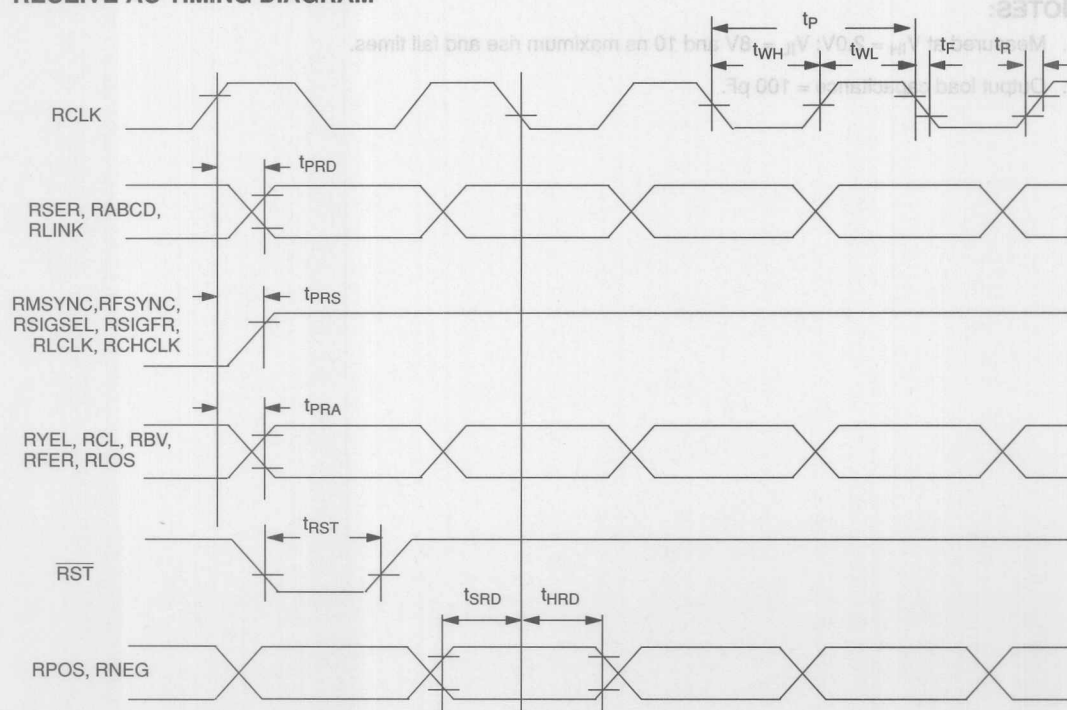
- Measured at $V_{IH} = 2.0V$; $V_{IL} = .8V$ and 10 ns maximum rise and fall times.
- Output load capacitance = 100 pF.



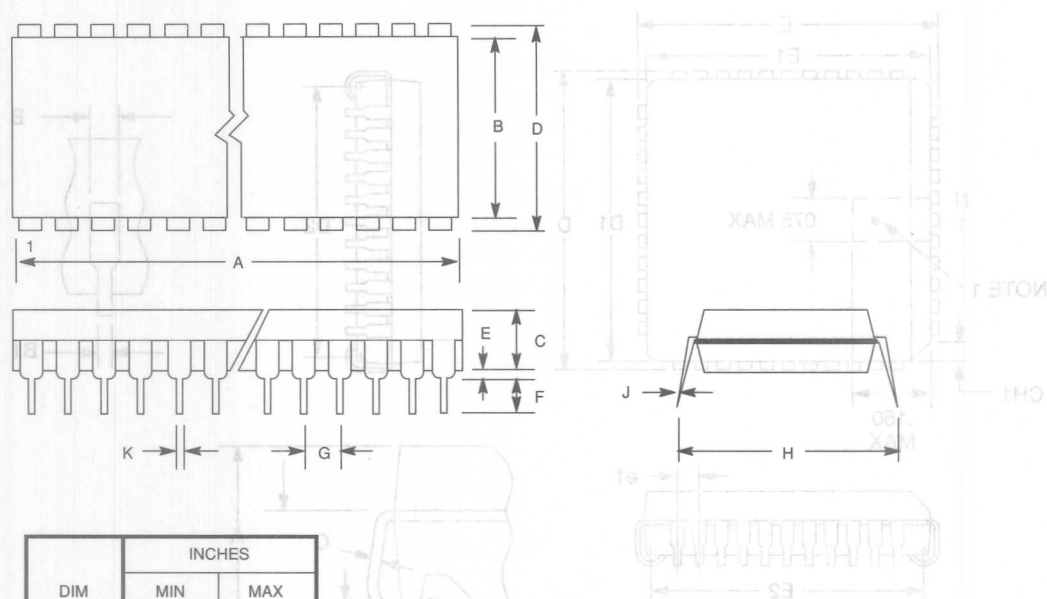
TRANSMIT AC TIMING DIAGRAM



RECEIVE AC TIMING DIAGRAM



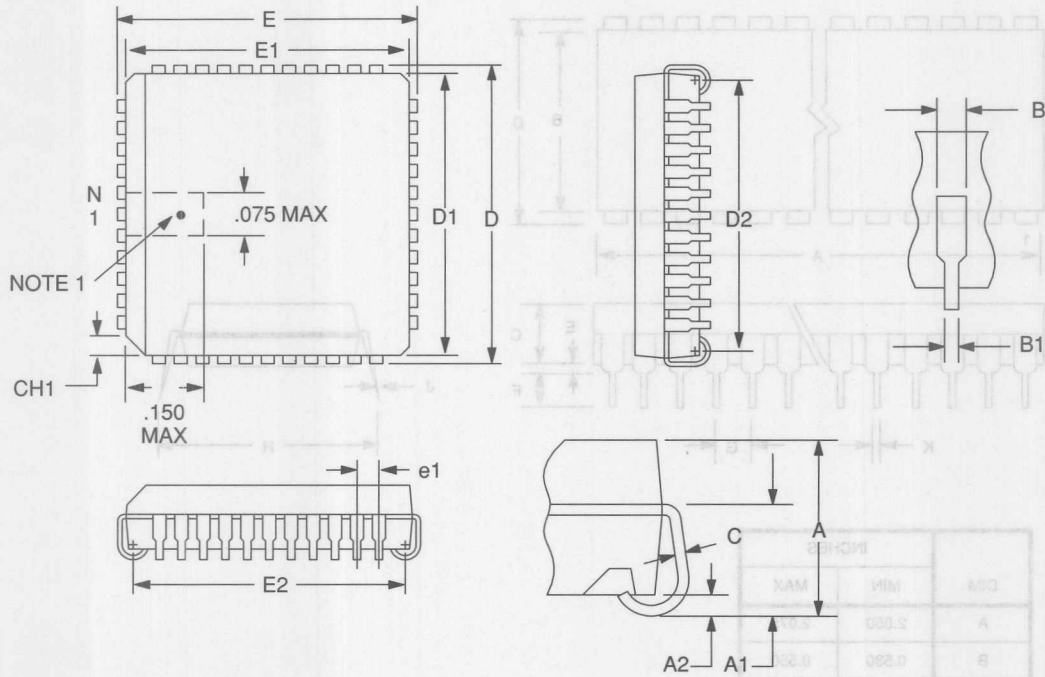
DS2180A SERIAL T1 TRANSCEIVER (600 MIL DIP)



DIM	INCHES	
	MIN	MAX
A	2.050	2.075
B	0.530	0.550
C	0.140	0.160
D	0.600	0.625
E	0.015	0.040
F	0.120	0.145
G	0.090	0.110
H	0.625	0.675
J	0.008	0.012
K	0.015	0.022

DIM	INCHES	
	MIN	MAX
A	0.135	0.150
B	0.050	0.070
C	0.005	0.010
D	0.005	0.010
E	0.005	0.010
F	0.005	0.010
G	0.005	0.010
H	0.005	0.010
I	0.005	0.010
J	0.005	0.010
K	0.005	0.010
L	0.005	0.010
M	0.005	0.010
N	0.005	0.010
O	0.005	0.010
P	0.005	0.010
Q	0.005	0.010
R	0.005	0.010
S	0.005	0.010
T	0.005	0.010
U	0.005	0.010
V	0.005	0.010
W	0.005	0.010
X	0.005	0.010
Y	0.005	0.010
Z	0.005	0.010

DS2180AQ SERIAL T1 TRANSCEIVER (PLCC)



DALLAS

SEMICONDUCTOR

DS2181A

CEPT Primary Rate Transceiver

FEATURES

- Single-chip primary rate transceiver meets CCITT standards G.704, G.706 and G.732
- Supports new CRC4-based framing standards and CAS and CCS signalling standards
- Simple serial interface used for device configuration and control in processor mode
- Hardware mode requires no host processor; intended for stand-alone applications
- Comprehensive, on-chip alarm generation, alarm detection, and error logging logic
- Shares footprint with DS2180A T1 Transceiver
- Companion to DS2175 T1/CEPT Elastic Store, DS2186 Transmit Line Interface, DS2187 Receive Line Interface, and DS2188 Jitter Attenuator
- 5V supply; low-power CMOS technology

DESCRIPTION

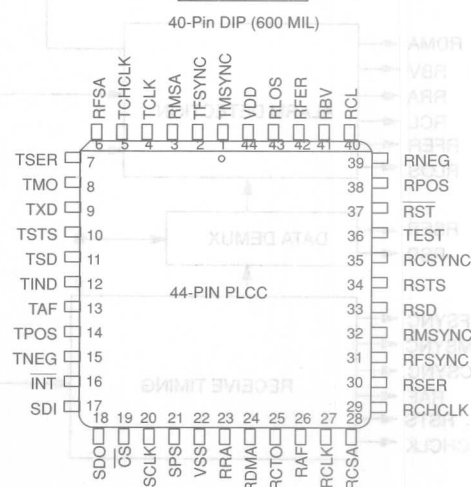
The DS2181A is designed for use in CEPT networks and supports all logical requirements of CCITT Red Book Recommendations G.704, G.706 and G.732. The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signalling data, and produces network alarm codes when enabled. The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignments. Once synchronized, the device extracts channel, signalling, and alarm data.

A serial port allows access to 14 on-chip control and status registers in the processor mode. In this mode, a host processor controls features such as error logging, per-channel code manipulation, and alteration of the receive synchronizer algorithm.

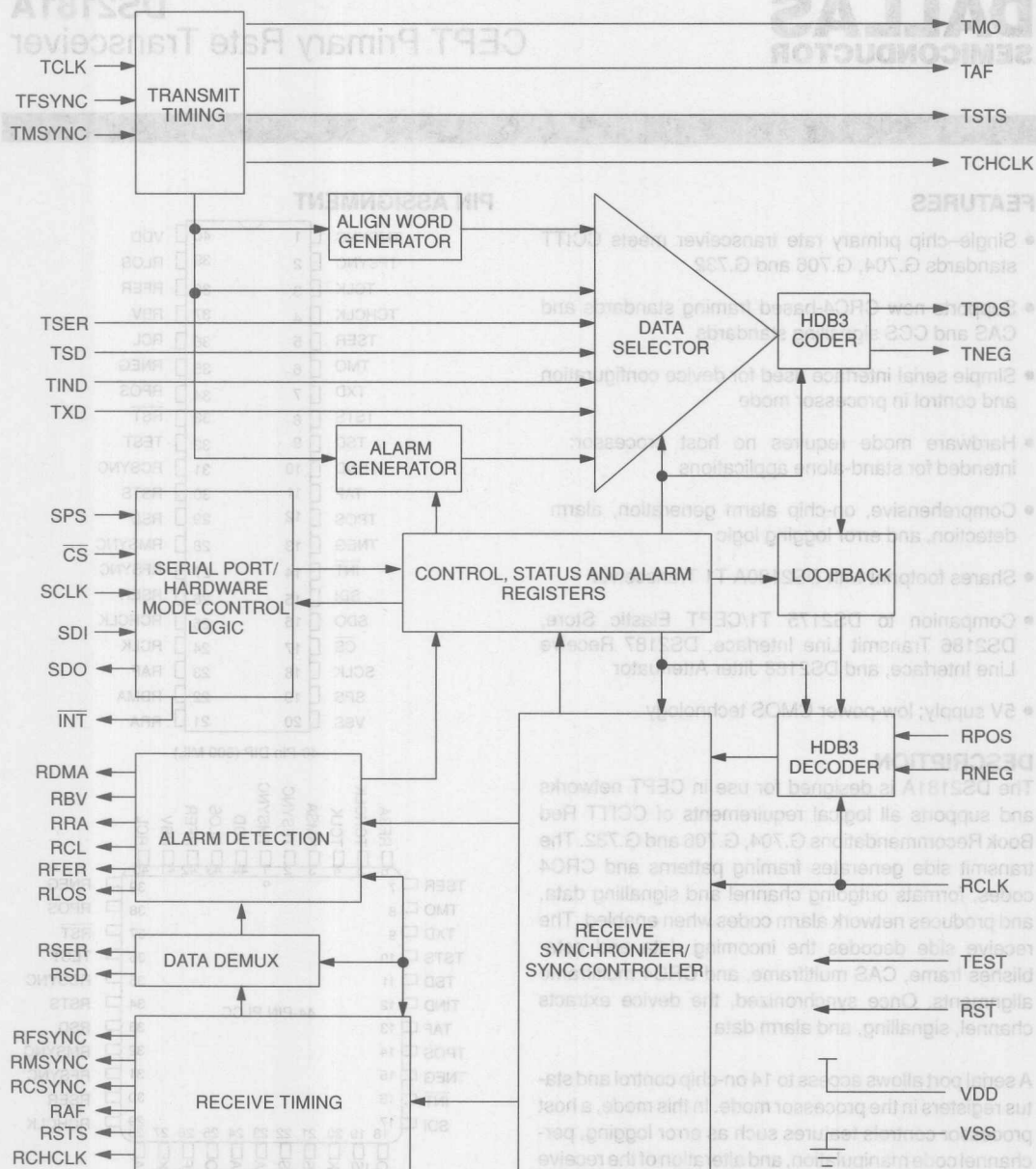
The hardware mode is intended for preliminary system prototyping and/or retrofitting into existing systems. This mode requires no host processor and disables special features available in the processor mode.

PIN ASSIGNMENT

TMSYNC	1	40	VDD
TFSYNC	2	39	RLOS
TCLK	3	38	RFER
TCHCLK	4	37	RBV
TSER	5	36	RCL
TMO	6	35	RNEG
TXD	7	34	RPOS
TSTS	8	33	RST
TSD	9	32	TEST
TIND	10	31	RCSYNC
TAF	11	30	RSTS
TPOS	12	29	RSD
TNEG	13	28	RMSYNC
INT	14	27	RFSYNC
SDI	15	26	RSER
SDO	16	25	RCHCLK
CS	17	24	RCLK
SCLK	18	23	RAF
SPS	19	22	RDMA
VSS	20	21	RRA



DS2181A BLOCK DIAGRAM Figure 1



TRANSMIT PIN DESCRIPTION (40-PIN DIP ONLY) Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TMSYNC	I	Transmit Multiframe Sync. Low-high transition establishes start of CAS and/or CRC4 multiframe. Can be tied low, allowing internal multiframe counter to run free.
2	TFSYNC	I	Transmit Frame Sync. Low-high transition every frame period establishes frame boundaries. Can be tied low, allowing TMSYNC to establish frame boundaries.
3	TCLK	I	Transmit Clock. 2.048 MHz primary clock.
4	TCHCLK	O	Transmit Channel Clock. 256 KHz clock which identifies timeslot boundaries. Useful for parallel-to-serial conversion of channel data.
5	TSER	I	Transmit Serial Data. NRZ data input, sampled on falling edges of TCLK.
6	TMO	O	Transmit Multiframe Out. Output of multiframe counter; high during frame 0, low otherwise.
7	TXD	I	Transmit Extra Data. Sampled on falling edge of TCLK during bit times 5, 7, and 8 of timeslot 16 in frame 0 when CAS signalling is enabled.
8	TSTS	O	Transmit Signalling Timeslot. High during timeslot 16 of every frame, low otherwise.
9	TSD	I	Transmit Signalling Data. CAS signalling data input; sampled on falling edges of TCLK for insertion into outgoing timeslot 16 when enabled.
10	TIND	I	Transmit International and National Data. Sampled on falling edge of TCLK during bit 1 time of timeslot 0 every frame (international) and/or during bit times 4 through 8 of timeslot 0 during non-align frames (national) when enabled.
11	TAF	O	Transmit Alignment Frame. High during frames containing the frame alignment signal, low otherwise.
12	TPOS	O	Transmit Bipolar Data Outputs. Updated on rising edge of TCLK.
13	TNEG	O	

SYNCHRONIZER STATUS PIN (44-PIN PLCC ONLY) Table 2A

PIN	SYMBOL	TYPE	DESCRIPTION
3	RMSA	O	Receive Multiframe Search Active. This pin will transition high when the synchronizer searching for the CAS multiframe alignment word is active.
6	RFSA	O	Receive Frame Search Active. This pin will transition high when the synchronizer searching for the FAS is active.
25	RCTO	O	Receive CRC4 Time Out. This pin will transition high when the RCTO counter reaches its maximum count of 32. The pin will return low when either the DS2181AQ reaches CRC4 multiframe synchronization, or if CRC4 is disabled via CRC.2, or if the device is issued a hardware reset via the RST pin.
28	RCSA	O	Receive CRC4 Search Active. This pin will transition high when the synchronizer searching for the CRC4 multiframe alignment word is active.

NOTES:

- These output status pins are only available on the DS2181AQ.
- If the TEST pin is tied low and CCR.1=0, then these pins will be tri-stated.

RECEIVE PIN DESCRIPTION (40-PIN DIP ONLY) Table 2B

PIN	SYMBOL	TYPE	DESCRIPTION
21	RRA	O	Receive Remote Alarm. Transitions high when alarm detected; returns low when alarm cleared.
22	RDMA	O	Receive Distant Multiframe Alarm. Transitions high when alarm detected; returns low when alarm cleared.
23	RAF	O	Receive Alignment Frame. High during frames containing the frame alignment signal, low otherwise.
24	RCLK	I	Receive Clock. 2.048 MHz primary clock.
25	RCHCLK	O	Receive Channel Clock. 256 KHz clock, identifies timeslot boundaries; useful for serial-to-parallel conversion of channel data.
26	RSER	O	Receive Serial Data. Received NRZ data, updated on rising edges of RCLK.
27	RFSYNC	O	Receive Frame Sync. Trailing edge indicates start of frame.
28	RMSYNC	O	Receive Multiframe Sync. Low-high transition indicates start of CAS multiframe; held high during frame 0.
29	RSD	O	Receive Signalling Data. Extracted timeslot 16 data; updated on rising edge of RCLK.
30	RSTS	O	Receive Signalling Timeslot. High during timeslot 16 of every frame, low otherwise.
31	RCSYNC	O	Receive CRC4 Sync. Low-high transition indicates start of CRC4 multiframe; held high during CRC4 frames 0 thru 7 and held low during frames 8 through 15.
33	RST	I	Reset. Must be asserted during device power-up and when changing to/from the hardware mode.
34	RPOS	I	Receive Bipolar Data. Sampled on falling edges of RCLK. Tie together to receive NRZ data and disable BPV monitor circuitry.
35	RNEG	I	
36	RCL	O	Receive Carrier Loss. Low-high transition indicates loss of carrier.
37	RBV	O	Receive Bipolar Violation. Pulses high during detected bipolar violations.
38	RFER	O	Receive Frame Error. Pulses high when frame alignment, CAS multiframe alignment or CRC4 words received in error.
39	RLOS	O	Receive Loss of Sync. Indicates synchronizer status; high when frame, CAS and/or CRC4 multiframe search underway, low otherwise.

PORT PIN DESCRIPTION (40-PIN DIP ONLY) Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
14	INT	O	Receive Alarm Interrupt. Flags host controller during alarm conditions. Active low; open drain output.
15	SDI	I	Serial Data In. Data for on-chip control registers; sampled on rising edge of SCLK.
16	SDO	O	Serial Data Out. Control and status data from on-chip registers. Updated on falling edge of SCLK; tri-stated during port write or when CS is high.
17	$\overline{\text{CS}}$	I	Chip Select. Must be low to write or read the serial port.
18	SCLK	I	Serial Data Clock. Used to write or read the serial port registers.
19	SPS	I	Serial Port Select. Tie to V_{DD} to select the serial port. Tie to V_{SS} to select the hardware mode.

POWER AND TEST PIN DESCRIPTION (40-PIN DIP ONLY) Table 4

PIN	SYMBOL	TYPE	DESCRIPTION
20	V _{SS}	—	Signal Ground. 0.0 volts.
32	TEST	I	Test Mode. Tie to V _{SS} to select the old DS2181 sync algorithm and to tri-state the synchronizer status pins on the DS2181AQ. Tie to V _{DD} to select the new DS2181A sync algorithm and activate the synchronizer status pins on the DS2181AQ.
40	V _{DD}	—	Positive Supply. 5.0 volts.

REGISTER SUMMARY Table 5

REGISTER	ADDRESS	T/R ¹	DESCRIPTION/FUNCTION
RIMR	0000	R	Receive Interrupt Mask Register. Allows masking of alarm generated interrupts.
RSR	0001	R ²	Receive Status Register. Reports all receive alarm conditions.
BVCR	0010	R	Bipolar Violation Count Register. 8-bit presetable counter which records individual bipolar violations.
CECR	0011	R	CRC4 Error Count Register. 8-bit presetable counter which records individual errors.
FECD	0100	R	Frame Error Count Register. 8-bit presetable counter which logs individual errors in the received frame alignment signal.
RCR	0101	R	Receive Control Register. Establishes receive side operating characteristics.
CCR	0110	T/R	Common Control Register. Establishes additional operating characteristics for transmit and receive sides.
TCR	0111	T	Transmit Control Register. Establishes transmit side operation characteristics.
TIR1 TIR2 TIR3 TIR4	1000 1001 1010 1011	T	Transmit Idle Registers. Designates which outgoing timeslots are to be substituted with idle code.
TINR	1100	T	Transmit International and National Register. When enabled via the TCR, contents inserted into the outgoing national and/or international bit positions.
TXR	1101	T	Transmit Extra Register. When enabled via the TCR, contents inserted into the outgoing extra bit positions.

NOTES:

1. Transmit or receive side register.
2. RSR is a read-only register; all other registers are read/write.
3. Reserved bit locations must be programmed to 0.

SERIAL PORT INTERFACE

Pins 14 through 18 of the DS2181A serve as a microprocessor/microcontroller-compatible serial port. Fourteen on-chip registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces.

Port read/write timing is unrelated to the chip transmit and receive timing, allowing asynchronous reads and/or writes by the host. The timing set is identical to that of 8051-type microcontrollers operating in serial port mode 0. For proper operation of the port and the transmit and receive registers, the user should provide TCLK and RCLK as well as SCLK.

ADDRESS/COMMAND

An address/command byte write must precede any read or write of the port registers. The first bit written (LSB) of the address/command byte specifies read or write. The following nibble identifies register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables the burst mode when set; the burst mode allows consecutive reading or writing of all register data. Data is written to and read from the port LSB first.

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the \overline{CS} input low. Data is sampled on the rising edge of SCLK. Data is

output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated and SDO tri-stated when \overline{CS} returns to high.

CLOCKS

To access the serial port registers both TCLK and RCLK are required along with the SCLK. The TCLK and RCLK are used to internally access the transmit and receive registers, respectively. The CCR is considered a receive register for this purpose.

DATA I/O

Following the eight SCLK cycles that input the address/command byte, data at SDI is strobed into the addressed register on the next eight SCLK cycles (register write) or data is presented at SDO on the next eight SCLK cycles (register read). SDO is tri-stated during writes and may be tied to SDI in applications where the host processor has bidirectional I/O capability.

BURST MODE

The burst mode allows all on-chip registers to be consecutively read or written by the host processor. This feature minimizes device initialization time on system power-up or reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. *All registers must be read or written during the burst mode. If \overline{CS} transitions high before the burst is complete, data validity is not guaranteed.*

Transmit Idle Register. Designates which outgoing time slots are to be substituted with idle code.	T	1000 1001 1010 1011	TIR1 TIR2 TIR3 TIR4
Transmit International and National Register. When enabled via the TCR, contents are inserted into the outgoing national and international bit positions.	T	1100	TINR
Transmit Extra Register. When enabled via the TCR, contents are inserted into the outgoing extra bit positions.	T	1101	TXR

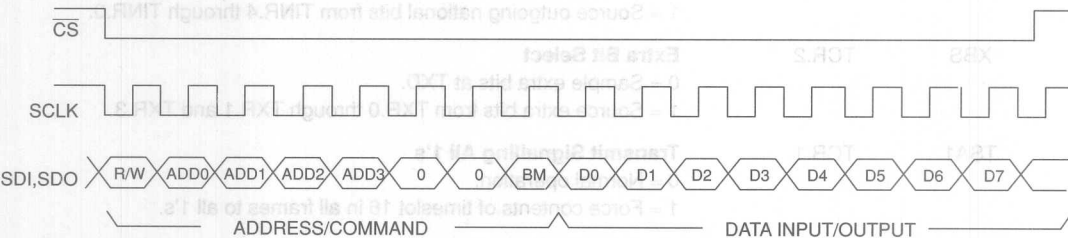
NOTES:

1. Transmit or receive side register.
2. RSR is a read-only register; all other registers are read/write.
3. Reserved bit positions must be programmed to 0.

ACB: ADDRESS COMMAND BYTE Figure 2

(MSB)			(LSB)			
BM	ADD3	ADD2	ADD1	ADD0	R/W	
SYMBOL	POSITION	NAME AND DESCRIPTION				
BM	ACB.7	Burst Mode. If set (and ACB.1 through ACB.4 = 0), burst read or write is enabled.				
—	ACB.6	Reserved; must be 0 for proper operation.				
—	ACB.5	Reserved; must be 0 for proper operation.				
ADD3	ACB.4	MSB of register address.				
ADD2	ACB.3					
ADD1	ACB.2					
ADD0	ACB.1	LSB of register address.				
R/W	ACB.0	Read/Write Select. 0 = Write address register. 1 = Read address register.				

SERIAL PORT READ/WRITE Figure 3



NOTES:

1. SDI sampled on rising edge of SCLK.
2. SDO updated on falling edge of SCLK.

TCR: TRANSMIT CONTROL REGISTER Figure 4

(MSB)			(LSB)				
TUA1	TSS	TSM	INBS	NBS	XBS	TSA1	ODM
SYMBOL	POSITION	NAME AND DESCRIPTION		POSITION	SYMBOL		
TUA1	TCR.7	Transmit Unframed All 1's. 0 = Normal operation. 1 = Replace outgoing data at TPOS and TNEG with unframed all 1's code.		TCR.7	BM		
TSS	TCR.6	Transmit Signalling Select¹ 0 = Signalling data embedded in the serial bit stream is sampled at TSEF during timeslot 16. 1 = Signalling data is channel associated and sampled at TSD as shown in Table 6.		TCR.6	ADCB		
TSM	TCR.5	Transmit Signalling Mode¹ 0 = Channel Associated Signalling (CAS). 1 = Common Channel Signalling (CCS).		TCR.5	ADCB		
INBS	TCR.4	International Bit Select 0 = Sample international bit at TIND. 1 = Outgoing international bit = TINR.7.		TCR.4	ADCB		
NBS	TCR.3	National Bit Select 0 = Sample national bits at TIND. 1 = Source outgoing national bits from TINR.4 through TINR.0.		TCR.3	ADCB		
XBS	TCR.2	Extra Bit Select 0 = Sample extra bits at TXD. 1 = Source extra bits from TXR.0 through TXR.1 and TXR.3.		TCR.2	ADCB		
TSA1	TCR.1	Transmit Signalling All 1's 0 = Normal operation. 1 = Force contents of timeslot 16 in all frames to all 1's.		TCR.1	ADCB		
ODM	TCR.0	Output Data Mode 0 = TPOS and TNEG outputs are 100% duty cycle. 1 = TPOS and TNEG outputs are 50% duty cycle.		TCR.0	ADCB		

NOTE:

1. When the common channel signalling mode is enabled (TCR.5 = 1), the TSD input is disabled internally; all timeslot 16 data is sampled at TSER.

CCR: COMMON CONTROL REGISTER Figure 5

(MSB)				(LSB)			
RESERVED	TAFP	THDE	RHDE	TCE	RCE	SAS	LLB

SYMBOL	POSITION	NAME AND DESCRIPTION
—	CCR.7	Reserved; must be 0 for proper operation.
TAFP	CCR.6	Transmit Align Frame Position¹ When clear, the CAS multiframe begins with a frame containing the frame alignment signal. When set, the CAS multiframe begins with a frame not containing the frame alignment signal.
THDE	CCR.5	Transmit HDB3 Enable 0 = Outgoing data at TPOS and TNEG is AMI coded. 1 = Outgoing data at TPOS and TNEG is HDB3 coded.
RHDE	CCR.4	Receive HDB3 Enable 0 = Incoming data at RPOS and RNEG is AMI coded. 1 = Incoming data at RPOS and RNEG is HDB3 coded.
TCE	CCR.3	Transmit CRC4 Enable When set, outgoing international bit positions in frames 0 through 12 and 14 are replaced by CRC4 multiframe alignment and checksum words.
RCE	CCR.2	Receive CRC4 Enable 0 = Disable CRC4 multiframe synchronizer. 1 = Enable CRC4 synchronizer; search for CRC4 multiframe alignment once frame alignment complete.
SAS	CCR.1	Sync Algorithm Select 0 = Use 'old DS2181' sync algorithm 1 = Use new DS2181A sync algorithm
LLB	CCR.0	Local Loopback 0 = Normal operation. 1 = Internally loop TPOS, TNEG, and TCLK to RPOS, RNEG, and RCLK.

NOTES:

1. This bit must be cleared when CRC4 multiframe mode is enabled (CCR.3 = 1); its state does not affect CCS framing (CCR.5 = 1).
2. CCR is considered a receive register and operates from RCLK and SCLK.

RCR: RECEIVE CONTROL REGISTER Figure 6

(MSB)				(LSB)			
		RSM	CMSC	CMRC	FRC	SYNCE	RESYNC
SYMBOL	POSITION	NAME AND DESCRIPTION					
—	RCR.7	Reserved; must be 0 for proper operation.					
—	RCR.6	Reserved; must be 0 for proper operation.					
RSM	RCR.5	Received Signalling Mode 0 = Channel Associated Signalling (CAS). 1 = Common Channel Signalling (CCS).					
CMSC	RCR.4	CAS Multiframe Sync Criteria 0 = Declare sync when fixed sync criteria met. 1 = Declare sync when fixed criteria are met and two additional consecutive valid multiframe alignment signals are detected.					
CMRC	RCR.3	CAS Multiframe Resync Criteria 0 = Utilize only fixed resync criteria. 1 = Resync if fixed criteria met and/or if two consecutive timeslot 16 words have values of 0 in the first four MSB positions (0000xxxx).					
FRC	RCR.2	Frame Resync Criteria 0 = Utilize only fixed resync criteria. 1 = Resync if fixed criteria met and/or if bit 2 in timeslot 0 of non-align frames is received in error on three consecutive occasions.					
SYNCE	RCR.1	Sync Enable If clear, the synchronizer will automatically begin resync if error criteria are met. If high, no auto resync occurs.					
RESYNC	RCR.0	Resync When toggled low to high, the receive synchronizer will initiate immediately. The bit must be cleared, then set again for subsequent resyncs.					

CEPT FRAME STRUCTURE

The CEPT frame is made up of 32 8-bit channels (time-slots) numbered from 0 to 31. The frame alignment signal in bit positions 2 through 8 of timeslot 0 of every other frame is independent of the various multiframe modes described below. Outputs TAF and RAF indicate frames which contain the alignment signal. Timeslot 0 of frames not containing the frame alignment signal is used for alarm and national data. See the separate DS2181A CEPT Transceiver Application Note for more details.

CAS SIGNALLING

CEPT networks support Channel Associated Signalling (CAS) or Common Channel Signalling (CCS). These

signalling modes are independently selectable for transmit and receive sides.

CAS (selected when TCR.5 = 0 and/or when RCR.5 = 0) is a bit-oriented signalling technique which utilizes a 16-frame multiframe. The multiframe alignment signal (0-hex), extra and alarm bits occupy timeslot 16 of frame 0. Timeslot 16 of the remaining 15 frames is reserved for channel signalling data. Four signalling bits (A, B, C and D) are transmitted once per multiframe as shown in Figure 7. Input TMSYNC establishes the transmitted CAS multiframe position. Signalling data can be sourced from input TSD (TCR.6 = 1) or multiplexed into TSER (TCR.6 = 0).

CCS SIGNALLING

CCS (selected when $TCR.5 = 1$ and/or when $RCR.1 = 1$) utilizes all bit positions of timeslot 16 in every frame for message-oriented signalling data transmission. In CCS mode one can use either timeslot 16 or any one of the other 30 data channels for message-oriented signalling. The CCS mode has no multiframe structure and the insertion of CAS multiframe alignment, distant multiframe alarm and/or extra bits into timeslot 16 is disabled. TSER is the source of timeslot 16 data.

CRC4 CODING

The need for enhanced error monitoring capability and additional protection against emulators of the frame alignment word has led to the development of a cyclic redundancy check (CRC) procedure. When enabled via $CCR.2$ and/or $CCR.3$, CRC4 coding replaces the international bit positions in frames 0 through 12 and 14 with a CRC4 multiframe alignment pattern and associated checksum words. The CRC4 multiframe must begin with a frame containing the frame alignment signal ($CCR.6 = 0$). A rising edge at TMSYNC establishes the CRC4 multiframe alignment (TMSYNC will also establish outgoing CAS multiframe alignment if enabled via $TCR.5$).

Incoming CRC4 multiframe alignment is indicated by RCSYNC. Detected CRC4 checksum errors are reported at output RFER and logged in the CECR.

RECEIVE SYNCHRONIZER

The fixed characteristics of the receive synchronizer may be modified by use of programmable characteristics resident in the RCR and CCR. Sync criteria must be met before synchronization is declared. Resync criteria establish error occurrences which will cause an auto-resync event when enabled ($RCR.1 = 0$).

The receive synchronizer searches for the frame alignment pattern first. Once identified, the output timing set associated with the framing pattern (all outputs except RCSYNC and RMSYNC) is updated to that new alignment. If enabled, the synchronizer then begins CAS and/or CRC4 multiframe search; outputs RMSYNC and/or RCSYNC are then updated. Output RLOS is held high during the entire resync process, then transitions low after the last output timing update indicating resync is complete. For more details about the receive synchronizer, see the separate DS2181A CEPT Transceiver Application Note.

FIXED FRAME SYNC CRITERIA

Valid frame sync is assumed when the correct frame alignment signal is present in frame N and frame $N + 2$ and not present in frame $N + 1$ (bit 2 of timeslot 0 of Frame $N + 1$ is also checked for 1). CAS and/or CRC4 multiframe alignment search is initiated when the frame search is complete if enabled via $RCR.5$ and/or $CCR.2$.

FIXED CAS MULTIFRAME SYNC CRITERIA

CAS multiframe sync is declared when the multiframe alignment pattern is properly detected and timeslot 16 of the previous frame contains code other than zeros. If no valid pattern can be found in 12 to 14 milliseconds (no time out period exists if $CCR.1 = 1$ or $TEST = 1$), frame search is restarted.

FIXED CRC4 MULTIFRAME SYNC CRITERIA

CRC4 multiframe sync is declared if at least two valid CRC4 multiframe alignment signals are found within 12 to 14 milliseconds (8 ms if $CCR.1 = 1$ or $TEST = 1$) after frame alignment is completed. If not found within 12 to 14 milliseconds (8 ms if $CCR.1 = 1$ or $TEST = 1$), frame search is restarted. The search for the multiframe alignment signal is performed in timeslot 0 of frames not containing the frame alignment signal.

FIXED FRAME RESYNC CRITERIA

When enabled via $RCR.1$, the device will automatically initiate frame search whenever the frame alignment word is received in error three consecutive times.

FIXED CAS MULTIFRAME RESYNC CRITERIA

When enabled via $RCR.1$, the device will automatically initiate frame search whenever two consecutive CAS multiframe alignment words are received in error.

FIXED CRC4 RESYNC CRITERIA

If $CCR.1 = 1$ or if the TEST pin is tied high, then the DS2181A will initiate the resync at the FAS level if 915 or more CRC4 words out of 1000 are received in error.

CAS SIGNALLING SOURCE

CAS applications sample signalling data at TSER when $TCR.6 = 0$; an on-chip data multiplexer accepts channel-associated data input at TSD when $TCR.6 = 1$. The data multiplexer must be disabled ($TCR.6 = 0$) when the CCS mode is enabled ($TCR.5 = 1$).

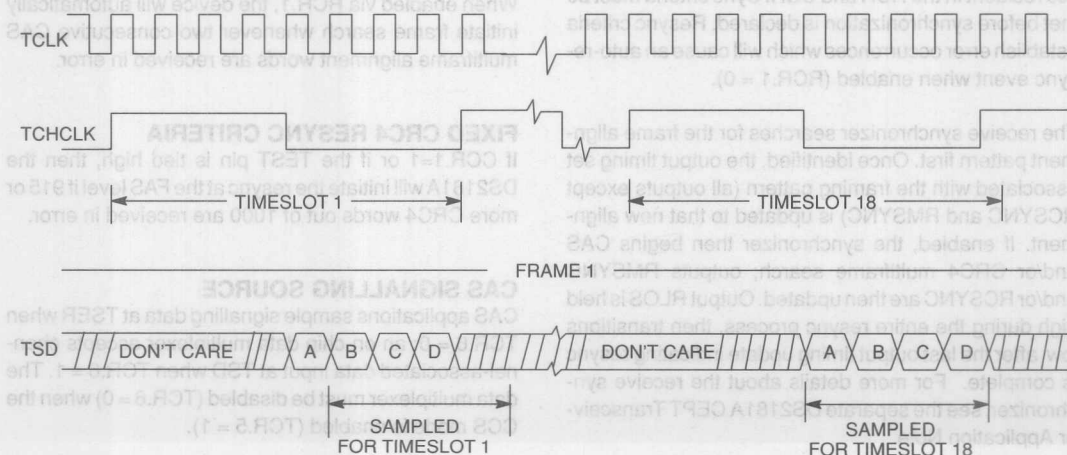
TSD INPUT TIMING (TCR.6 = 1; TCR.5 = 0) Table 6

FRAME #	TIMESLOT SIGNALLING DATA SAMPLED AT TSD
0	17
1	1,18
2	2,19
3	3,20
4	4,21
5	5,22
6	6,23
7	7,24
8	8,25
9	9,26
10	0,27
11	11,28
12	12,29
13	13,30
14	14,31
15	15

NOTE:

1. A, B, C and D data is sampled on falling edges of TCLK during bit times 5, 6, 7 and 8 of timeslots indicated.

TSD INPUT TIMING - Figure 7



CAS OUTPUT FORMAT IN TIMESLOT 16 Figure 8

Frame 0 ¹	Frame 1	Frame 15
0000XYXX	ABCD for timeslot 1	ABCD for timeslot 17
	---	ABCD for timeslot 15
		ABCD for timeslot 31

NOTE:

1. Timeslot 16 of frame 0 is reserved for the multiframe alignment word (0000), distant multiframe alarm (Y) and extra bits (X-XX).

TINR: TRANSMIT INTERNATIONAL AND NATIONAL REGISTER Figure 9

(MSB)		(LSB)					
INB	—	TRA	NB4	NB5	NB6	NB7	NB8
SYMBOL	POSITION	NAME AND DESCRIPTION					
INB	TINR.7	International Bit. Inserted into the outgoing data stream when TCR.4 = 1.					
—	TINR.6	Reserved; must be 0 for proper operation.					
TRA	TINR.5	Transmit Remote Alarm 0 = Normal operation; bit 3 of timeslot 0 in non-alignment frame clear. 1 = Alarm condition; bit 3 of timeslot 0 in non-align frames set.					
NB4	TINR.4	Transmit National Bits. Inserted into the outgoing data stream at TPOS and TNEG when TCR.3 = 1.					
NB5	TINR.3						
NB6	TINR.2						
NB7	TINR.1						
NB8	TINR.0						

TRANSMIT INTERNATIONAL AND NATIONAL DATA

Bit 1 of timeslot 0 in all frames is known as the international bit. When TCR.4 = 1, the transmitted international bit is sourced from TINR.7. When TCR.4 = 0, the transmitted international bit is sampled at TIND during the first bit period of each frame. The international bit positions in all outgoing frames except 13 and 15 are replaced by CRC4 codewords and the CRC4 multiframe alignment signal when CCR.3 = 1.

Bits 4 through 8 of timeslot 0 in non-align frames are reserved for national use. When TCR.3 = 1, the transmitted national bits are sourced from register locations TINR.4 through TINR.0. If TCR.3 = 0, the national bits are sampled at TIND during bit times 4 through 8 of timeslot 0 in non-align frames.

Reserved bit positions in the TINR must be set to 0 when written; those bits can be 0 or 1 when read.

TXR: TRANSMIT EXTRA REGISTER Figure 10

(MSB)				(LSB)			
—	—	—	—	XB1	TDMA	XB2	XB3
SYMBOL	POSITION	NAME AND DESCRIPTION					
—	TXR.7	Reserved; must be 0 for proper operation.					
—	TXR.6	Reserved; must be 0 for proper operation.					
—	TXR.5	Reserved; must be 0 for proper operation.					
—	TXR.4	Reserved; must be 0 for proper operation.					
XB1	TXR.3	Extra Bit 1					
TDMA	TXR.2	Transmit Distant Multiframe Alarm					
		0 = Normal operation; bit 6 of timeslot 16 in frame 0 clear.					
		1 = Alarm condition; bit 6 of timeslot 16 in frame 0 set.					
XB2	TXR.1	Extra Bit 2					
XB3	TXR.0	Extra Bit 3					

TRANSMIT EXTRA DATA

In the CAS mode, timeslot 16 of frame 0 contains the multiframe alignment pattern, extra bits and the distant multiframe alarm. When CAS is enabled (TCR.5 = 0), the extra bits are sourced from TXR.0, TXR.1 and TXR.3 (TCR.2 = 1) or the extra bits are sampled externally at TXD during the extra bit time (TCR.2 = 0). The

extra bits, alignment pattern and alarm signal are not utilized in the CCS mode (TCR.5 = 1); input TSER overwrites all timeslot 16 bit positions.

Reserved bit positions in the TXR must be set to 0 when written; those bits can be 0 or 1 when read.

TIR1 - TIR4: TRANSMIT IDLE REGISTERS Figure 11

(MSB)				(LSB)				
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0 ¹	TIR1
TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TIR2
TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16 ¹	TIR3
TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	TIR4
SYMBOL	POSITION	NAME AND DESCRIPTION						
TS31	TIR4.7	Transmit Idle Registers Each of these bit positions represents a timeslot in the outgoing stream at TPOS and TNEG; when set, the contents of that timeslot are forced to idle code (11010101).						
TS0	TIR1.0							

NOTE:

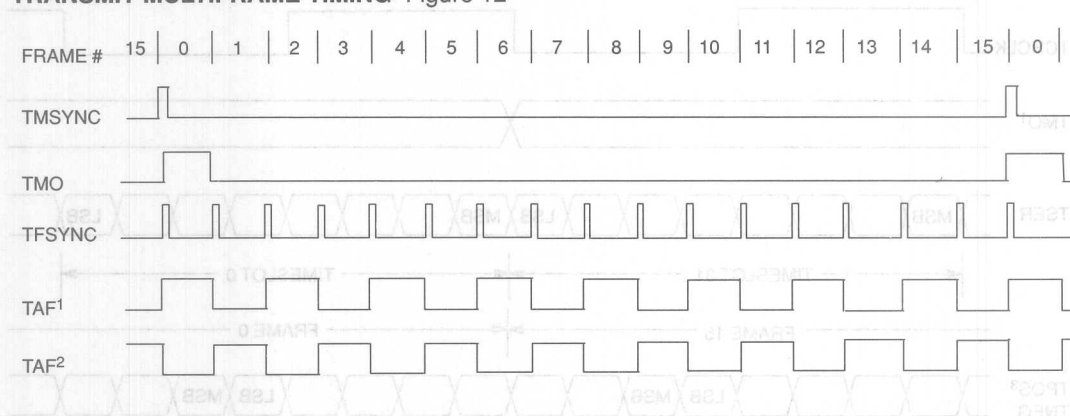
1. TS0 and TS16 are not affected by the idle register.

TRANSMIT TIMING

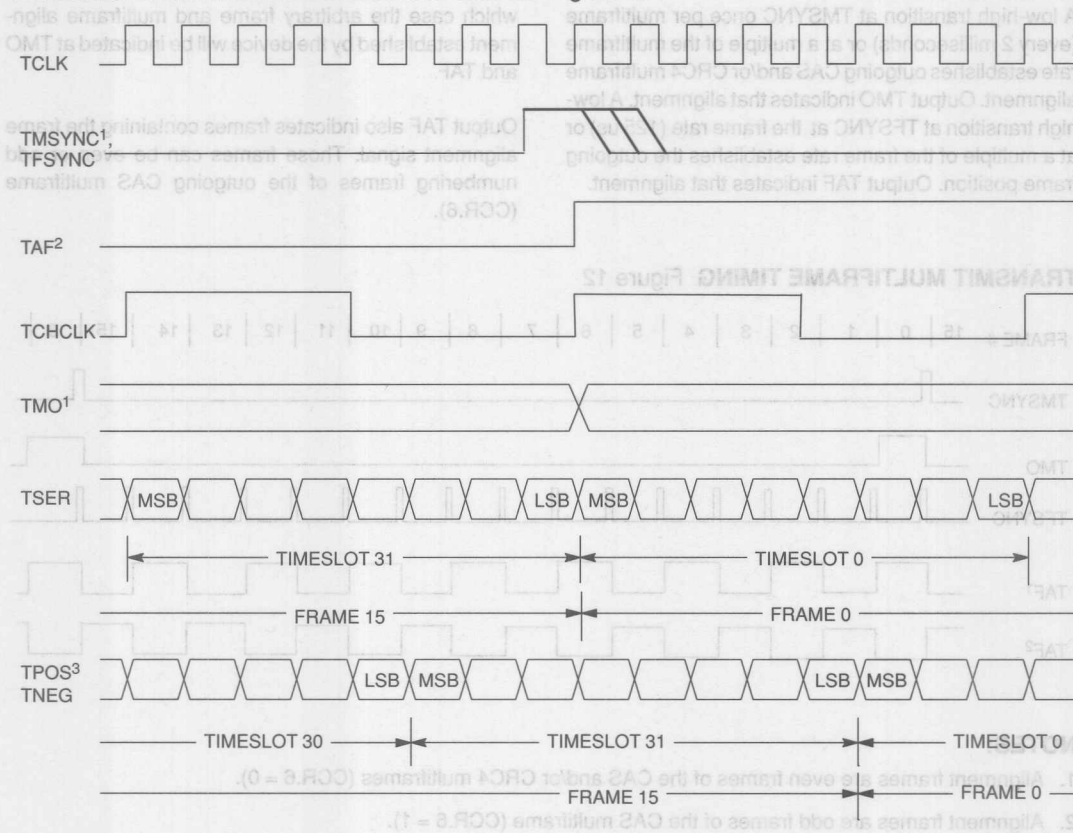
A low-high transition at TMSYNC once per multiframe (every 2 milliseconds) or at a multiple of the multiframe rate establishes outgoing CAS and/or CRC4 multiframe alignment. Output TMO indicates that alignment. A low-high transition at TFSYNC at the frame rate (125 us) or at a multiple of the frame rate establishes the outgoing frame position. Output TAF indicates that alignment.

TMSYNC and/or TFSYNC can be tied low by the user, in which case the arbitrary frame and multiframe alignment established by the device will be indicated at TMO and TAF.

Output TAF also indicates frames containing the frame alignment signal. Those frames can be even or odd numbering frames of the outgoing CAS multiframe (CCR.6).

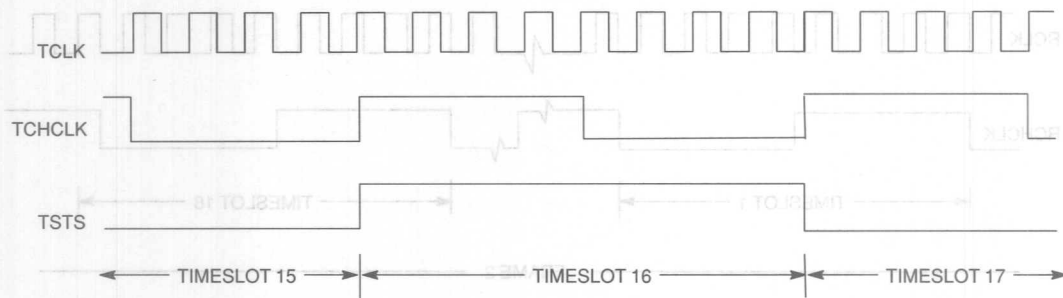
TRANSMIT MULTIFRAME TIMING Figure 12**NOTES:**

1. Alignment frames are even frames of the CAS and/or CRC4 multiframes (CCR.6 = 0).
2. Alignment frames are odd frames of the CAS multiframe (CCR.6 = 1).

TRANSMIT MULTIFRAME BOUNDARY TIMING Figure 13**NOTES:**

1. Low-high transitions on TMSYNC and/or TFSYNC must occur one TCLK period early with respect to actual frame and multiframe boundaries. TMO follows the rising edge of TMSYNC or TFSYNC.
2. TAF transitions on true frame boundaries.
3. Delay from TSER to TPOS, TNEG is five TCLK periods.

TRANSMIT SIGNALLING TIMESLOT TIMING Figure 14



RECEIVE SIGNALLING

Receive signalling data is available at two outputs: RSER and RSD. RSER outputs the signalling data in timeslot 16 at RSER. The signalling data is also ex-

tracted from timeslot 16 and presented at RSD during the timeslots shown in Table 7. This channel-associated signalling simplifies CAS system design.

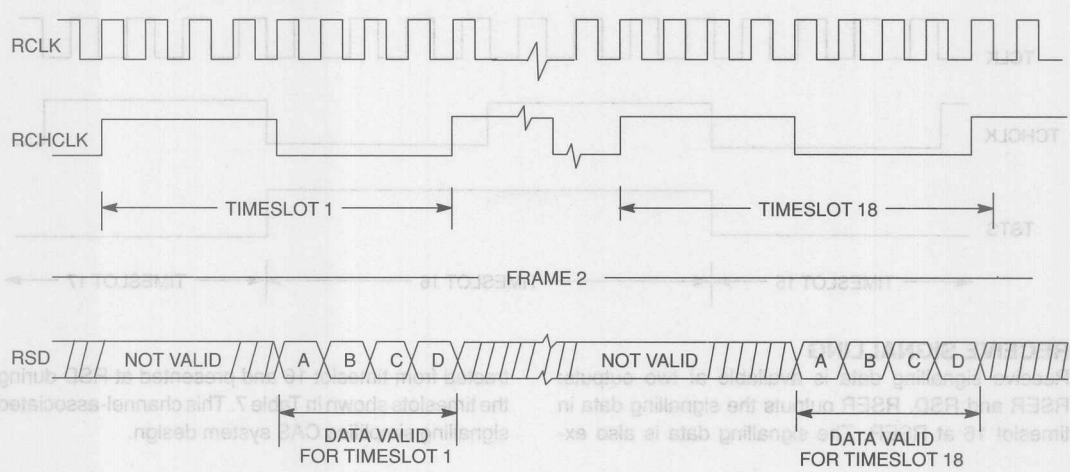
RECEIVE SIGNALLING Table 7

FRAME #	RSD ¹ VALID DURING TIMESLOT #
0	15,2
1	2,17
2	1,18
3	2,19
4	3,20
5	4,21
6	5,22
7	6,23
8	7,24
9	8,25
10	9,26
11	10,27
12	11,28
13	12,29
14	13,30
15	14,31

NOTES: (Applicable only to CAS systems.)

1. RSD is valid for the least significant nibble in each indicated timeslot. Timeslot A data appears in bit 5, B in bit 6, C in bit 7 and D in bit 8.
2. RSD does not output valid data during timeslots 0 and 16.

RECEIVE MULTIFRAME TIMING Figure 15



RECEIVE TIMING

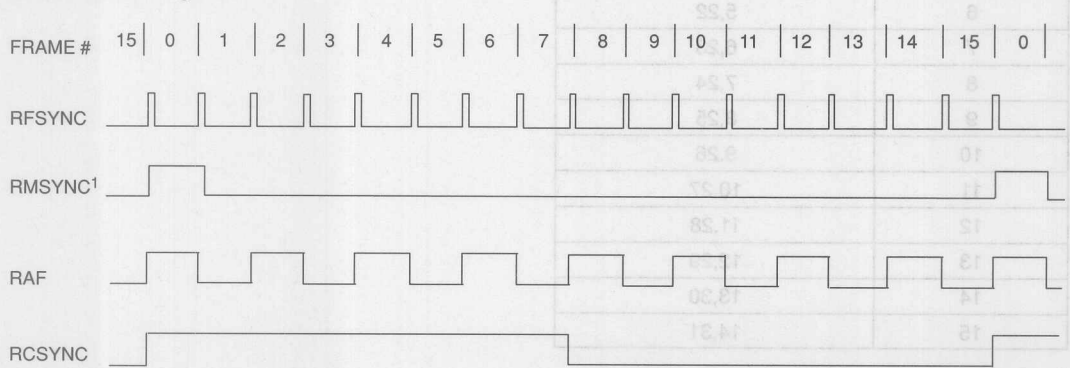
The receive side output timing set is identical to that found on the transmit side. The user can tie receive outputs directly to the transmit inputs for drop and insert

applications. The received data of RPOS, RNEG appear at RSER after six RCLK delays, without any change except for the HDB3-to-NRZ conversion when HDB3 is enabled.

NOTE:

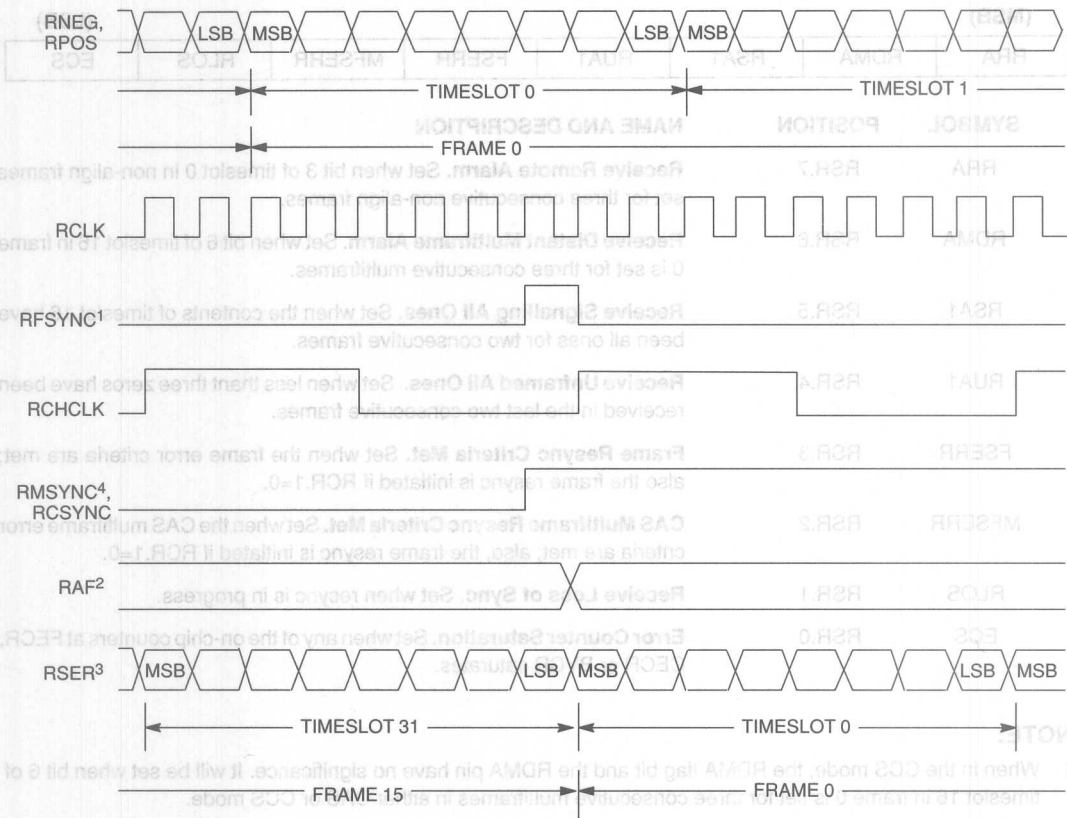
- 1. The CAS multiframe can start with an align or non-align frame. The CRC4 multiframe always starts with an align frame.

RSD TIMING Figure 16



NOTES: (Applicable only to CAS systems)
1. RSD is valid for the least significant nibble in each indicated timeslot. Timeslot A data appears in bit 5, B in bit 6, C in bit 7, and D in bit 8.
2. RSD does not output valid data during timeslots 0 and 16.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 17



NOTES:

1. Low-high transitions on RMSYNC and RFSYNC occur one RCLK period early with respect to actual frame and multiframe boundaries.
2. RAF transitions on true frame boundaries.
3. Delay from RPOS, RNEG to RSER is six RCLK periods.
4. RMSYNC and RCSYNC transition low on the falling edge of RFSYNC.

RSR: RECEIVE STATUS REGISTER Figure 18

(MSB)				(LSB)			
RRA	RDMA	RSA1	RUA1	FSERR	MFERR	RLOS	ECS
SYMBOL	POSITION	NAME AND DESCRIPTION					
RRA	RSR.7	Receive Remote Alarm. Set when bit 3 of timeslot 0 in non-align frames set for three consecutive non-align frames.					
RDMA	RSR.6	Receive Distant Multiframe Alarm. Set when bit 6 of timeslot 16 in frame 0 is set for three consecutive multiframe.					
RSA1	RSR.5	Receive Signalling All Ones. Set when the contents of timeslot 16 have been all ones for two consecutive frames.					
RUA1	RSR.4	Receive Unframed All Ones. Set when less than three zeros have been received in the last two consecutive frames.					
FSERR	RSR.3	Frame Resync Criteria Met. Set when the frame error criteria are met; also the frame resync is initiated if RCR.1=0.					
MFERR	RSR.2	CAS Multiframe Resync Criteria Met. Set when the CAS multiframe error criteria are met; also, the frame resync is initiated if RCR.1=0.					
RLOS	RSR.1	Receive Loss of Sync. Set when resync is in progress.					
ECS	RSR.0	Error Counter Saturation. Set when any of the on-chip counters at FECR, CECR or BVCR saturates.					

NOTE:

1. When in the CCS mode, the RDMA flag bit and the RDMA pin have no significance. It will be set when bit 6 of timeslot 16 in frame 0 is set for three consecutive multiframe in either CAS or CCS mode.

RIMR: RECEIVE INTERRUPT MASK REGISTER Figure 19

(MSB)				(LSB)			
RRA	RDMA	RSA1	RUA1	FSERR	MFSERR	RLOS	ECS
SYMBOL	POSITION	NAME AND DESCRIPTION					
RRA	RIMR.7	Receive Remote Alarm 1 = Interrupt enabled 0 = Interrupt masked					
RDMA	RIMR.6	Receive Distant Multiframe Alarm 1 = Interrupt enabled 0 = Interrupt masked					
RSA1	RIMR.5	Receive Signalling All 1's 1 = Interrupt enabled 0 = Interrupt masked					
RUA1	RIMR.4	Receive Unframed All 1's 1 = Interrupt enabled 0 = Interrupt masked					
FSERR	RIMR.3	Frame Resync Criteria Met 1 = Interrupt enabled 0 = Interrupt masked					
MFSERR	RIMR.2	CAS Multiframe Resync Criteria Met 1 = Interrupt enabled 0 = Interrupt masked					
RLOS	RIMR.1	Receive Loss of Sync 1 = Interrupt enabled 0 = Interrupt masked					
ECS	RIMR.0	Error Count Saturation 1 = Interrupt enabled 0 = Interrupt masked					

ALARM REPORTING AND INTERRUPT SERVICING

Alarm and error conditions are reported at outputs and the RSR. Use of the RSR and error count registers simplifies system error monitoring. The RSR can be read in one of two ways: a burst read does not disturb the RSR contents; a direct read will clear all bits set in the RSR unless the alarm condition which set them is still active.

Interrupts are enabled via the RIMR and are generated whenever an alarm or error condition sets an RSR bit. The host controller must service the transceiver in order to clear an interrupt condition. Clearing the appropriate RIMR bit will unconditionally clear an interrupt.

BVCR: BIPOLAR VIOLATION COUNT REGISTER Figure 20

(MSB)				(LSB)			
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0
SYMBOL	POSITION	NAME AND DESCRIPTION					
BVD7	BVCR.7	MSB of bipolar violation count.					
BVD0	BVCR.0	LSB of bipolar violation count.					

CECR: CRC4 ERROR COUNT REGISTER Figure 21

(MSB)				(LSB)			
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
SYMBOL	POSITION	NAME AND DESCRIPTION					
CRC7	BVCR.7	MSB of CRC4 error count.					
CRC0	BVCR.0	LSB of CRC4 error count.					

FECR: FRAME ERROR COUNT REGISTER Figure 22

(MSB)				(LSB)			
FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
SYMBOL	POSITION	NAME AND DESCRIPTION					
FE7	FECR.7	MSB of frame error count.					
FE0	FECR.0	LSB of frame error count.					

ERROR LOGGING

The BVCR, CECR and FECR contain 8-bit binary up counters which increment on individual bipolar violations, CRC4 code word errors (when CCR.2 = 1), and word errors in the frame alignment signal. Each counter saturates at 255. Once saturated, each following error occurrence will generate an interrupt (RIMR.0 = 1) until the register is reprogrammed to a value other than FF (hex). Presetting the registers allows the user to establish specific error count thresholds; the counter will count up to saturation from the preset value. The BVCR increments at all times (regardless of sync status), except when HDB3 code words are received with CCR.4=1. CECR and FECR increments are disabled whenever resync is in progress (RLOS high).

ALARM OUTPUTS

Alarm conditions are also reported real time at alarm outputs. These outputs can be used with off-chip logic to complement the on-chip error reporting capability of the DS2181A. In the hardware mode, they are the only alarm reporting means available.

RLOS

The RLOS output indicates the status of the receive synchronizer. When high, frame, CAS multiframe and/or CRC4 multiframe synchronization is in progress. A high-low transition indicates resync is complete. The RLOS bit (RSR.1) is a latched version of the RLOS output.

RRA

The remote alarm output transitions high when a remote alarm is detected. A high-low transition indicates the alarm condition has been cleared. The alarm condition is defined as bit 3 of time slot 0 set for three consecutive non-align frames. The alarm state is cleared when bit 3 has been clear for three consecutive non-align frames. The RRA bit (RSR.7) is a latched version of the RRA output.

RBV

RBV pulses high when the accused bit emerges at RSER. RBV will return low when RCLK goes low. Bipolar violations are also logged in the BVCR. The RBV pin provides a pulse for every violation which can be counted externally.

RDMA

RDMA transitions high when bit 6 of timeslot 16 in frame 0 is set for three consecutive occasions and returns low when the bit is clear for three consecutive occasions.

The RDMA bit (RSR.6) is a latched version of the RDMA output.

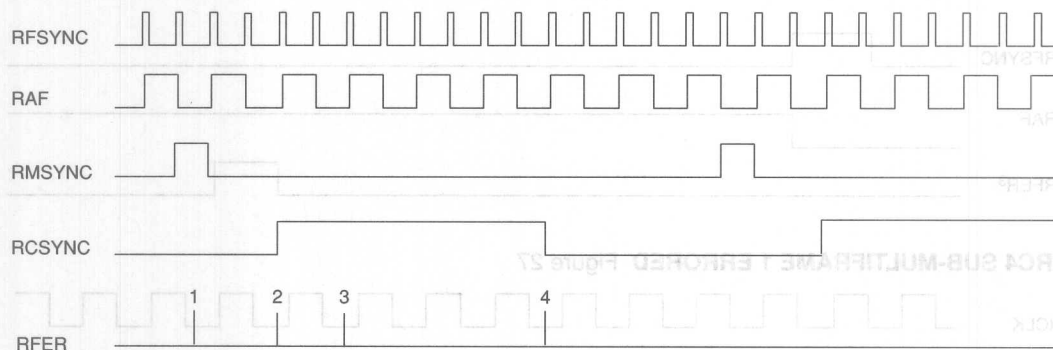
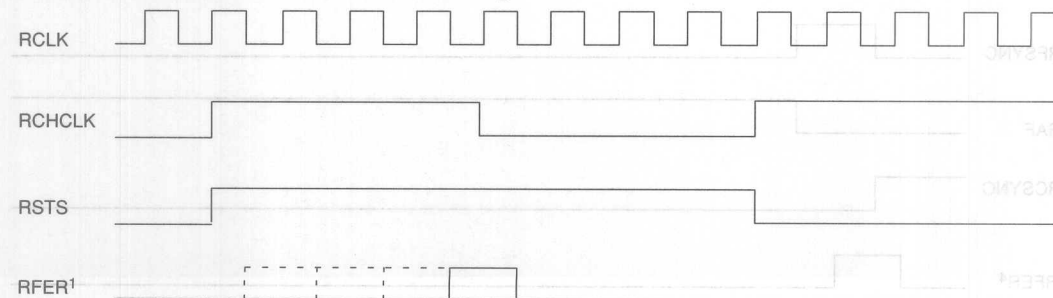
RCL

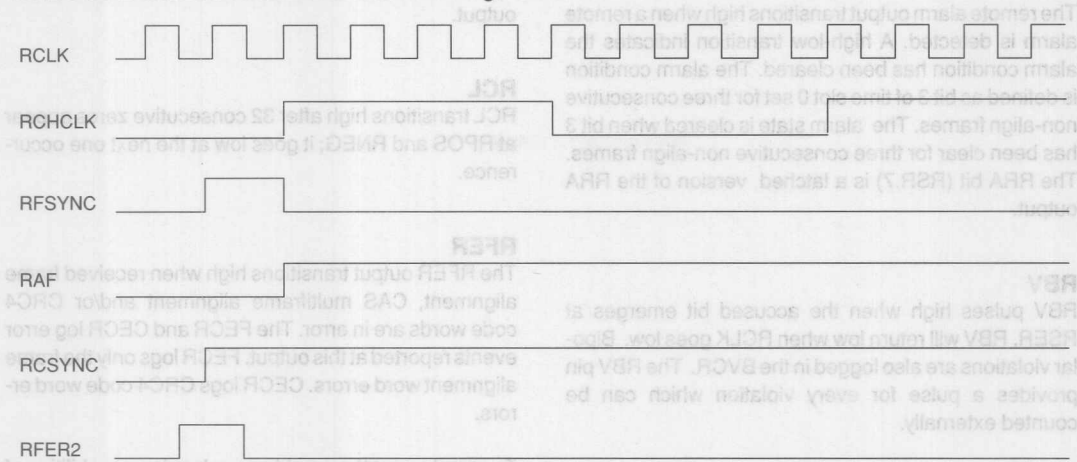
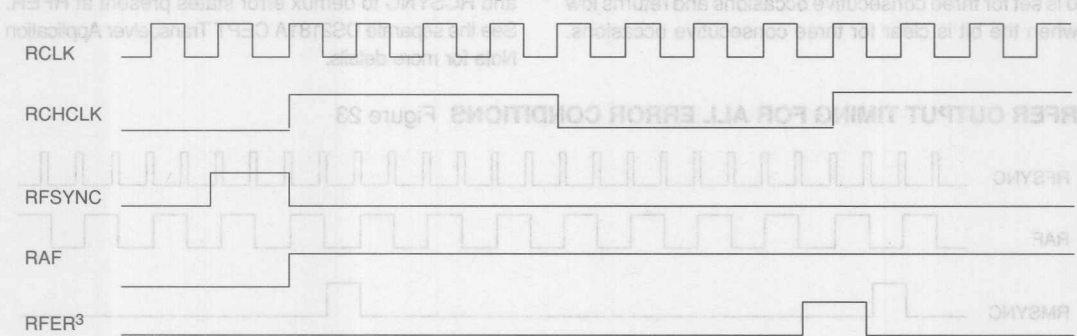
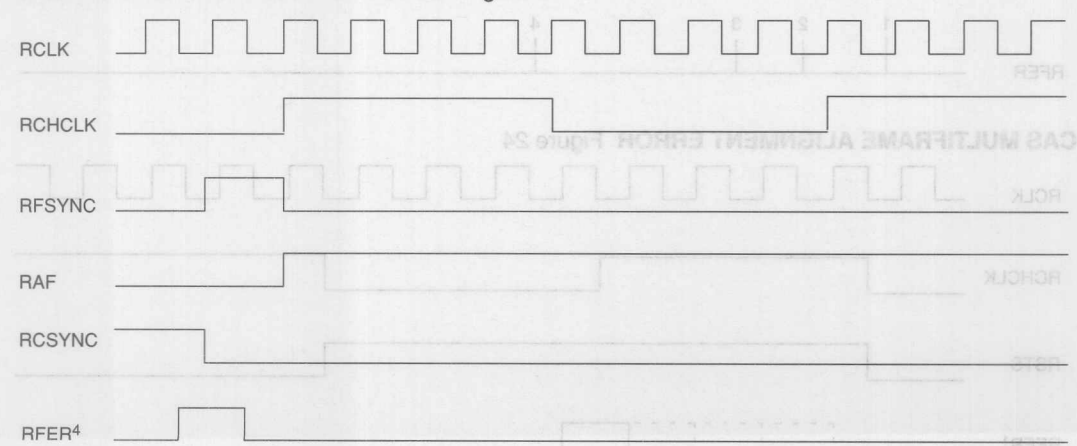
RCL transitions high after 32 consecutive zeros appear at RPOS and RNEG; it goes low at the next one occurrence.

RFER

The RFER output transitions high when received frame alignment, CAS multiframe alignment and/or CRC4 code words are in error. The FECR and CECR log error events reported at this output. FECR logs only the frame alignment word errors. CECR logs CRC4 code word errors.

To complement the on-chip error logging capabilities of the DS2181A, the system designer can use off-chip logic gated by receive side outputs RCHCLK, RAF, RSTS and RCSYNC to demux error states present at RFER. See the separate DS2181A CEPT Transceiver Application Note for more details.

RFER OUTPUT TIMING FOR ALL ERROR CONDITIONS Figure 23**CAS MULTIFRAME ALIGNMENT ERROR** Figure 24

CRC4 SUB-MULTIFRAME 2 ERRORED Figure 25**FRAME ALIGNMENT WORD ERRORED** Figure 26**CRC4 SUB-MULTIFRAME 1 ERRORED** Figure 27

NOTES FOR FIGURES 23 THROUGH 27:

1. CAS multiframe alignment word received in error; RFER will transition high at first error occurrence and remain high as shown.
2. Previous CRC4 sub-multiframe 2 errored.
3. Frame alignment word errored.
4. Previous CRC4 sub-multiframe 1 errored.

RESET

A high-low transition on $\overline{\text{RST}}$ clears all internal registers except the three error counters; a resync is initiated until $\overline{\text{RST}}$ returns high. $\overline{\text{RST}}$ must be held low on system power-up and when switching to/from the hardware mode. Following reset, the host processor should update all on-chip registers to establish desired operating modes.

do not require the features of the serial port. Tying SPS low disables the serial port, clears all internal register locations except those shown below, and redefines pins 14 through 18 as mode control inputs. The mode control inputs establish device operational characteristics as shown in Table 8. The hardware mode simplifies device retrofit into existing applications where control interfaces are designed with discrete logic.

HARDWARE MODE

An on-chip hardware control mode simplifies preliminary system prototyping and serves applications which

HARDWARE MODE CONTROL Table 8

PIN NUMBER	REGISTER LOCATION	NAME AND DESCRIPTION
14 (16)	TINR.5	TRA - Transmit Remote Alarm 0 = Normal operation 1 = Enable alarm
15 (17)	TXR.2	TDMA - Transmit Distant Multiframe Alarm 0 = Normal operation 1 = Enable alarm
16 (18)	CCR.5/CCR.4	Data Format 0 = Input and output data AMI coded 1 = Input and output data HDB3 coded
17 (19)	CCR.3/CCR.2	Transmit and Receive CRC4 Multiframe 0 = Disabled 1 = Enabled
18 (20)	TCR.5/RCR.5	Transmit and Receive CAS Multiframe 0 = Enabled 1 = Disabled

NOTE:

1. Pin numbers for PLCC package are listed in parenthesis.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground
 Operating Temperature
 Storage Temperature
 Soldering Temperature

-1.0V to 7.0V
 0°C to +70°C
 -55°C to 125°C
 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C, $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6	10	mA	1,2
Input Leakage	I_{IL}	-1.0		+1.0	μA	3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	5
Output Leakage	I_{LO}	-1.0		+1.0	μA	6

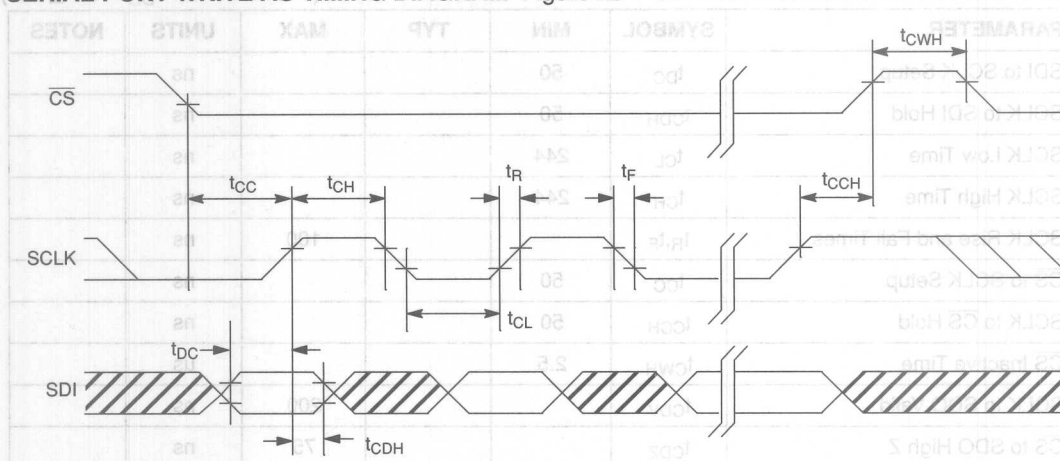
NOTES:

1. $TCLK = RCLK = 2.048$ MHz.
2. Outputs open.
3. $0V < V_{IN} < V_{DD}$.
4. All outputs except \overline{INT} which is open collector.
5. All outputs.
6. Applies to SDO when tri-stated.

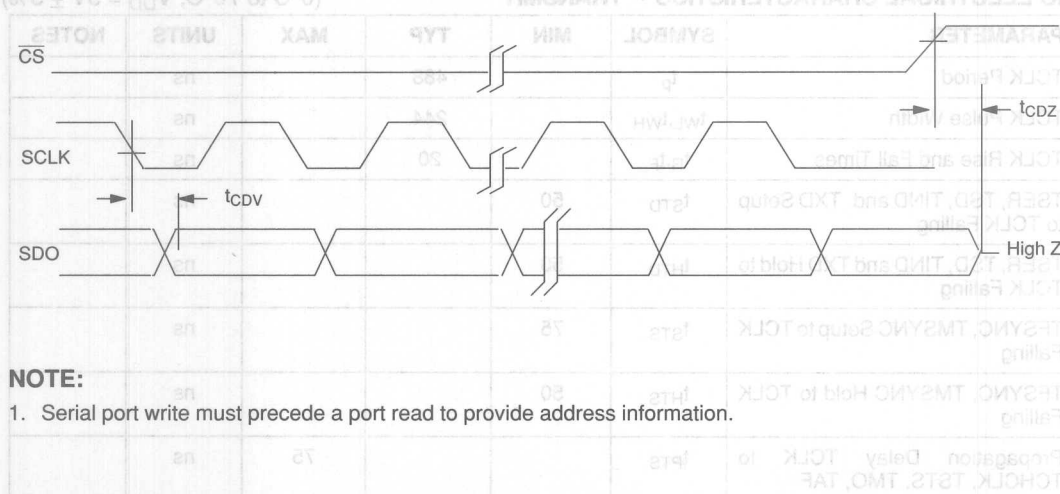
Transmit and Receive CAS Multiturn	0 = Enabled 1 = Disabled	18 (20)
------------------------------------	-----------------------------	------------

NOTE:

1. Pin numbers for PLOC package are listed in parentheses.

SERIAL PORT WRITE AC TIMING DIAGRAM Figure 28**NOTE:**

1. Shaded regions indicate "don't care" states of input data.

SERIAL PORT READ¹ AC TIMING Figure 29**NOTE:**

1. Serial port write must precede a port read to provide address information.

AC ELECTRICAL CHARACTERISTICS^{1,2} SERIAL PORT (0°C to 70°C, $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t_{DC}	50			ns	
SCLK to SDI Hold	t_{CDH}	50			ns	
SCLK Low Time	t_{CL}	244			ns	
SCLK High Time	t_{CH}	244			ns	
SCLK Rise and Fall Times	t_R, t_F			100	ns	
\overline{CS} to SCLK Setup	t_{CC}	50			ns	
SCLK to \overline{CS} Hold	t_{CCH}	50			ns	
\overline{CS} Inactive Time	t_{CWH}	2.5			us	
SCLK to SDO Valid	t_{CDV}			200	ns	
\overline{CS} to SDO High Z	t_{CDZ}			75	ns	

NOTES:

1. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8$ and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

AC ELECTRICAL CHARACTERISTICS^{1,2} TRANSMIT (0°C to 70°C, $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_p		488		ns	
TCLK Pulse Width	t_{WL}, t_{WH}		244		ns	
TCLK Rise and Fall Times	t_R, t_F		20		ns	
TSER, TSD, TIND and TXD Setup to TCLK Falling	t_{STD}	50			ns	
TSER, TSD, TIND and TXD Hold to TCLK Falling	t_{HTD}	50			ns	
TFSYNC, TMSYNC Setup to TCLK Falling	t_{STS}	75			ns	
TFSYNC, TMSYNC Hold to TCLK Falling	t_{HTS}	50			ns	
Propagation Delay TCLK to TCHCLK, TSTS, TMO, TAF	t_{PTS}			75	ns	

NOTES:

1. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8$ and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

AC ELECTRICAL CHARACTERISTICS^{1,2} RECEIVE (0°C to 70°C, $V_{DD} = 5V \pm 5\%$)

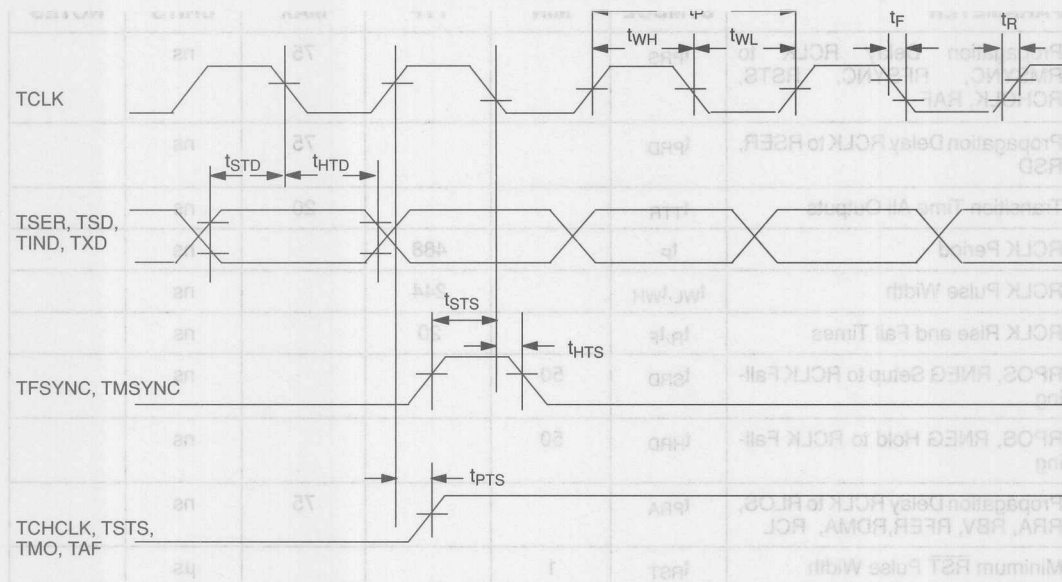
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay RCLK to RMSYNC, RFSYNC, RSTS, RCHCLK, RAF	t_{PRS}			75	ns	
Propagation Delay RCLK to RSER, RSD	t_{PRD}			75	ns	
Transition Time All Outputs	t_{TTR}			20	ns	
RCLK Period	t_p		488		ns	
RCLK Pulse Width	t_{WL}, t_{WH}		244		ns	
RCLK Rise and Fall Times	t_R, t_F		20		ns	
RPOS, RNEG Setup to RCLK Fall-ing	t_{SRD}	50			ns	
RPOS, RNEG Hold to RCLK Fall-ing	t_{HRD}	50			ns	
Propagation Delay RCLK to RLOS, RRA, RBV, RFER, RDMA, RCL	t_{PRA}			75	ns	
Minimum RST Pulse Width	t_{RST}	1			μs	

NOTES:

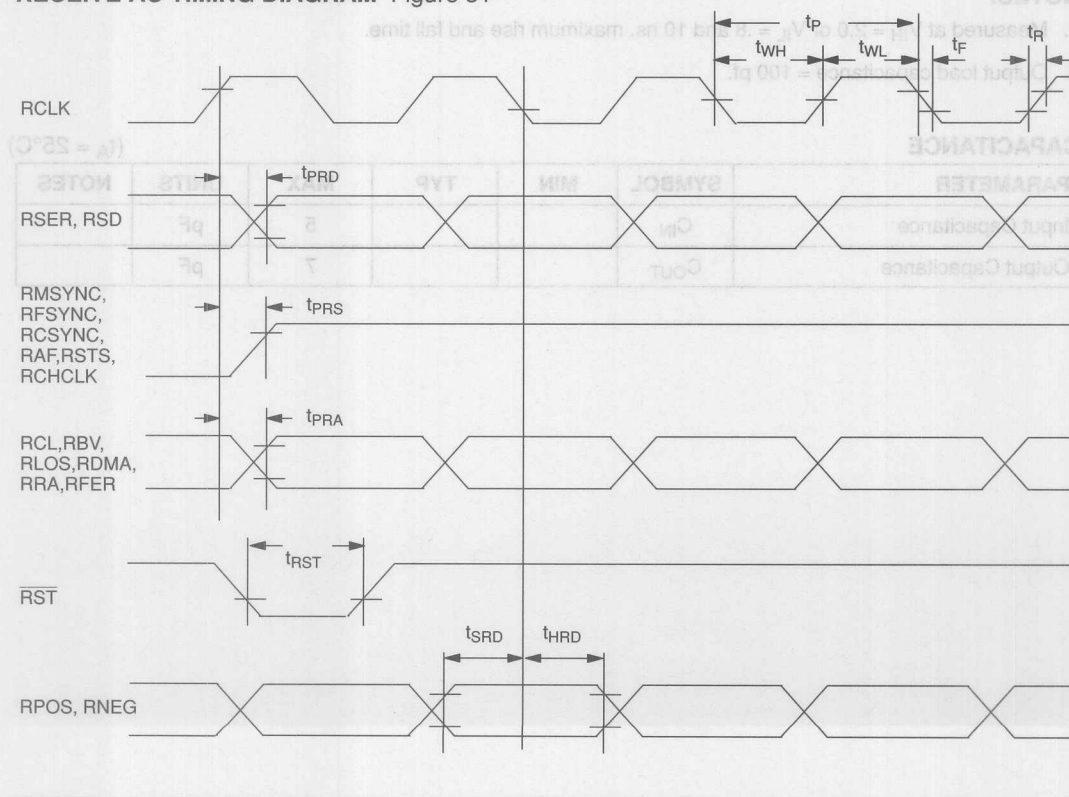
1. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8$ and 10 ns. maximum rise and fall time.
2. Output load capacitance = 100 pf.

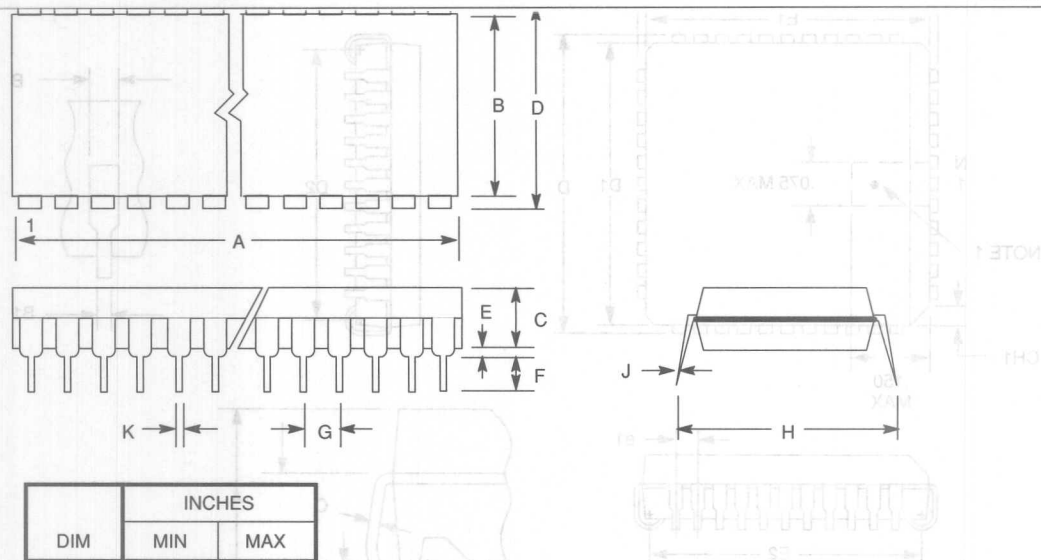
CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	



RECEIVE AC TIMING DIAGRAM Figure 31

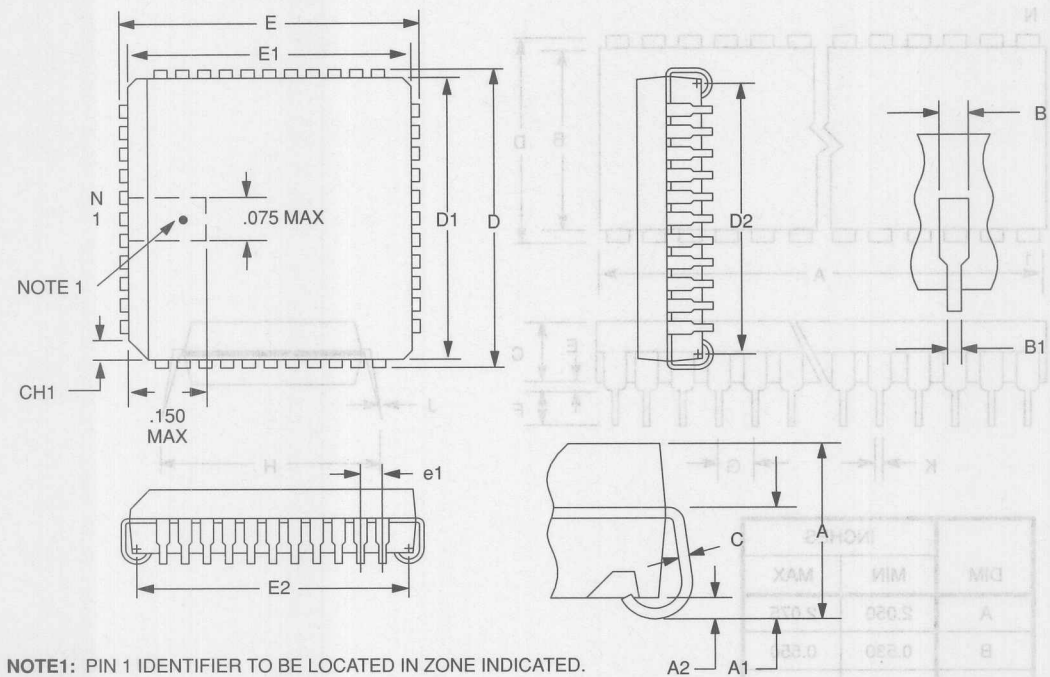




DIM	INCHES	
	MIN	MAX
A	2.050	2.075
B	0.530	0.550
C	0.140	0.160
D	0.600	0.625
E	0.015	0.040
F	0.120	0.145
G	0.090	0.110
H	0.625	0.675
J	0.008	0.012
K	0.015	0.022
N	40	

DIM	INCHES	
	MIN	MAX
A	0.015	0.018
A1	0.020	0.025
AS	0.020	—
B	0.020	0.025
B1	0.015	0.020
C	0.005	0.010
CH1	0.040	0.045
D	0.020	0.025
D1	0.020	0.025
D2	0.020	0.025
E	0.020	0.025
E1	0.020	0.025
E2	0.020	0.025
E3	0.020	0.025
E4	0.020	0.025
E5	0.020	0.025
E6	0.020	0.025
E7	0.020	0.025
E8	0.020	0.025
E9	0.020	0.025
E10	0.020	0.025
E11	0.020	0.025
E12	0.020	0.025
E13	0.020	0.025
E14	0.020	0.025
E15	0.020	0.025
E16	0.020	0.025
E17	0.020	0.025
E18	0.020	0.025
E19	0.020	0.025
E20	0.020	0.025
E21	0.020	0.025
E22	0.020	0.025
E23	0.020	0.025
E24	0.020	0.025
E25	0.020	0.025
E26	0.020	0.025
E27	0.020	0.025
E28	0.020	0.025
E29	0.020	0.025
E30	0.020	0.025
E31	0.020	0.025
E32	0.020	0.025
E33	0.020	0.025
E34	0.020	0.025
E35	0.020	0.025
E36	0.020	0.025
E37	0.020	0.025
E38	0.020	0.025
E39	0.020	0.025
E40	0.020	0.025
E41	0.020	0.025
E42	0.020	0.025
E43	0.020	0.025
E44	0.020	0.025
E45	0.020	0.025
E46	0.020	0.025
E47	0.020	0.025
E48	0.020	0.025
E49	0.020	0.025
E50	0.020	0.025
E51	0.020	0.025
E52	0.020	0.025
E53	0.020	0.025
E54	0.020	0.025
E55	0.020	0.025
E56	0.020	0.025
E57	0.020	0.025
E58	0.020	0.025
E59	0.020	0.025
E60	0.020	0.025
E61	0.020	0.025
E62	0.020	0.025
E63	0.020	0.025
E64	0.020	0.025
E65	0.020	0.025
E66	0.020	0.025
E67	0.020	0.025
E68	0.020	0.025
E69	0.020	0.025
E70	0.020	0.025
E71	0.020	0.025
E72	0.020	0.025
E73	0.020	0.025
E74	0.020	0.025
E75	0.020	0.025
E76	0.020	0.025
E77	0.020	0.025
E78	0.020	0.025
E79	0.020	0.025
E80	0.020	0.025
E81	0.020	0.025
E82	0.020	0.025
E83	0.020	0.025
E84	0.020	0.025
E85	0.020	0.025
E86	0.020	0.025
E87	0.020	0.025
E88	0.020	0.025
E89	0.020	0.025
E90	0.020	0.025
E91	0.020	0.025
E92	0.020	0.025
E93	0.020	0.025
E94	0.020	0.025
E95	0.020	0.025
E96	0.020	0.025
E97	0.020	0.025
E98	0.020	0.025
E99	0.020	0.025
E100	0.020	0.025

DS2181AQ CEPT TRANSCEIVER (PLCC)



DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	—

INCHES		DIM
MAX	MIN	
0.180	0.165	A
0.120	0.090	A1
0.020	—	A2
0.033	0.026	B
0.021	0.013	B1
0.012	0.009	C
0.048	0.042	CH1
0.695	0.685	D
0.656	0.650	D1
0.630	0.590	D2
0.695	0.685	E
0.656	0.650	E1
0.630	0.590	E2
0.050 BSC		e1
—	44	N

DALLAS

SEMICONDUCTOR

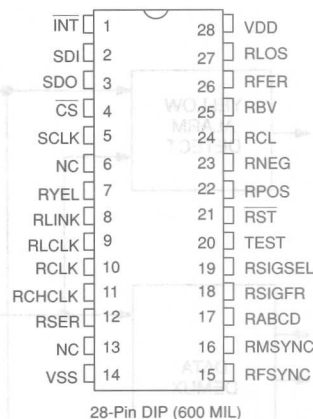
DS2182A

T1 Line Monitor

FEATURES

- Performs framing and monitoring functions
- Supports Superframe and Extended Superframe formats
- Four onboard error counters
 - 16-bit bipolar violation
 - 8-bit CRC
 - 8-bit OOF
 - 8-bit frame bit error
- Indication of the following
 - yellow and blue alarms
 - incoming B8ZS code words
 - 8 and 16 zero strings
 - change of frame alignment
 - loss of sync
 - carrier loss
- Simple serial interface used for configuration, control and status monitoring
- Burst mode allows quick access to counters for status updates
- Automatic counter reset feature
- Single 5V supply; low-power CMOS technology
- Available in 28-pin DIP and 28-pin PLCC
- The DS2182A is upward-compatible from the original DS2182

PIN ASSIGNMENT



The updated DS2182A includes the following changes from the original DS2182:

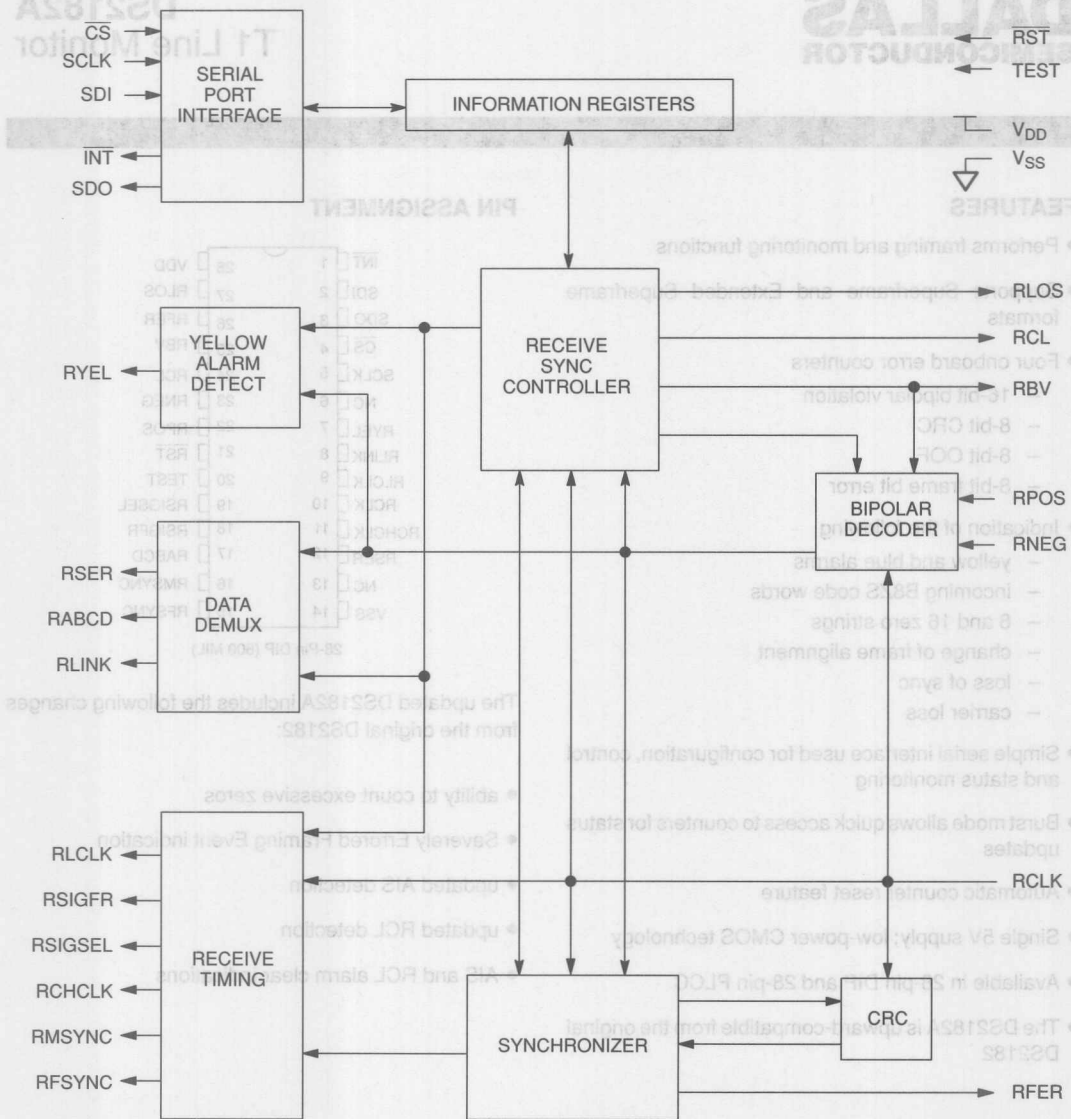
- ability to count excessive zeros
- Severely Errored Framing Event indication
- updated AIS detection
- updated RCL detection
- AIS and RCL alarm clear indications

DESCRIPTION

The DS2182A T1 Line Monitor Chip is a monolithic CMOS device designed to monitor real-time performance on T1 lines. The DS2182A frames to the data on the line, counts errors, and supplies detailed information about the status and condition of the line. Large onboard counters allow the accumulation of errors for ex-

tended periods, which permits a single CPU to monitor a number of T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of S-Bits, FDL bits, signaling bits, and channel data. The DS2182A meets the requirements of ANSI T1.231.

DS2182A BLOCK DIAGRAM Figure 1



The DS2182A T1 Line Monitor Chip is a monolithic CMOS device designed to monitor real-time performance on T1 lines. The DS2182A frames to the data on the line, counts errors, and supplies detailed information about the status and condition of the line. It also on-board counters allow the accumulation of errors for extended periods, which permits single CPU to monitor multiple T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of 8-bits, FDL bits, signaling bits, and channel data. The DS2182A meets the requirements of ANSI T1.301.

DESCRIPTION

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PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
6	NC	-	No Connect. No internal connection. This pin can be tied to either V_{SS} or V_{DD} , or it can be floated.
7	RYEL	O	Receive Yellow Alarm. Transitions high when yellow alarm detected; goes low when alarm clears.
8	RLINK	O	Receive Link Data. Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
9	RLCLK	O	Receive Link Clock. 4 KHz demand clock for RLINK.
10	RCLK	I	Receive Clock. 1.544 MHz primary clock.
11	RCHCLK	O	Receive Channel Clock. 192 KHz clock; identifies time slot (channel) boundaries.
12	RSER	O	Receive Serial Data. Received NRZ serial data; updated on rising edges of RCLK.
13	NC	-	No Connect. No internal connection. This pin can be tied to either V_{SS} or V_{DD} , or it can be floated.
15	RFSYNC	O	Receive Frame Sync. Extracted 8 KHz clock, one RCLK wide; F-bit position in each frame.
16	RMSYNC	O	Receive Multiframe Sync. Extracted multiframe sync; positive-going edge indicates start of multiframe; 50% duty cycle.
17	RABCD	O	Receive ABCD Signaling. Extracted signaling data output; valid for each channel in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
18	RSIGFR	O	Receive Signaling Frame. High during signaling frames; low during non-signaling frames (and during resync).
19	RSIGSEL	O	Receive Signaling Select. In 193E framing, a .667 KHz clock that identifies signaling frames A and C; a 1.33 KHz clock in 193S.
21	RST	I	Reset. A high-low transition clears all internal registers and resets counters. A high-low-high transition initiates a resync.
22 23	RPOS RNEG	I	Receive Bipolar Data Inputs. Sampled on falling of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
24	RCL	O	Receive Carrier Loss. High if 192 consecutive 0s appear at RPOS and RNEG; goes low upon seeing 12.5% one's density.
25	RBV	O	Receive Bipolar Violation. High during accused bit time at RSER. If bipolar violation detected, low otherwise.
26	RFER	O	Receive Frame Error. High during F-bit time when FT or FS errors occur (193S), or when FPS or CRC errors occur (193E). Low during resync.
27	RLOS	O	Receive Loss of Sync. Indicates sync status; high when internal resync is in progress, low otherwise.

PORT PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
1	INT	O	Receive Alarm Interrupt. Flags host controller during alarm conditions. Active low; open drain output.
2	SDI	I	Serial Data In. Data for onboard registers. Sampled on rising edge of SCLK.
3	SDO	O	Serial Data Out. Control and status information from onboard registers. Updated on falling edge of SCLK; tri-stated during serial port write or when CS is high.
4	CS	I	Chip Select. Must be low to read or write the serial port.
5	SCLK	I	Serial Data Clock. Used to read or write the serial port registers.

POWER AND TEST PIN DESCRIPTION Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
14	V _{SS}	—	Signal Ground. 0.0 volts.
20	TEST	I	Test Mode. Tie to V _{SS} for normal operation.
28	V _{DD}	—	Positive Supply. 5.0 volts.

REGISTER SUMMARY Table 4

REGISTER	ADDRESS	DESCRIPTION/FUNCTION
BVCR2	0000	Bipolar Violation Count Register 2. LSW of a 16-bit presetable counter that records individual bipolar violations.
BVCR1	0001	Bipolar Violation Count Register 1. MSW of a 16-bit presetable counter that records individual bipolar violations.
CRCCR	0010	CRC Error Count Register. 8-bit presetable counter that records CRC6 errored words in the 193E frame mode.
OOF CR	0011	OOFCR Count Register. 8-bit presetable counter that records OOF events. OOF events are defined by RCR1.5 and RCR1.6.
FE CR	0100	Frame Error Count Register. 8-bit presetable counter that records individual bit errors in the framing pattern.
RSR1	0101	Receive Status Register 1. Reports alarm conditions.
RIMR1	0110	Receive Interrupt Mask Register 1. Allows masking of individual alarm-generated interrupts from RSR1.
RSR2	0111	Receive Status Register 2. Reports alarm conditions.
RIMR2	1000	Receive Interrupt Mask Register 2. Allows masking of individual alarm-generated interrupts from RSR2.
RCR1	1001	Receive Control Register 1. Programs device operating characteristics.
RCR2	1010	Receive Control Register 2. Programs device operating characteristics.

SERIAL PORT INTERFACE

The port pins of the DS2182A serve as a microprocessor/microcontroller-compatible serial port. Eleven on-board registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. The port on the DS2182A can be read from or written to at any time. Serial port reads and writes are independent of T1 line timing signals RCLK, RPOS, and RNEG. However, RCLK is needed in order to clear RSR1 and RSR2 after reads.

ADDRESS/COMMAND

Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. The following four bits identify the register address. The next two bits are reserved and must be set to 0 for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively read or written to. Data is read and written to the DS2182A LSB first.

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the \overline{CS} input low. Input data is latched on the rising edge of SCLK and

must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the \overline{CS} input transitions high. Port control logic is disabled and SDO is tri-stated when \overline{CS} is high.

DATA I/O

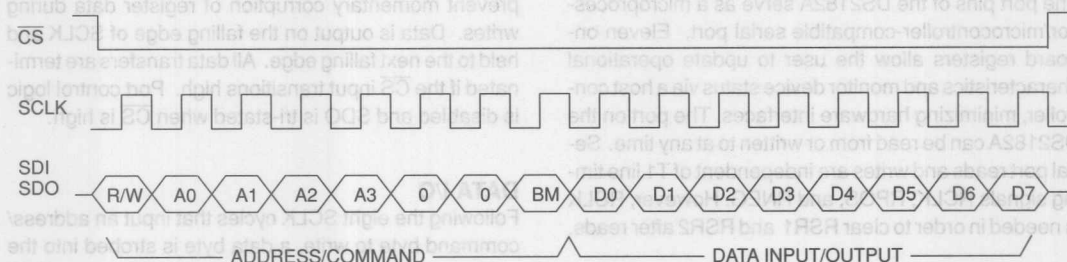
Following the eight SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edge of the next eight SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next eight SCLK cycles. The SDO pin is tri-stated during device write and can be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE

The burst mode allows all onboard registers to be consecutively written to or read by the host processor. A burst read is used to poll all registers; RSR1 and RSR2 contents will be unaffected. This feature minimizes device initialization time on system power-up or reset. Burst mode is initiated when ACB.7 is set and the address is 0000. A burst is terminated by a low-high transition on \overline{CS} .

ACB: ADDRESS COMMAND BYTE Figure 2

(MSB)				(LSB)			
BM	—	—	ADD3	ADD2	ADD1	ADD0	R/W
SYMBOL	POSITION	NAME AND DESCRIPTION					
BM	ACB.7	Burst Mode. If set (and register address is 0000) burst read or write is enabled.					
—	ACB.6	Reserved, must be 0 for proper operation.					
—	ACB.5	Reserved, must be 0 for proper operation.					
ADD3	ACB.4	MSB of register address.					
ADD0	ACB.1	LSB of register address.					
R/W	ACB.0	Read/Write Select. 0 = write addressed register 1 = read addressed register					

SERIAL PORT READ/WRITE Figure 3**NOTES:**

1. SDI is sampled on rising edge of SCLK.
2. SDO is updated on falling edge of SCLK.

OPERATION OF THE COUNTERS

All four of the counters in the DS2182A can be preset by the user to establish an event count interrupt threshold. The counters count up from the preset value until they reach saturation. At saturation, each additional event occurrence sets the appropriate bit in RSR2 and generates an interrupt if enabled by RIMR2.

The DS2182A contains an auto counter reset feature in the burst read mode. If RCR1.4 is set, then the user can burst read the four counters (five registers), and all four counters will be automatically reset to 0 after the read takes place. Since the burst mode can be terminated at any time by taking \overline{CS} high, the user has the option of

reading all of the registers or only the counters. If RCR1.4 is set, then any read of the registers, burst mode or not, will clear the count in all four counters. If the user wishes to read the port and not clear the counters, then RCR1.4 must be cleared first.

The counter registers can be read or written to at any time with the serial port, which operates totally asynchronously with the monitoring of the T1 line. Reading a register will not affect the count as long as RCR1.4 is cleared. The dual buffer architecture of the DS2182A insures that no error events will be missed while the serial port is being accessed for reads.

BVCR1: BIPOLAR VIOLATION COUNT REGISTER 1;
BVCR2: BIPOLAR VIOLATION COUNT REGISTER 2 Figure 4

(MSB)				(LSB)			
BV7	BV6	BV5	BV4	BV3	BV2	BV1	BV0

SYMBOL	POSITION	NAME AND DESCRIPTION
BV7	BVCR.7	MSB of bipolar violation count
BV0	BVCR.0	LSB of bipolar violation count

Bipolar Violation Count Register 1 (BVCR1) is the most significant word and BVCR2 is the least significant word of a presetable 16-bit counter that records individual bipolar violations. If the B8ZS mode is enabled (RCR2.2 = 1), then B8ZS code words are not counted. The BVCR can also be programmed to count excessive zeros by setting the RCR2.5 bit. In this mode, the BVCR will

count occurrences of 8 consecutive zeros when B8ZS is enabled or 16 consecutive zeros when B8ZS is disabled. This counter increments at all times and is not disabled by a loss of sync condition (RLOS = 1). The counter saturates at 65,535 and generates an interrupt for each occurrence after saturation if RIMR2.0 is set.

NOTE:

1. In order to properly preset the Bipolar Violation Count Register, BVCR2 must be written to before BVCR1 is written to.

CRCCR: CRC COUNT REGISTER Figure 5

(MSB)				(LSB)			
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC7	CRCCR.7	MSB of CRC6 word error count
CRC0	CRCCR.0	LSB of CRC6 word error count

The CRC Count Register (CRCCR) is an 8-bit presettable counter that records word errors in the Cyclic Redundancy Check (CRC). This 8-bit binary counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.1 is set. The count

in this register is only valid in the 193E framing mode (RCR2.4 = 1) and is reset and disabled in the 193S framing mode (RCR2.4 = 0). The count is disabled during a loss of sync condition (RLOS = 1).

OOF CR: OOF COUNT REGISTER Figure 6

(MSB)				(LSB)			
OOF7	OOF6	OOF5	OOF4	OOF3	OOF2	OOF1	OOF0

SYMBOL	POSITION	NAME AND DESCRIPTION
OOF7	OOF CR.7	MSB of OOF event count
OOF0	OOF CR.0	LSB of OOF event count

The OOF Count Register (OOF CR) is an 8-bit presettable counter that records Out Of Frame (OOF) events. OOF events are defined by RCR1.5 and RCR1.6. This 8-bit counter saturates at 255 and generates an inter-

rupt for each occurrence after saturation if RIMR2.2 is set. The count is disabled during a loss of sync condition (RLOS = 1).

FE CR: FRAME ERROR COUNT REGISTER Figure 7

(MSB)				(LSB)			
FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0

SYMBOL	POSITION	NAME AND DESCRIPTION
FE7	FE CR.7	MSB of frame error count
FE0	FE CR.0	LSB of frame error count

The Frame Error Count Register (FE CR) is an 8-bit presettable counter that records individual frame bit errors. In the 193E mode (RCR2.4 = 1), the FE CR records bit errors in the FPS framing pattern (001011). In the 193S mode (RCR2.4 = 0), the FE CR records bit errors in both the FT (101010) and FS (001110) framing patterns if

RCR1.3 is set. If RCR1.3 is cleared, then the FE CR only records bit errors in the FT pattern. This 8-bit counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.3 is set. The count is disabled during a loss of sync condition (RLOS = 1).

RSR1: RECEIVE STATUS REGISTER 1 Figure 8

(MSB)				(LSB)			
8ZD	16ZD	RCL	RYEL	RLOS	B8ZSD	RBL	COFA
SYMBOL	POSITION	NAME AND DESCRIPTION					
8ZD	RSR1.7	8 Zero Detect. Set when a string of eight consecutive 0s has been received at RPOS and RNEG.					
16ZD	RSR1.6	16 Zero Detect. Set when a string of 16 consecutive 0s has been received at RPOS and RNEG.					
RCL	RSR1.5	Receive Carrier Loss. Set when a string of 192 consecutive 0s has been received at RPOS and RNEG. Cleared when 14 or more ones out of 112 possible bit positions are received.					
RYEL	RSR1.4	Receive Yellow Alarm. Set when yellow alarm is detected. The format of yellow alarm is determined by RCR2.3 and RCR2.4.					
RLOS	RSR1.3	Receive Loss of Sync. Set when resync is in progress.					
B8ZSD	RSR1.2	B8ZS Code Word Detect. Set when a B8ZS code word is received at RPOS and RNEG independent of whether the B8ZS mode is enabled or not (RCR2.2).					
RBL	RSR1.1	Receive Blue Alarm. Set when over a 3 ms window, 5 or less zeros are received. Cleared when over a 3 ms window, 6 or more zeros are received.					
COFA	RSR1.0	Change of Frame Alignment. Set when the last resync resulted in a change of frame or multiframe alignment.					

NOTE:

1. Alarms 8ZD and 16ZD are cleared on the next occurrence of a 1 at RPOS and RNEG.

RECEIVE STATUS REGISTERS

The receive status registers (RSR1 and RSR2) can be used in either a polled or an interrupt configuration. In a polled configuration, the user reads the RSR at regular intervals to check for alarms. In an interrupt configuration, the user monitors the INT pin. When the INT pin goes low, an alarm condition has occurred and has been reported in one of the RSRs. The processor can then read the RSRs to find which bits have been set. All of the bits in the RSRs operate in a latched fashion. That is, once set, they remain set until read. The bits in the RSR are cleared when read unless the read was performed in the burst mode or the alarm condition still exists.

YELLOW ALARM

193S BIT 2. If RCR2.4 = 0 and RCR2.3 = 0, then the DS2182A examines bit 2 of all incoming channels for

the presence of a yellow alarm. If bit 2 is set to 0 in 256 consecutive channels, then the reception of a yellow alarm is declared. The alarm is considered cleared when the first channel with bit 2 set to a 1 is received.

193S S-BIT. If RCR2.4 = 0 and RCR2.3 = 1, then the DS2182A examines the S-bit position of frame 12 for the presence of a yellow alarm. The DS2182A declares the presence of a yellow alarm on the first occurrence of the S-bit in frame 12 being set to 1. The alarm is considered cleared when this S-bit returns to 0.

193E FDL. If RCR2.4 = 1, then the DS2182A examines the FDL for a repeating 00FF pattern. If this pattern is received in the FDL 16 consecutive times without error, then a yellow alarm is declared. The alarm is considered cleared as soon as any pattern other than 00FF is received.

RIMR1: RECEIVE INTERRUPT MASK REGISTER 1 Figure 9

(MSB)				(LSB)			
8ZD	16ZD	RCL	RYEL	RLOS	B8ZSD	RBL	COFA
SYMBOL	POSITION	NAME AND DESCRIPTION		POSITION	SYMBOL		
8ZD	RIMR1.7	8 Zero Detect Mask. 1 = interrupt enabled 0 = interrupt masked					
16ZD	RIMR1.6	16 Zero Detect Mask. 1 = interrupt enabled 0 = interrupt masked					
RCL	RIMR1.5	Receive Carrier Loss Mask. 1 = interrupt enabled 0 = interrupt masked					
RYEL	RIMR1.4	Receive Yellow Alarm Mask. 1 = interrupt enabled 0 = interrupt masked					
RLOS	RIMR1.3	Receive Loss Of Sync Mask. 1 = interrupt enabled 0 = interrupt masked					
B8ZSD	RIMR1.2	B8ZS Code Word Detect Mask. 1 = interrupt enabled 0 = interrupt masked					
RBL	RIMR1.1	Receive Blue Alarm Mask. 1 = interrupt enabled 0 = interrupt masked					
COFA	RIMR1.0	Change Of Frame Alignment Mask. 1 = interrupt enabled 0 = interrupt masked					

RSR2: RECEIVE STATUS REGISTER 2 Figure 10

(MSB)				(LSB)			
SEFE	RCLC	RBLC	FERR	FECS	OOFCS	CRCCS	BPVCS
SYMBOL	POSITION	NAME AND DESCRIPTION					
SEFE	RSR2.7	Severely Errored Framing Event. Set when 2 out of 6 framing bits (Ft or FPS) are received in error.					
RCLC	RSR2.6	Receive Carrier Loss Clear. Set when the carrier signal is restored; will remain set until read.					
RBLC	RSR2.5	Receive Blue Alarm Clear. Set when the Blue Alarm (AIS) is no longer detected; will remain set until read.					
FERR	RSR2.4	Frame Bit Error. Set when FT (193S) or FPS (193E) bit errors occur.					
FECS	RSR2.3	Frame Error Count Saturation. Set on the next frame error event after the 8-bit Frame Error Count Register (FECR) saturates at 255.					
OOFCS	RSR2.2	Out Of Frame Count Saturation. Set on the next OOF event after the 8-bit OOF Count Register (OOFER) saturates at 255.					
CRCCS	RSR2.1	CRC Count Saturation. Set on the next CRC error event after the 8-bit CRC Count Register (CRCCR) saturates at 255.					
BPVCS	RSR2.0	Bipolar Violation Count Saturation. Set on the next BPV error event after the 16-bit Bipolar Violation Count Register (BVCR) saturates at 65,535.					

RIMR2: RECEIVE INTERRUPT MASK REGISTER 2 Figure 11

(MSB)				(LSB)			
SEFE	RCLC	RBLC	FERR	FECS	OOFCS	CRCCS	BPVCS
SYMBOL	POSITION	NAME AND DESCRIPTION					
SEFE	RIMR2.7	Severely Errored Framing Event Mask. 0 = interrupt masked 1 = interrupt enabled					
RCLC	RIMR2.6	Receive Carrier Loss Clear Mask. 0 = interrupt masked 1 = interrupt enabled					
RBLC	RIMR2.5	Receive Blue Alarm Clear Mask. 0 = interrupt masked 1 = interrupt enabled					
FERR	RIMR2.4	Frame Bit Error Mask. 1 = interrupt enabled 0 = interrupt masked					
FECS	RIMR2.3	Frame Error Count Saturation Mask. 1 = interrupt enabled 0 = interrupt masked					
OOFCS	RIMR2.2	Out Of Frame Count Saturation Mask. 1 = interrupt enabled 0 = interrupt masked					

CRCOS RIMR2.1 **CRC Count Saturation Mask.**

- 1 = interrupt enabled
- 0 = interrupt masked

BPVCS RIMR2.0 **Bipolar Violation Count Saturation Mask.**

- 1 = interrupt enabled
- 0 = interrupt masked

RCR1: RECEIVE CONTROL REGISTER 1 Figure 12

(MSB)

(LSB)

ARC	OOF1	OOF2	ACR	SYNCC	SYNCT	SYNCE	RESYNC
-----	------	------	-----	-------	-------	-------	--------

SYMBOL POSITION

NAME AND DESCRIPTION

ARC RCR1.7

Auto Resync Criteria.

- 1 = resync on OOF event only
- 0 = resync on OOF event or Receive Carrier Loss (RCL)

OOF1 RCR1.6

Out Of Frame 1. OOF event description. Valid when RCR1.5 is cleared

- 1 = 2 out of 5 frame bits (FT or FPS) in error
- 0 = 2 out of 4 frame bits (FT or FPS) in error

OOF2 RCR1.5

Out Of Frame 2. OOF event description.

- 1 = 2 out of 6 frame bits (FT or FPS) in error
- 0 = follow OOF event described in RCR1.6

ACR RCR1.4

Auto Counter Reset. When set, all four of the counters will be reset to 0 when read.

SYNCC RCR1.3

Sync Criteria. Determines the type of algorithm utilized by the receive synchronizer; differs for each frame mode.

193S Framing (RCR2.4 = 0)

0 = synchronize to frame boundaries using FT pattern, then search for multiframe by using FS.

1 = cross couple FT and FS patterns in sync algorithm.

193E Framing (RCR2.4 = 1)

0 = normal sync (utilizes FPS only).

1 = validate new alignment with CRC before declaring sync.

SYNCT RCR1.2

Sync Time.

1 = validate 24 consecutive F-bits before declaring sync.

0 = validate 10 consecutive F-bits before declaring sync.

SYNCE RCR1.1

Sync Enable. If clear, the DS2182A automatically begins a resync if the conditions described in RCR1.7 are met. If set, no auto resync occurs.

RESYNC RCR1.0

Resync. When toggled low to high, the DS2182A initiates a resync immediately. The bit must be cleared and set again for subsequent resyncs.

SYNCHRONIZER

The heart of the monitor is the receive synchronizer. This circuit serves two purposes: 1) monitors the incoming data stream for loss of frame or multiframe alignment, and 2) searches for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR, which is

forced low during resync. When one and only one candidate is qualified, the output timing moves to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR1 allow tailoring of the resync algorithm by the user. These bits are described below.

SYNC CRITERIA (RCR1.3)

193E. Bit RCR1.3 determines which sync algorithm is utilized when resync is in progress (RLOS = 1). In 193E framing, when RCR1.3 = 0, the synchronizer will lock only to the FPS pattern and will move to the new frame and multiframe alignment after the framing candidate is qualified. RLOS will go low one frame after the move to the new alignment. When RCR1.3 = 1, the new alignment is further tested by a CRC6 code match. RLOS will transition low after a CRC6 match occurs. If no CRC6 match occurs in three attempts (three multiframes), the algorithm resets and a new search for the FPS pattern begins. It takes 9 ms for the synchronizer to check the first CRC6 code after the new FPS alignment has been loaded. Each additional CRC6 test takes 3 ms. Regardless of the state of RCR1.3, if more than one candidate exists after 24 ms, the synchronizer begins eliminating emulators by testing their CRC6 codes in order to find the true framing candidate.

193S. In 193S framing, when RCR1.3 = 1, the synchronizer cross-checks the FT pattern with the FS pattern to help eliminate false framing candidates such as digital milliwatts. The FS patterns are compared to the repeating pattern ...00111000111000...(00111x0 if RCR2.3 = 1). In this mode, FT and FS must be correctly identified

by the synchronizer before sync is declared. Clearing RCR1.3 causes the synchronizer to search for the FT pattern (101010...) without cross-coupling the FS pattern. Frame sync is established using the FT information, while multiframe sync is established only if valid FS information is present. If no valid FS pattern is identified, the synchronizer moves to the FT alignment, RLOS goes low, and a false multiframe position may be indicated by RMSYNC. RFER indicates when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode will be used in applications where non-standard S-bit patterns exist. In such applications, multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

SYNC TIME (RCR1.2)

Bit RCR1.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR1.2 = 1, the algorithm validates 24 bits; if RCR1.2 = 0, 10 bits are validated. Validating 24 bits results in superior false framing protection while 10-bit testing minimizes reframe time. In either case, the synchronizer only establishes resync when one and only one candidate is found (see Table 5).

AVERAGE REFRAME TIME Table 5

FRAME MODE	RCR1.2 = 0			RCR1.2 = 1		
	MIN.	AVG.	MAX.	MIN.	AVG.	MAX.
193S	3.0ms	3.75ms	4.5ms	6.5ms	7.25ms	8.0ms
193E	6.0ms	7.5ms	9.0ms	13.0ms	14.5ms	16.0ms

NOTE:

1. Average reframe time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

SYNC ENABLE (RCR1.1)

When RCR1.1 is cleared, the receiver initiates automatic resync if an OOF event occurs or if carrier loss (192 consecutive 0s) occurs (depends on RCR1.7). When RCR1.1 is set, the automatic resync circuitry is disabled. In this case, resync can only be initiated by setting RCR1.0 to 1 or externally transitioning RST from low to high. Note that using RST to initiate a resync resets the output timing while RST is low; use of RCR1.1

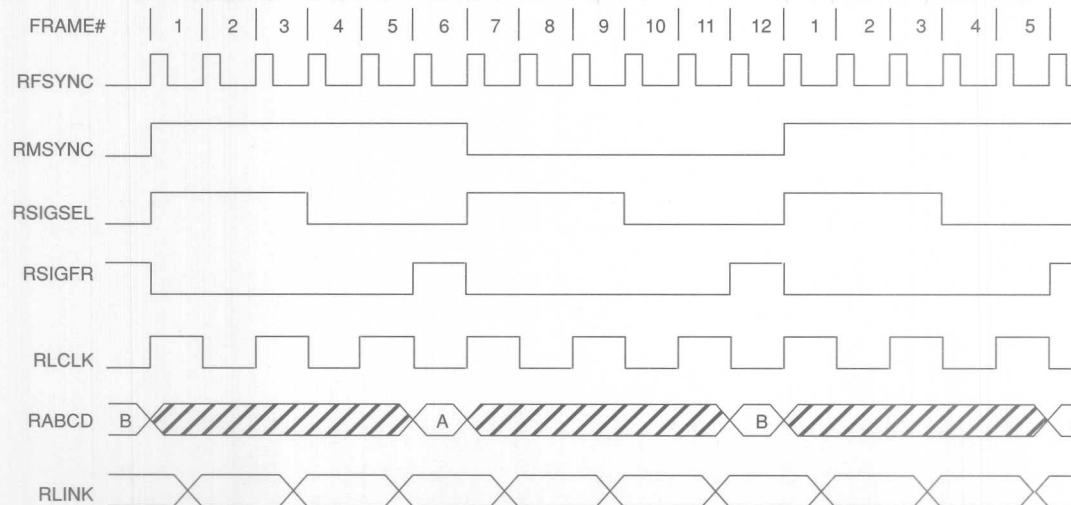
will not affect the output timing until the new alignment is located.

RESYNC (RCR1.0)

A 0-to-1 transition of RCR1.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

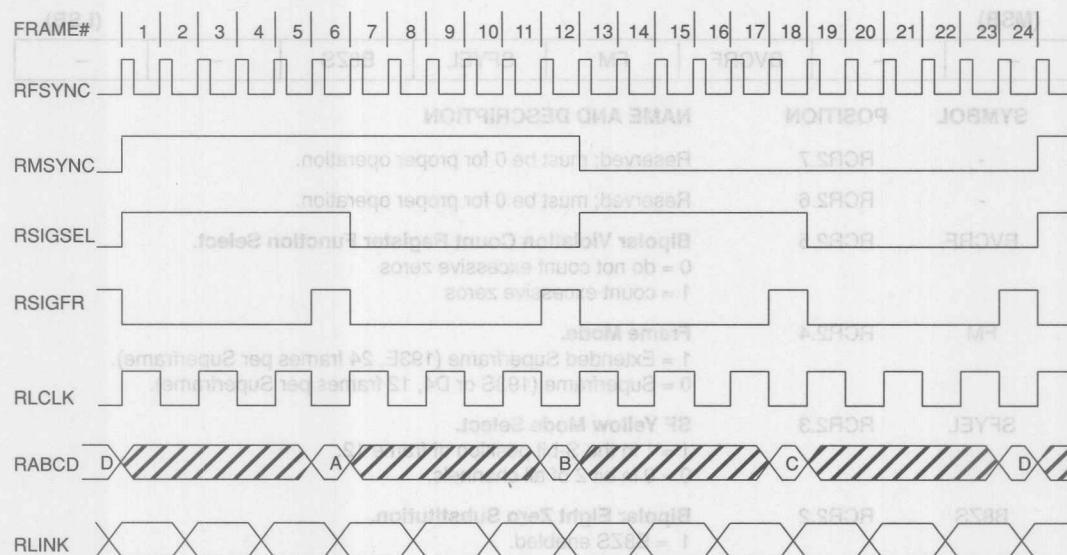
RCR2: RECEIVE CONTROL REGISTER 2 Figure 13

(MSB)							(LSB)
-	-	BVCRF	FM	SFYEL	B8ZS	-	-
SYMBOL	POSITION	NAME AND DESCRIPTION					
-	RCR2.7	Reserved; must be 0 for proper operation.					
-	RCR2.6	Reserved; must be 0 for proper operation.					
BVCRF	RCR2.5	Bipolar Violation Count Register Function Select. 0 = do not count excessive zeros 1 = count excessive zeros					
FM	RCR2.4	Frame Mode. 1 = Extended Superframe (193E, 24 frames per Superframe). 0 = Superframe (193S or D4, 12 frames per Superframe).					
SFYEL	RCR2.3	SF Yellow Mode Select. 1 = 1 in the S-bit position of frame 12. 0 = 0 in bit 2 of all channels.					
B8ZS	RCR2.2	Bipolar Eight Zero Substitution. 1 = B8ZS enabled. 0 = B8ZS disabled.					
-	RCR2.1	Reserved; must be 0 for proper operation.					
-	RCR2.0	Reserved; must be 0 for proper operation.					

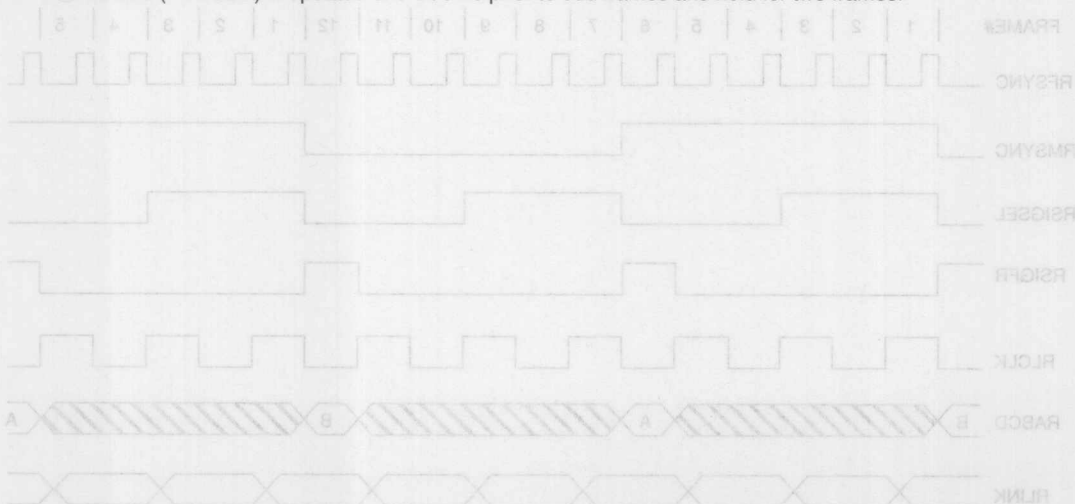
193S RECEIVE MULTIFRAME TIMING Figure 14**NOTES:**

1. Signaling data is updated during signaling frames on channel boundaries. Pin RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit-time prior to S-bit frames and held for two frames.

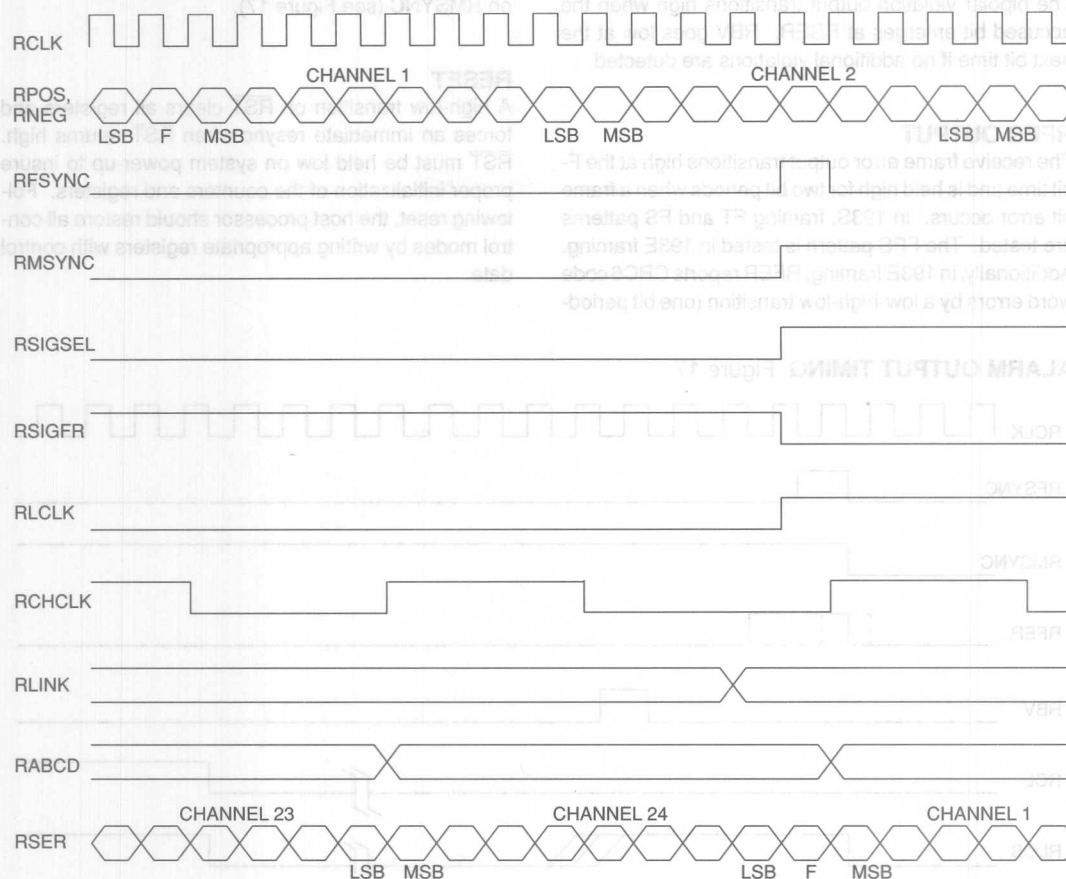
193E RECEIVE MULTIFRAME TIMING Figure 15

**NOTES:**

1. Signaling data is updated during signaling frames on channel boundaries. Pin RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL data) is updated one bit-time prior to odd frames and held for two frames.

**NOTES:**

1. Signaling data is updated during signaling frames on channel boundaries. Pin RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL data) is updated one bit-time prior to odd frames and held for two frames.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 16**NOTES:**

1. RLINK timing is shown for 193E; in 193S, RLINK is updated on even frame boundaries and is held across multiframe edges.
2. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.

ALARM OUTPUTS

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the onboard alarm logic.

RLOS OUTPUT

The receive loss of sync output indicates the status of the receiver synchronizer circuitry; when high, an off-line resynchronization is in progress and a high-low transition indicates that resync is complete. The RLOS

bit (RSR1.3) is a latched version of the RLOS output. If the auto-resync mode is selected (RCR1.1 = 0), RLOS is a real-time indication of a carrier loss or OOF event occurrence.

RYEL OUTPUT

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR1.4) is a latched version of the RYEL output.

RBV OUTPUT

The bipolar violation output transitions high when the accused bit emerges at RSER. RBV goes low at the next bit time if no additional violations are detected.

RFER OUTPUT

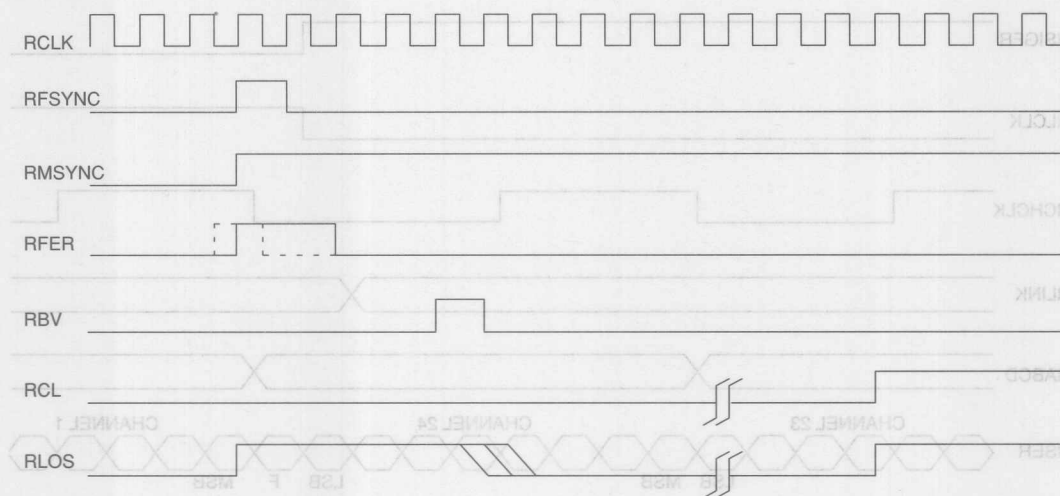
The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S, framing FT and FS patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports CRC6 code word errors by a low-high-low transition (one bit period-

wide) one-half RCLK period before a low-high transition on RMSYNC (see Figure 17).

RESET

A high-low transition on $\overline{\text{RST}}$ clears all registers and forces an immediate resync when $\overline{\text{RST}}$ returns high. $\overline{\text{RST}}$ must be held low on system power-up to insure proper initialization of the counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

ALARM OUTPUT TIMING Figure 17



NOTES:

1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if RCR2.3 = 1.) Also, in 193E, RFER transitions high 1/2 bit-time before rising edge of RMSYNC to indicate a CRC6 error for the previous multiframe.
2. RBV indicates received bipolar violation and transitions high when accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high when 192 consecutive bits are 0; RCL transitions low upon reception of 12.5% ones density.
4. RLOS transitions high during F-bit time that caused an OOF event if auto-resync is enabled (RCR1.1 = 0). Resync also occurs when loss of carrier is detected (RCL = 1) if RCR1.7 = 0. When RCR1.1 = 1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR1.0 transitions low-to-high or the $\overline{\text{RST}}$ pin transitions high-low-high.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

-1.0V to 7.0V

0°C to +70°C

-55°C to 125°C

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		3		mA	1,2
Input Leakage	I_{IL}	-1.0		+1.0	μA	3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	5
Output Leakage	I_{LO}	-1.0		+1.0	μA	6

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. RCLK = 1.544 MHz.
2. Outputs open.
3. $0V < V_{IN} < V_{DD}$.
4. All outputs except \overline{INT} which is open collector.
5. All outputs.
6. Applies to SDO when tri-stated.

CHARACTERISTICS^{1,2} SERIAL PORT(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t_{DC}	50			ns	
SCLK to SDI Hold	t_{CDH}	50			ns	
SDI to SCLK Falling Edge	t_{CD}	50			ns	
SCLK Low Time	t_{CL}	250			ns	
SCLK High Time	t_{CH}	250			ns	
SCLK Rise and Fall Times	t_R, t_F			100	ns	
\overline{CS} to SCLK Setup	t_{CC}	50			ns	
SCLK to \overline{CS} hold	t_{CCH}	50			ns	
\overline{CS} Inactive Time	t_{CWH}	2.5			μs	
SCLK to SDO Valid	t_{CDV}			200	ns	
\overline{CS} to SDO High Z	t_{CDZ}			75	ns	

NOTES:

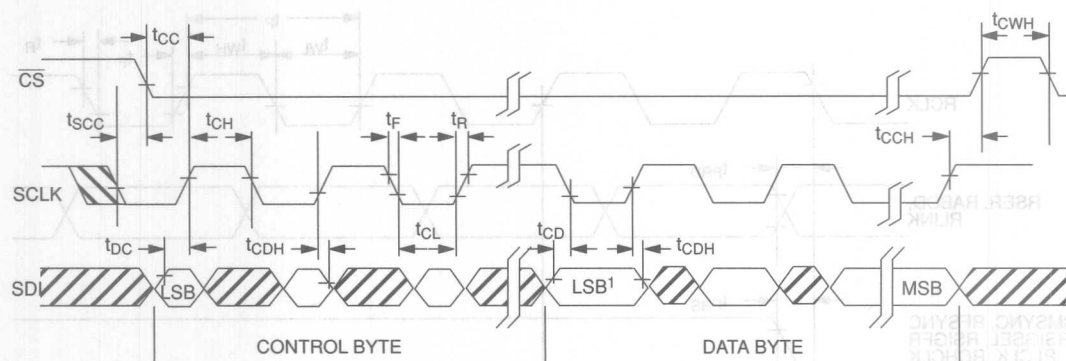
1. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8$ and 10ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

AC ELECTRICAL CHARACTERISTICS^{1,2} RECEIVE(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

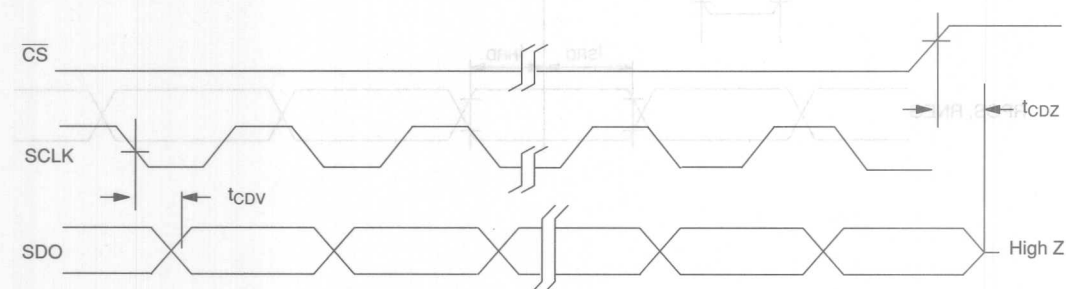
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay RCLK to RMSYNC, RFSYNC, RSISEL, RSIGFR, RLCLK, RCHCLK	t_{PRS}			75	ns	
Propagation Delay RCLK to RSER, RABCD, RLINK	t_{PRD}			75	ns	
Transition Time All Outputs	t_{TTR}			20	ns	
RCLK Period	t_P		648		ns	
RCLK Pulse Width	t_{WL}, t_{WH}		324		ns	
RCLK Rise and Fall Times	t_R, t_F		20		ns	
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50			ns	
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns	
Propagation Delay RCLK to RLOS, RYEL, RBV, RCL, RFER	t_{PRA}			75	ns	
Minimum \overline{RST} Pulse Width	t_{RST}	1			μs	

NOTES:

1. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8$ and 10ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

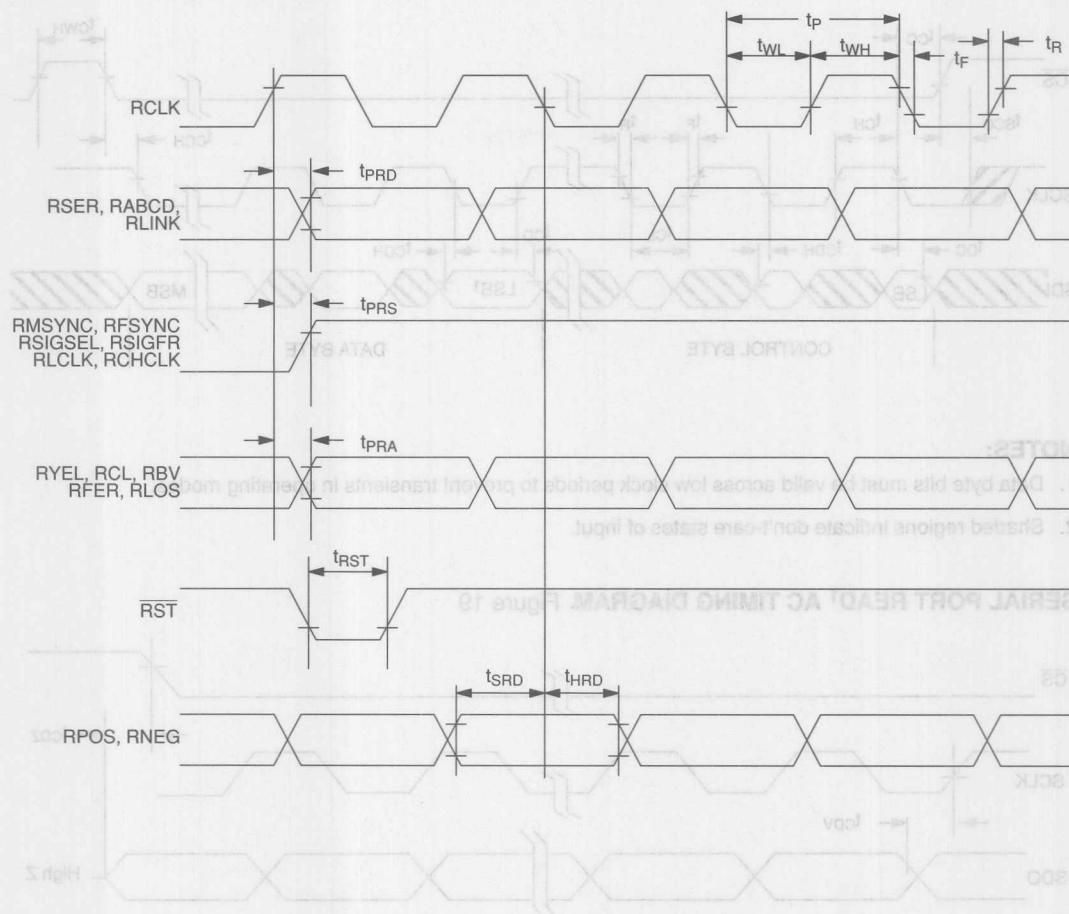
SERIAL PORT WRITE AC TIMING DIAGRAM Figure 18**NOTES:**

1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.
2. Shaded regions indicate don't-care states of input.

SERIAL PORT READ¹ AC TIMING DIAGRAM Figure 19**NOTE:**

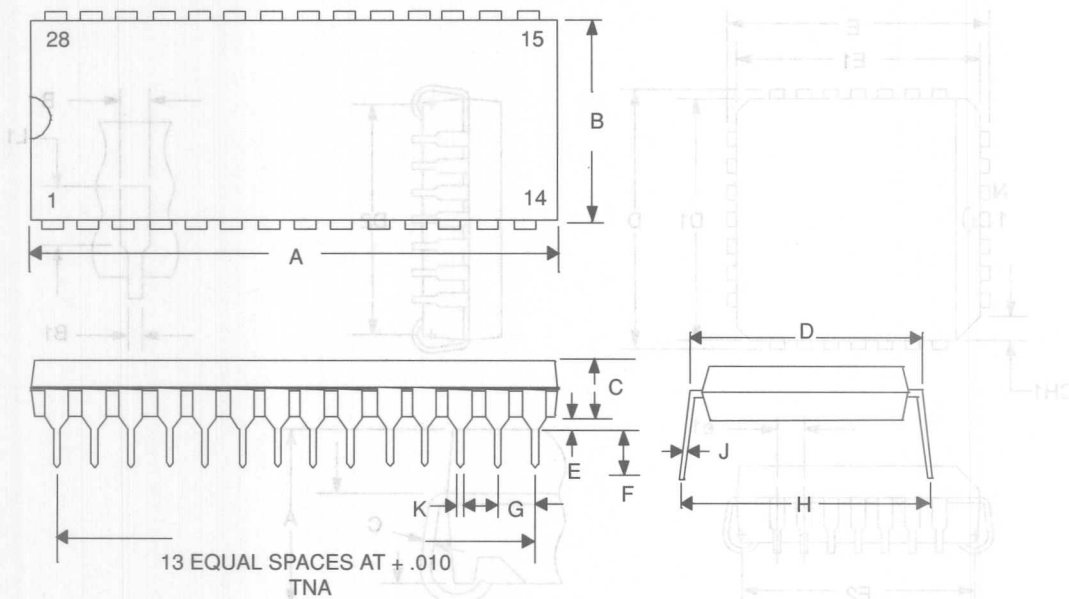
1. Serial port write must precede a port read to provide address information.

RECEIVE AC TIMING DIAGRAM Figure 20



DS2182A T1 LINE MONITOR 28-PIN DIP

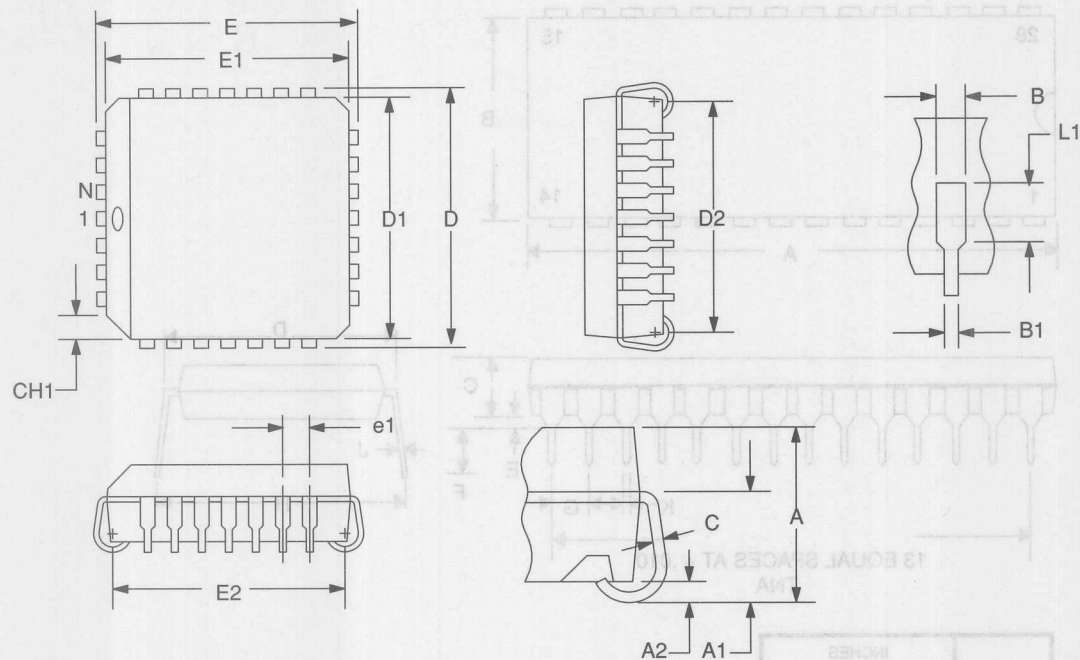
DS2182A T1 LINE MONITOR 28-PIN PLCC



DIM	INCHES	
	MIN	MAX
A	1.445	1.470
B	0.530	0.550
C	0.140	0.160
D	0.600	0.625
E	0.015	0.040
F	0.120	0.145
G	0.090	0.110
H	0.600	0.680
J	0.008	0.012
K	0.015	0.022

INCHES		
MAX	MIN	DIM
0.617	0.617	A
0.517	0.500	TA
	0.030	SA
0.030	0.030	B
0.500	0.500	18
0.100	0.090	C
0.600	0.600	D
0.030	0.030	10
0.030	0.030	DS
0.030	0.030	E
0.030	0.030	13
0.030	0.030	15
	0.030	11
	0.030	14
0.030	0.030	16
0.030	0.030	17

DS2182AQ T1 LINE MONITOR 28-PIN PLCC



DS21510

T1 Single-Chip Transceiver

T1/CEPT (E1) COMBINATION LINE INTERFACE/FRAMER PRODUCTS

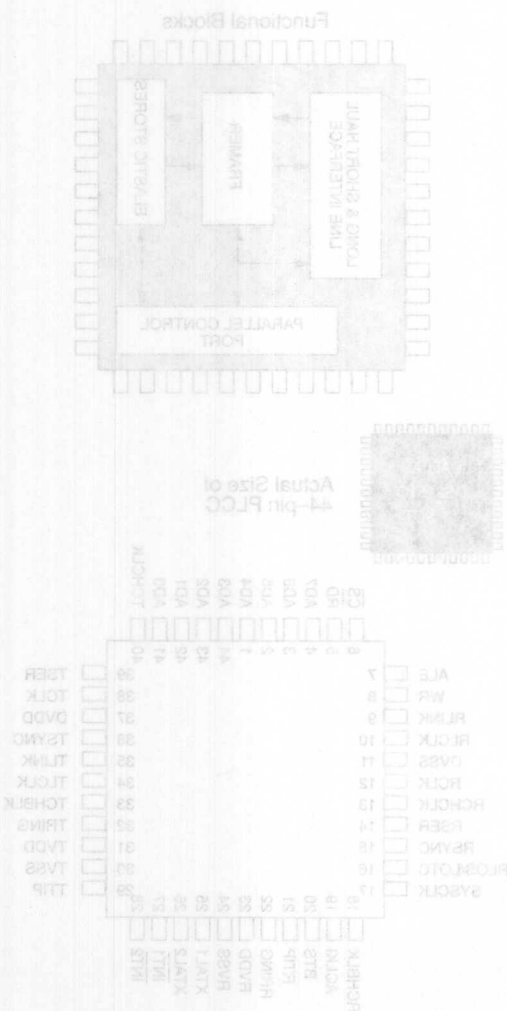
FEATURES

- Complete DS21510-PRI transceiver functionality
- Line interface can handle both long and short haul trunks
- 32-bit or 128-bit jitter attenuator
- Generates DSX-1 and CSU line build outs
- Frames to D4, ESF, and SLC-66b formats
- Dual onboard two-frame elastic store slip buffers that connect to backplanes up to 8.192 MHz
- 8-bit parallel control port that can be used on either multiplexed or non-multiplexed buses
- Extracts and inserts robbed bit signaling
- Detects and generates yellow and blue alarms
- Programmable output blocks for Functional T1
- Fully independent transmit and receive functionality
- Onboard FDL support circuitry
- Generates and detects CSU loop codes
- Contains ANSI one's density monitor and enforcer
- Large path and line error counters including BPV, CV, CRC8, and framing bit errors
- Pin compatible with DS21510 E1 Single-Chip Transceiver
- 5V supply, low power CMOS

DESCRIPTION

The DS21510 T1 Single-Chip Transceiver (SCT) contains all of the necessary functions for connection to T1 lines, whether they be DS-1 long haul or DSX-1 short haul. The clock recovery circuitry automatically adjusts

PIN ASSIGNMENT



to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX-1 line build outs as well as CSU build outs at -7.5 dB, -15 dB, and -22.5 dB. The onboard jitter attenuator (selectable to either

DALLAS

SEMICONDUCTOR

DS2151Q

T1 Single-Chip Transceiver

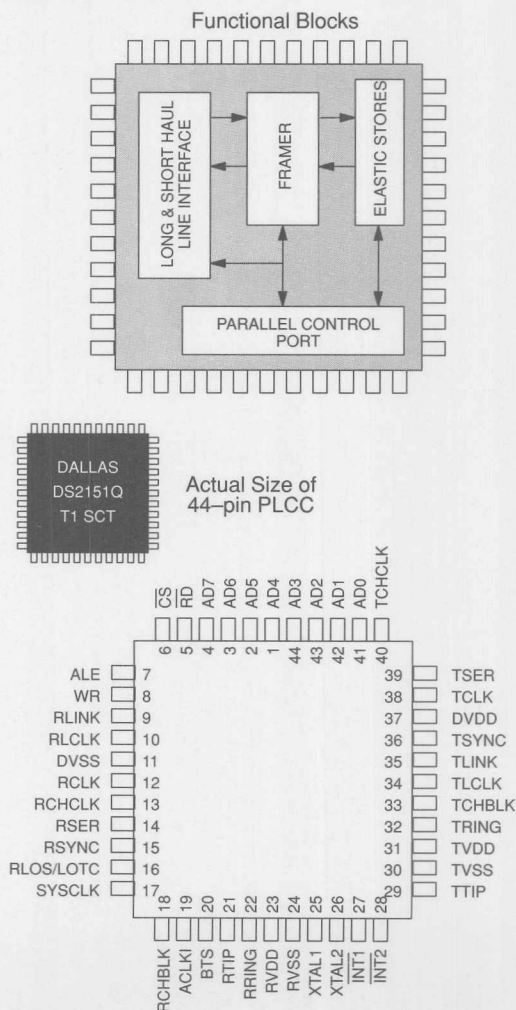
FEATURES

- Complete DS1/ISDN-PRI transceiver functionality
- Line interface can handle both long and short haul trunks
- 32-bit or 128-bit jitter attenuator
- Generates DSX-1 and CSU line build outs
- Frames to D4, ESF, and SLC-96^R formats
- Dual onboard two-frame elastic store slip buffers that connect to backplanes up to 8.192 MHz
- 8-bit parallel control port that can be used on either multiplexed or non-multiplexed buses
- Extracts and inserts robbed bit signaling
- Detects and generates yellow and blue alarms
- Programmable output clocks for Fractional T1
- Fully independent transmit and receive functionality
- Onboard FDL support circuitry
- Generates and detects CSU loop codes
- Contains ANSI one's density monitor and enforcer
- Large path and line error counters including BPV, CV, CRC6, and framing bit errors
- Pin compatible with DS2153Q E1 Single-Chip Transceiver
- 5V supply; low power CMOS

DESCRIPTION

The DS2151Q T1 Single-Chip Transceiver (SCT) contains all of the necessary functions for connection to T1 lines whether they be DS-1 long haul or DSX-1 short haul. The clock recovery circuitry automatically adjusts

PIN ASSIGNMENT



to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX-1 line build outs as well as CSU build outs of -7.5 dB, -15 dB, and -22.5 dB. The onboard jitter attenuator (selectable to either

32-bits or 128-bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting robbed-bit signaling data and FDL data. The device contains a set of 64 eight-bit internal registers which the user can access and control the operation of the unit. Quick access via the parallel control port allows a single micro to handle many T1 lines. The device fully meets all of the latest T1 specifications including ANSI T1.403-199X, AT&T TR 62411 (12-90), and ITUG.703, G.704, G.706, G.823, and I.431.

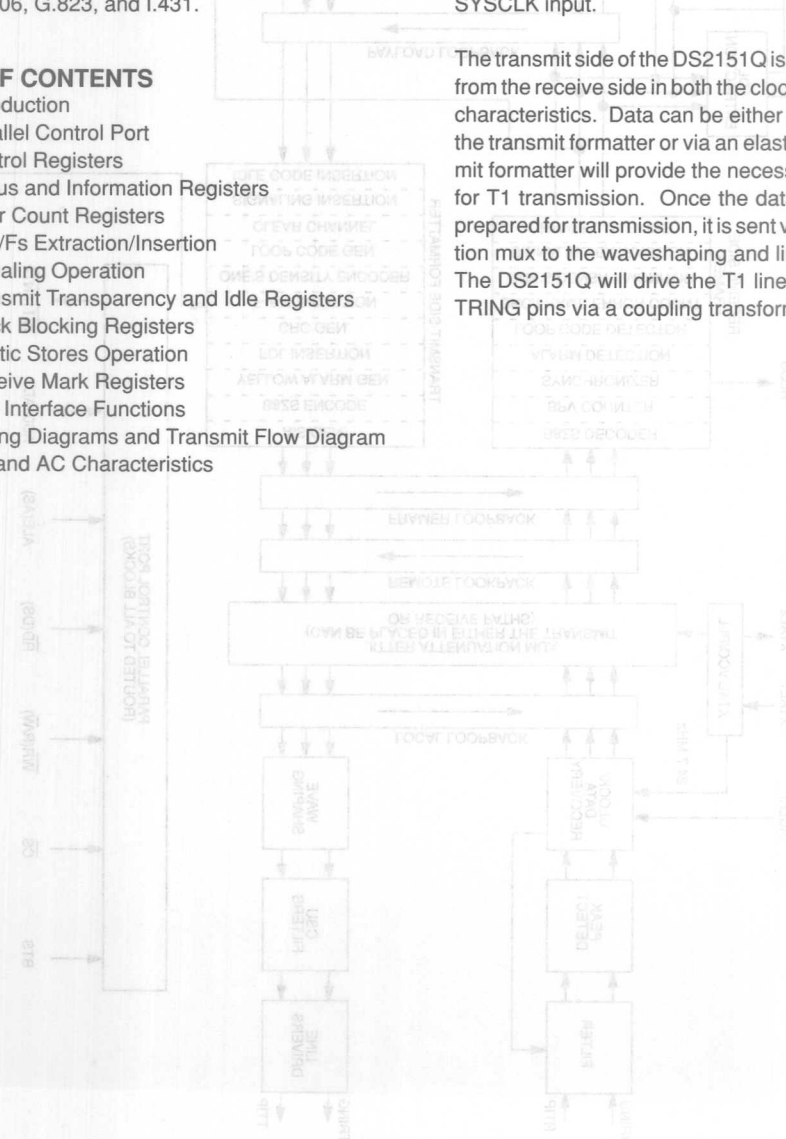
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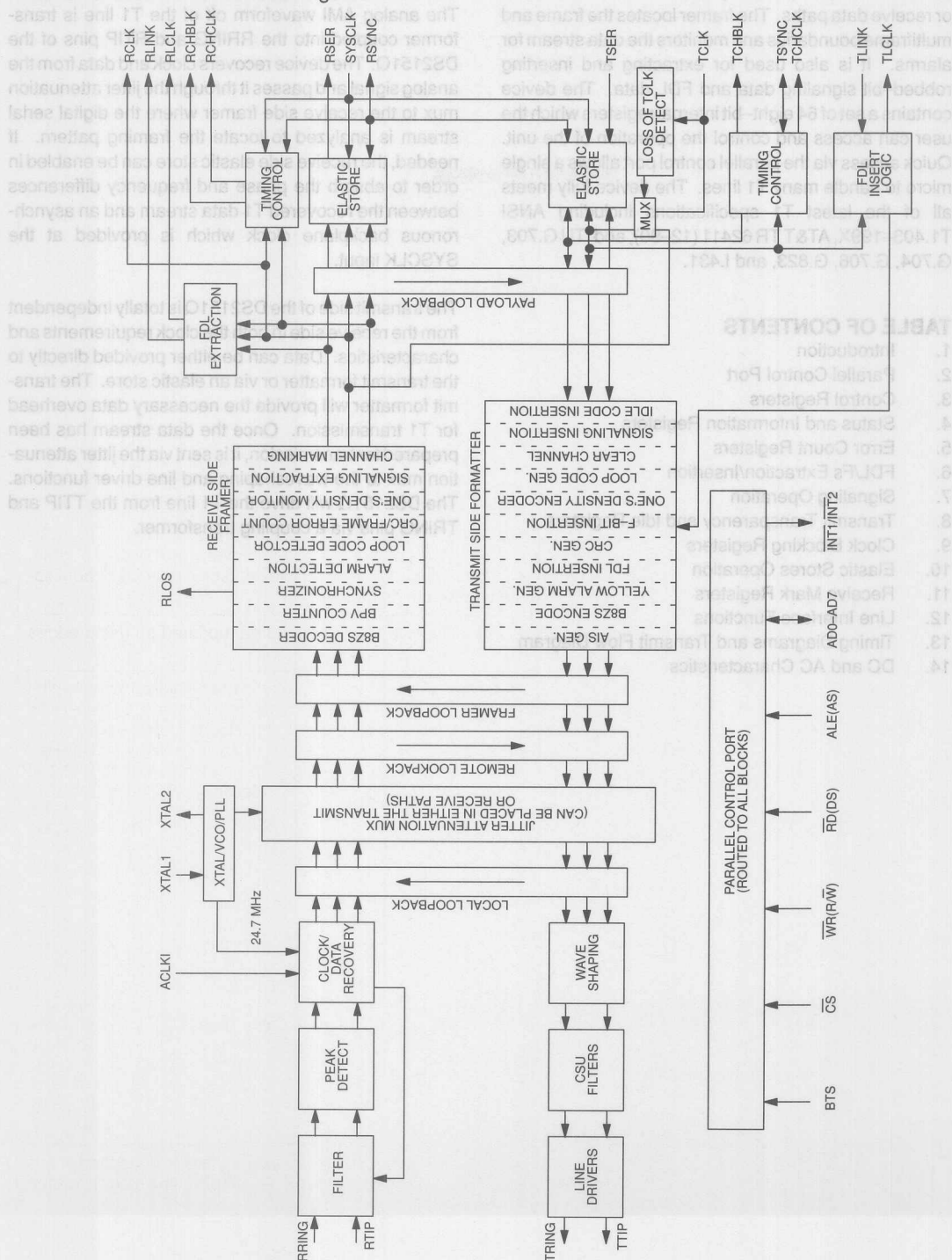
1.0 INTRODUCTION

The analog AMI waveform off of the T1 line is transformer coupled into the RRING and RTIP pins of the DS2151Q. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing pattern. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input.

The transmit side of the DS2151Q is totally independent from the receive side in both the clock requirements and characteristics. Data can be either provided directly to the transmit formatter or via an elastic store. The transmit formatter will provide the necessary data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2151Q will drive the T1 line from the TTIP and TRING pins via a coupling transformer.



DS2151Q BLOCK DIAGRAM Figure 1-1



PIN DESCRIPTION Table 1–1

PIN	SYMBOL	TYPE	DESCRIPTION
1 2 3 4	AD4 AD5 AD6 AD7	I/O	Address/Data Bus. A 8-bit multiplexed address/data bus.
5	RD(DS)	I	Read Input (Data Strobe).
6	CS	I	Chip Select. Must be low to read or write the port.
7	ALE(AS)	I	Address Latch Enable (Address Strobe). A positive going edge serves to demultiplex the bus.
8	WR(R/W)	I	Write Input (Read/Write).
9	RLINK	O	Receive Link Data. Updated with either FDL data (ESF) or Fs bits (D4) or Z-bits (ZBTSI) one RCLK before the start of a frame. See Section 13 for timing details.
10	RLCLK	O	Receive Link Clock. 4 KHz or 2 KHz (ZBTSI) demand clock for the RLINK output. See Section 13 for timing details.
11	DVSS	–	Digital Signal Ground. 0.0 volts. Should be tied to local ground plane.
12	RCLK	O	Receive Clock. Recovered 1.544 MHz clock.
13	RCHCLK	O	Receive Channel Clock. 192 KHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 13 for timing details.
14	RSER	O	Receive Serial Data. Received NRZ serial data, updated on rising edges of RCLK or SYSCLK.
15	RSYNC	I/O	Receive Sync. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4=0) or multiframe boundaries (RCR2.4=1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the elastic store is enabled via the CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame boundary pulse is applied. See Section 13 for timing details.
16	RLOS/LOTCL	O	Receive Loss of Sync/Loss of Transmit Clock. A dual function output. If CCR3.5=0, will toggle high when the synchronizer is searching for the T1 frame and multiframe; if CCR3.5=1, will toggle high if the TCLK pin has not toggled for 5 μ s.
17	SYSCLK	I	System Clock. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store functions are enabled via either CCR1.7 or CCR1.2. Should be tied low in applications that do not use the elastic store. If tied high for more than 100 μ s, will force all output pins (including the parallel port) to 3-state.
18	RCHBLK	O	Receive Channel Block. A user programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384Kbps service, 768Kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 13 for timing details.
19	ACLKI	I	Alternate Clock Input. Upon a receive carrier loss, the clock applied at this pin (normally 1.544 MHz) will be routed to the RCLK pin. If no clock is routed to this pin, then it should be tied to DVSS.

PIN	SYMBOL	TYPE	DESCRIPTION
20	BTS	I	Bus Type Select. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD(DS), ALE(AS), and WR(R/W) pins. If BTS=1, then these pins assume the function listed in parenthesis ().
21 22	RTIP RRING	—	Receive Tip and Ring. Analog inputs for clock recovery circuitry; connects to a 1:1 transformer (see Section 12 for details).
23	RVDD	—	Receive Analog Positive Supply. 5.0 volts. Should be tied to DVDD and TVDD pins.
24	RVSS	—	Receive Signal Ground. 0.0 volts. Should be tied to local ground plane
25 26	XTAL1 XTAL2	—	Crystal Connections. A pullable 6.176 MHz crystal must be applied to these pins. See Section 12 for crystal specifications.
27	INT1	O	Receive Alarm Interrupt 1. Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
28	INT2	O	Receive Alarm Interrupt 2. Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
29	TTIP	—	Transmit Tip. Analog line driver output; connects to a step-up transformer (see Section 12 for details).
30	TVSS	—	Transmit Signal Ground. 0.0 volts. Should be tied to local ground plane.
31	TVDD	—	Transmit Analog Positive Supply. 5.0 volts. Should be tied to DVDD and RVDD pins.
32	TRING	—	Transmit Ring. Analog line driver outputs; connects to a step-up transformer (see Section 12 for details).
33	TCHBLK	O	Transmit Channel Block. A user programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384Kbps service, 768Kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 13 for timing details.
34	TLCLK	O	Transmit Link Clock. 4 KHz or 2 KHz (ZBTSI) demand clock for the TLINK input. See Section 13 for timing details.
35	TLINK	I	Transmit Link Data. If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 13 for timing details.
36	TSYNC	I/O	Transmit Sync. A pulse at this pin will establish either frame or multiframe boundaries for the DS2151Q. Via TCR2.2, the DS2151Q can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 13 for timing details.
37	DVDD	—	Digital Positive Supply. 5.0 volts. Should be tied to RVDD and TVDD pins.
38	TCLK	I	Transmit Clock. 1.544 MHz primary clock.
39	TSER	I	Transmit Serial Data. Transmit NRZ serial data, sampled on the falling edge of TCLK.

PIN	SYMBOL	TYPE	DESCRIPTION
40	TCHCLK	O	Transmit Channel Clock. 192 KHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 13 for timing details.
41	AD0	I/O	Address/Data Bus. A 8-bit multiplexed address/data bus.
42	AD1		
43	AD2		
44	AD3		

DS2151Q REGISTER MAP

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
20	R/W	Status Register 1.	30	R/W	Common Control Register 3.
21	R/W	Status Register 2.	31	R/W	Receive Information Register 2.
22	R/W	Receive Information Register 1.	32	R/W	Transmit Channel Blocking Register 1.
23	R	Line code Violation Count Register 1.	33	R/W	Transmit Channel Blocking Register 2.
24	R	Line code Violation Count Register 2.	34	R/W	Transmit Channel Blocking Register 3.
25	R	Path Code Violation Count Register 1. (1)	35	R/W	Transmit Control Register 1.
26	R	Path Code Violation Count Register 2.	36	R/W	Transmit Control Register 2.
27	R	Multiframe Out of Sync Count Register 2.	37	R/W	Common Control Register 1.
28	R	Receive FDL Register	38	R/W	Common Control Register 2.
29	R/W	Receive FDL Match Register 1.	39	R/W	Transmit Transparency Register 1.
2A	R/W	Receive FDL Match Register 2.	3A	R/W	Transmit Transparency Register 2.
2B	R/W	Receive Control Register 1.	3B	R/W	Transmit Transparency Register 3.
2C	R/W	Receive Control Register 2.	3C	R/W	Transmit Idle Register 1.
2D	R/W	Receive Mark Register 1.	3D	R/W	Transmit Idle Register 2.
2E	R/W	Receive Mark Register 2.	3E	R/W	Transmit Idle Register 3.
2F	R/W	Receive Mark Register 3.	3F	R/W	Transmit Idle Definition Register.
60	R	Receive Signaling Register 1.	70	R/W	Transmit Signaling Register 1.
61	R	Receive Signaling Register 2.	71	R/W	Transmit Signaling Register 2.
62	R	Receive Signaling Register 3.	72	R/W	Transmit Signaling Register 3.

63	R	Receive Signaling Register 4.	73	R/W	Transmit Signaling Register 4.
64	R	Receive Signaling Register 5.	74	R/W	Transmit Signaling Register 5.
65	R	Receive Signaling Register 6.	75	R/W	Transmit Signaling Register 6.
66	R	Receive Signaling Register 7.	76	R/W	Transmit Signaling Register 7.
67	R	Receive Signaling Register 8.	77	R/W	Transmit Signaling Register 8.
68	R	Receive Signaling Register 9.	78	R/W	Transmit Signaling Register 9.
69	R	Receive Signaling Register 10.	79	R/W	Transmit Signaling Register 10.
6A	R	Receive Signaling Register 11.	7A	R/W	Transmit Signaling Register 11.
6B	R	Receive Signaling Register 12.	7B	R/W	Transmit Signaling Register 12.
6C	R/W	Receive Channel Blocking Register 1.	7C	R/W	Line Interface Control Register.
6D	R/W	Receive Channel Blocking Register 2.	7D	R/W	Test Register. (2)
6E	R/W	Receive Channel Blocking Register 3.	7E	R/W	Transmit FDL Register.
6F	R/W	Interrupt Mask Register 2.	7F	R/W	Interrupt Mask Register 1.

NOTES:

1. Address 25 also contains Multiframe Out of Sync Count Register 1.
2. The Test Register is used only by the factory; this register must be cleared (set to all zeros) on power-up initialization to insure proper operation.

2.0 PARALLEL PORT

The DS2151Q is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2151Q can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics for more details. The multiplexed bus on the DS2151Q saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the DS2151Q latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or \overline{WR} pulses. In a read cycle, the DS2151Q outputs a byte of data during the latter portion of the DS or \overline{RD} pulses. The read cycle is

terminated and the bus returns to a high impedance state as \overline{RD} transitions high in Intel timing or as DS transitions low in Motorola timing. The DS2151Q can also be easily connected to non-multiplexed buses. Please see the separate Application Note for a detailed discussion of this topic.

3.0 CONTROL REGISTERS

The operation of the DS2151Q is configured via a set of eight registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2151Q has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), a Line Interface Control Register (LICR), and three Common Control Registers (CCR1, CCR2, and CCR3). Seven of the eight registers are described below. The LICR is described in Section 12.

(MSB)								(LSB)	
LCVCRF	ARC	OOF1	OOF2	SYNCC	SYNCT	SYNCE	RESYNC		
SYMBOL	POSITION	NAME AND DESCRIPTION							
LCVCRF	RCR1.7	Line Code Violation Count Register Function Select. 0=do not count excessive zeros 1=count excessive zeros							
ARC	RCR1.6	Auto Resync Criteria. 0=Resync on OOF or RCL event 1=Resync on OOF only							
OOF1	RCR1.5	Out Of Frame Select 1. 0=2/4 frame bits in error 1=2/5 frame bits in error							
OOF2	RCR1.4	Out Of Frame Select 2. 0=follow RCR1.5 1=2/6 frame bits in error							
SYNCC	RCR1.3	Sync Criteria. In D4 Framing Mode. 0=search for Ft pattern, then search for Fs pattern 1=cross couple Ft and Fs pattern In ESF Framing Mode 0=search for FPS pattern only 1=search for FPS and verify with CRC6							
SYNCT	RCR1.2	Sync Time. 0=qualify 10 bits 1=qualify 24 bits							
SYNCE	RCR1.1	Sync Enable. 0=auto resync enabled 1=auto resync disabled							
RESYNC	RCR1.0	Resync. When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.							

RCR2: RECEIVE CONTROL REGISTER 2 (Address=2C Hex)

(MSB)				(LSB)			
RCS	RZBTSI	RSDW	RSM	RSIO	RD4YM	FSBE	MOSCRF
SYMBOL	POSITION	NAME AND DESCRIPTION					
RCS	RCR2.7	Receive Code Select. 0=idle code (7F Hex) 1=digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex)					
RZBTSI	RCR2.6	Receive Side ZBTSI Enable. 0=ZBTSI disabled 1=ZBTSI enabled					

RSDW	RCR2.5	RSYNC Double-Wide. 0=do not pulse double-wide in signaling frames 1=do pulse double-wide in signaling frames (note: this bit must be set to zero when RCR2.4=1 or when RCR2.3=1)
RSM	RCR2.4	RSYNC Mode Select. 0=frame mode (see the timing in Section 13) 1=multiframe mode (see the timing in Section 13)
RSIO	RCR2.3	RSYNC I/O Select. 0=RSYNC is an output 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to zero when CCR1.2=0)
RD4YM	RCR2.2	Receive Side D4 Yellow Alarm Select. 0=zeros in bit 2 of all channels 1=a one in the S-bit position of frame 12
FSBE	RCR2.1	PCVCR Fs Bit Error Report Enable. 0=do not report bit errors in Fs bit position; only Ft bit position 1=report bit errors in Fs bit position as well as Ft bit position
MOSCRF	RCR2.0	Multiframe Out of Sync Count Register Function Select. 0=count errors in the framing bit position 1=count the number of multiframe out of sync

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=35 Hex)

(MSB)				(LSB)			
LOTMC	TFPT	TCPT	RBSE	GB7S	TLINK	TBL	TYEL
SYMBOL	POSITION	NAME AND DESCRIPTION					
LOTMC	TCR1.7	Loss Of Transmit Clock Mux Control. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK input should fail to transition (see Figure 1–1 for more details). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops					
TFPT	TCR1.6	Transmit Framing Pass Through. (see note below) 0=Ft or FPS bits sourced internally 1=Ft or FPS bits sampled at TSER during F-bit time					
TCPT	TCR1.5	Transmit CRC Pass Through. (see note below) 0=source CRC6 bits internally 1=CRC6 bits sampled at TSER during F-bit time					
RBSE	TCR1.4	Robbed Bit Signaling Enable. (see note below) 0=no signaling is inserted in any channel 1=signaling is inserted in all channels (the TTR registers can be used to block insertion on a channel by channel basis)					
GB7S	TCR1.3	Global Bit 7 Stuffing. (see note below) 0=allow the TTR registers to determine which channels containing all zeros are to be Bit 7 stuffed 1=force Bit 7 stuffing in all zero byte channels regardless of how the TTR registers are programmed					

TLINK	TCR1.2	TLINK Select. (see note below) 0=source FDL or Fs bits from TFDL register 1=source FDL or Fs bits from the TLINK pin
TBL	TCR1.1	Transmit Blue Alarm. (see note below) 0=transmit data normally 1=transmit an unframed all one's code at TPOS and TNEG
TYEL	TCR1.0	Transmit Yellow Alarm. (see note below) 0=do not transmit yellow alarm 1=transmit yellow alarm

Note: for a detailed description of how the bits in TCR1 affect the transmit side formatter of the DS2151Q, please see Figure 13–9.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=36 Hex)

(MSB)		(LSB)					
TEST1	TEST0	TZBTSI	TSDW	TSM	TSIO	TD4YM	B7ZS
SYMBOL	POSITION	NAME AND DESCRIPTION					
TEST1	TCR2.7	Test Mode Bit 1 for Output Pins. See Table 3–1.					
TEST0	TCR2.6	Test Mode Bit 0 for Output Pins. See Table 3–1.					
TZBTSI	TCR2.5	Transmit Side ZBTSI Enable. 0=ZBTSI disabled 1=ZBTSI enabled					
TSDW	TCR2.4	TSYNC Double–Wide. (note: this bit must be set to zero when TCR2.3=1 or when TCR2.2=0) 0=do not pulse double–wide in signaling frames 1=do pulse double–wide in signaling frames					
TSM	TCR2.3	TSYNC Mode Select. 0=frame mode (see the timing in Section 13) 1=multiframe mode (see the timing in Section 13)					
TSIO	TCR2.2	TSYNC I/O Select. 0=TSYNC is an input 1=TSYNC is an output					
TD4YM	TCR2.1	Transmit Side D4 Yellow Alarm Select. 0=zeros in bit 2 of all channels 1=a one in the S–bit position of frame 12					
B7ZS	TCR2.0	Bit 7 Zero Suppression Enable. 0=no stuffing occurs 1=Bit 7 force to a one in channels with all zeros					

OUTPUT PIN TEST MODES Table 3–1

TEST1	TEST0	EFFECT ON OUTPUT PINS
0	0	operate normally
0	1	force all output pins 3–state (including all I/O pins and parallel port pins)
1	0	force all output pins low (including all I/O pins except parallel port pins)
1	1	force all output pins high (including all I/O pins except parallel port pins)

CCR1: COMMON CONTROL REGISTER 1 (Address=37 Hex)

(MSB)				(LSB)			
TESE	LLB	RSAO	RLB	SCLKM	RESE	PLB	FLB
SYMBOL	POSITION	NAME AND DESCRIPTION					
TESE	CCR1.7	Transmit Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled					
LLB	CCR1.6	Local Loopback. 0=loopback disabled 1=loopback enabled					
RSAO	CCR1.5	Receive Signaling All One's. 0=allow robbed signaling bits to appear at RSER 1=force all robbed signaling bits at RSER to one					
RLB	CCR1.4	Remote Loopback. 0=loopback disabled 1=loopback enabled					
SCLKM	CCR1.3	SYSClk Mode Select. 0=if SYSClk is 1.544 MHz 1=if SYSClk is 2.048 MHz					
RESE	CCR1.2	Receive Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled					
PLB	CCR1.1	Payload Loopback. 0=loopback disabled 1=loopback enabled					
FLB	CCR1.0	Framer Loopback. 0=loopback disabled 1=loopback enabled					

LOCAL LOOPBACK

When CCR1.6 is set to a one, the DS2151Q will be forced into Local LoopBack (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the SCT. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator and the jitter attenuator should be programmed to be in the transmit path. LLB is primarily used in debug and test applications. Please see the DS2151Q Block Diagram in Section 1 for more details.

REMOTE LOOPBACK

When CCR1.4 is set to a one, the DS2151Q will be forced into Remote LoopBack (RLB). In this loopback, data recovered off the T1 line from the RTIP and RRING pins will transmitted back onto the T1 line (with any BPVs that might have occurred intact) via the TTIP and

TRING pins. Data will continue to pass through the receive side of the DS2151Q as it would normally and the data at the TSER input will be ignored. Data in this loopback will pass through the jitter attenuator. RLB is used to place the DS2151Q into "line" loopback which is a requirement of both ANSI T1.403 and AT&T TR62411. Please see the DS2151Q Block Diagram in Section 1 for more details.

PAYLOAD LOOPBACK

When CCR1.1 is set to a one, the DS2151Q will be forced into Payload LoopBack (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS2151Q will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the

DS2151Q. When PLB is enabled, the following will occur:

1. data will be transmitted from the TTIP and TRING pins synchronous with RCLK instead of TCLK
2. all of the receive side signals will continue to operate normally
3. the TCHCLK and TCHBLK signals are forced low
4. data at the TSER pin is ignored
5. the TLCLK signal will become synchronous with RCLK instead of TCLK.

in testing and debugging applications. In FLB, the DS2151Q will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. unless the RLB is active, an unframed all one's code will be transmitted at TTIP and TRING
2. data off the T1 line at RTIP and RRING will be ignored
3. the RCLK output will be replaced with the TCLK input.

FRAMER LOOPBACK

When CCR1.0 is set to a one, the DS2151Q will enter a Framers LoopBack (FLB) mode. This loopback is useful

CCR2: COMMON CONTROL REGISTER 2 (Address=38 Hex)

(MSB)				(LSB)			
TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL
SYMBOL	POSITION	NAME AND DESCRIPTION					
TFM	CCR2.7	Transmit Frame Mode Select. 0=D4 framing mode 1=ESF framing mode					
TB8ZS	CCR2.6	Transmit B8ZS Enable. 0=B8ZS disabled 1=B8ZS enabled					
TSLC96	CCR2.5	Transmit SLC-96/Fs Bit Insertion Enable. 0=SLC-96 disabled 1=SLC-96 enabled					
TFDL	CCR2.4	Transmit Zero Stuffer Enable. 0=zero stuffer disabled 1=zero stuffer enabled					
RFM	CCR2.3	Receive Frame Mode Select. 0=D4 framing mode 1=ESF framing mode					
RB8ZS	CCR2.2	Receive B8ZS Enable. 0=B8ZS disabled 1=B8ZS enabled					
RSLC96	CCR2.1	Receive SLC-96 Enable. 0=SLC-96 disabled 1=SLC-96 enabled					
RFDL	CCR2.0	Receive Zero Destuffer Enable. 0=zero destuffer disabled 1=zero destuffer enabled					

CCR3: COMMON CONTROL REGISTER 3 (Address=30 Hex)

(MSB)								(LSB)
ESMDM	ESR	P16F	RSMS	PDE	TLD	TLU	LIRST	
SYMBOL		POSITION		NAME AND DESCRIPTION				
ESMDM	CCR3.7	Elastic Store Minimum Delay Mode. See Section 10.3 for details. 0=elastic stores operate at full two frame depth 1=elastic stores operate at 32-bit depth						
ESR	CCR3.6	Elastic Store Reset. Setting this bit from a zero to a one will force the elastic stores to a known depth. Should be toggled after SYSCLK has been applied and is stable. Must be cleared and set again for a subsequent reset.						
P16F	CCR3.5	Function of Pin 16. 0=Receive Loss of Sync (RLOS). 1=Loss of Transmit Clock (LOTCL).						
RSMS	CCR3.4	RSYNC Multiframe Skip Control. Useful in framing format conversions from D4 to ESF. 0=RSYNC will output a pulse at every multiframe 1=RSYNC will output a pulse at every other multiframe note: for this bit to have any affect, the RSYNC must be set to output multiframe pulses (RCR2.4=1 and RCR2.3=0).						
PDE	CCR3.3	Pulse Density Enforcer Enable. 0=disable transmit pulse density enforcer 1=enable transmit pulse density enforcer						
TLD	CCR3.2	Transmit Loop Down Code (001). 0=transmit data normally 1=replace normal transmitted data with loop down code						
TLU	CCR3.1	Transmit Loop Up Code (00001). 0=transmit data normally 1=replace normal transmitted data with loop up code						
LIRST	CCR3.0	Line Interface Reset. Setting this bit from a zero to a one will initiate an internal reset that affects the slicer, AGC, clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.						

LOOP CODE GENERATION

When either the CCR3.1 or CCR3.2 bits are set to one, the DS2151Q will replace the normal transmitted payload with either the Loop Up or Loop Down code respectively. The DS2151Q will overwrite the repeating loop code pattern with the framing bits. The SCT will continue to transmit the loop codes as long as either bit is set. It is an illegal state to have both CCR3.1 and CCR3.2 set to one at the same time.

PULSE DENSITY ENFORCER

The SCT always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403-199X:

- no more than 15 consecutive zeros
- at least N ones in each and every time window of 8 x (N + 1) bits where N=1 through 23.

Violations for the transmit and receive data streams are reported in the RIR2.2 and RIR2.1 bits respectively.

When the CCR3.3 is set to one, the DS2151Q will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to zero since B8ZS encoded data streams cannot violate the pulse density requirements.

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS2151Q should be configured for operation by writing to all of the internal registers (this includes setting the Test Register to 00Hex) since the contents of the internal registers cannot be predicted on power-up. Next, the LIRST bit should be toggled from zero to one to reset the line interface (it will take the DS2151Q about 40ms to recover from the LIRST being toggled). Finally, after the SYSCLK input is stable, the ESR bit should be toggled from a zero to a one (this step can be skipped if the elastic stores are disabled).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2151Q, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register 1 (RIR1), and Receive Information Register 2 (RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will

not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS2151Q which bits the user wishes to read and have cleared. The user will write a byte to one of these four registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and the previous value will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. The write-read-write scheme is unique to the four status registers and it allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2151Q with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the INT1 and INT2 pins respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

RIR1: RECEIVE INFORMATION REGISTER 1 (Address=22 Hex)

(MSB)								(LSB)
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE	
SYMBOL	POSITION	NAME AND DESCRIPTION						
COFA	RIR1.7	Change of Frame Alignment. Set when the last resync resulted in a change of frame or multiframe alignment.						
8ZD	RIR1.6	Eight Zero Detect. Set when a string of eight consecutive zeros have been received at RPOS and RNEG.						
16ZD	RIR1.5	Sixteen Zero Detect. Set when a string of sixteen consecutive zeros have been received at RPOS and RNEG.						
RESF	RIR1.4	Receive Elastic Store Full. Set when the receive elastic store buffer fills and a frame is deleted.						

RESE	RIR1.3	Receive Elastic Store Empty. Set when the receive elastic store buffer empties and a frame is repeated.
SEFE	RIR1.2	Severely Errored Framing Event. Set when 2 out of 6 framing bits (Ft or FPS) are received in error.
B8ZS	RIR1.1	B8ZS Code Word Detect. Set when a B8ZS code word is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.6.
FBE	RIR1.0	Frame Bit Error. Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

RIR2: RECEIVE INFORMATION REGISTER 2 (Address=31 Hex)

(MSB)								(LSB)
RL1	RL0	TESF	TESE	TSLIP	JALT	RPDV	TPDV	
SYMBOL		POSITION		NAME AND DESCRIPTION				
RL1	RIR2.7	Receive Level Bit 1. See Table 4–1.						
RL0	RIR2.6	Receive Level Bit 0. See Table 4–1.						
TESF	RIR2.5	Transmit Elastic Store Full. Set when the transmit elastic store buffer fills and a frame is deleted.						
TESE	RIR2.4	Transmit Elastic Store Empty. Set when the transmit elastic store buffer empties and a frame is repeated.						
TSLIP	RIR2.3	Transmit Elastic Store Slip Occurrence. Set when the transmit elastic store has either repeated or deleted a frame.						
JALT	RIR2.2	Jitter Attenuator Limit Trip. Set when the jitter attenuator FIFO reaches to within 4–bits of it's limit; useful for debugging jitter attenuation operation.						
RPDV	RIR2.1	Receive Pulse Density Violation. Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.						
TPDV	RIR2.0	Transmit Pulse Density Violation. Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.						

DS2151Q RECEIVE T1 LEVEL INDICATION Table 4-1

RL1	RLO	LEVEL RECEIVED
0	0	+2 dB to -7.5 dB
0	1	-7.5 dB to -15 dB
1	0	-15 dB to -22.5 dB
1	1	less than -22.5 dB

SR1: STATUS REGISTER 1 (Address=20 Hex)

(MSB)				(LSB)			
LUP	LDN	LOT	RSLIP	RBL	RYEL	RCL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION					
LUP	SR1.7	Loop Up Code Detected. Set when the repeating ...00001... loop up code is being received.					
LDN	SR1.6	Loop Down Code Detected. Set when the repeating ...001... loop down code is being received.					
LOT	SR1.5	Loss of Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 5.2us). Will force pin 16 high if enabled via CCR1.6. Based on RCLK.					
RSLIP	SR1.4	Receive Elastic Store Slip Occurrence. Set when the receive elastic store has either repeated or deleted a frame.					
RBL	SR1.3	Receive Blue Alarm. Set when a blue alarm is received at RTIP and RRING. See note below.					
RYEL	SR1.2	Receive Yellow Alarm. Set when a yellow alarm is received at RTIP and RRING.					
RCL	SR1.1	Receive Carrier Loss. Set when 192 consecutive zeros have been detected at RTIP and RRING.					
RLOS	SR1.0	Receive Loss of Sync. Set when the device is not synchronized to the receive T1 stream.					

DS2151Q ALARM SET AND CLEAR CRITERIA Table 4–2

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (see note 1 below)	when over a 3 ms window, five or less zeros are received	when over a 3 ms window, six or more zeros are received
Yellow Alarm 1. D4 bit 2 mode (RCR2.2=0)	when bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences	when bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences
2. D4 12th F-bit mode (RCR2.2=1; this mode is also referred to as the "Japanese Yellow Alarm")	when the 12th framing bit is set to one for two consecutive occurrences	when the 12th framing bit is set to zero for two consecutive occurrences
3. ESF Mode	when 16 consecutive patterns of 00FF hex appear in the FDL	when 14 or less patterns of 00FF hex out of 16 possible appear in the FDL
Red Alarm (RCL) (this alarm is also referred to as Loss of Signal)	when 192 consecutive zeros are received	when four or more ones out of a sliding window of 32 bits is received

NOTE:

- The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all ones signal. Blue alarm detectors should be able to operate properly in the presence of a 10–3 error rate and they should not falsely trigger on a framed all ones signal. The blue alarm criteria in the DS2151Q has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS status bit in detecting a blue alarm.

LOOP UP/DOWN CODE DETECTION

Bits SR1.7 and SR1.6 will indicate when either the standard "loop up" or "loop down" codes are being received by the DS2151Q. When a loop up code has been received for 5 seconds, the CPE is expected to loop the recovered data (without correcting BPVs) back to the source. The loop down code indicates that the loopback should be discontinued. See the AT&T publication TR 62411 for more details. The DS2151Q will detect the loop up/down codes in both framed and unframed cir-

cumstances with bit error rates as high as 10⁻². The loop code detector has a nominal integration period of 48ms. Hence, after about 48ms of receiving either code, the proper status bit will be set to a one. After this initial indication, it is recommend that the software poll the DS2151Q every 100ms to 500ms until 5 seconds has elapsed to insure that the code is continuously present. Once 5 seconds has passed, the DS2151Q should be taken into or out of loopback via the Remote Loopback (RLB) bit in CCR1.

SR2: STATUS REGISTER 2 (Address=21 Hex)

(MSB)				(LSB)			
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	-
SYMBOL	POSITION	NAME AND DESCRIPTION					
RMF	SR2.7	Receive Multiframe. Set on receive multiframe boundaries.					
TMF	SR2.6	Transmit Multiframe. Set on transmit multiframe boundaries.					
SEC	SR2.5	One Second Timer. Set on increments of one second based on RCLK; will be set in increments of 999ms, 999ms, and 1002ms every 3 seconds.					
RFDL	SR2.4	Receive FDL Buffer Full. Set when the receive FDL buffer (RFDL) fills to capacity (8-bits).					
TFDL	SR2.3	Transmit FDL Buffer Empty. Set when the transmit FDL buffer (TFDL) empties.					
RMTCH	SR2.2	Receive FDL Match Occurrence. Set when the RFDL matches either RFDLM1 or RFDLM2.					
RAF	SR2.1	Receive FDL Abort. Set when eight consecutive one's are received in the FDL.					
-	SR2.0	Not Assigned. Should be set to zero when written to.					

IMR1: INTERRUPT MASK REGISTER 1 (Address=7F Hex)

(MSB)				(LSB)			
LUP	LDN	LOT	SLIP	RBL	RYEL	RCL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION					
LUP	IMR1.7	Loop Up Code Detected. 0=interrupt masked 1=interrupt enabled					
LDN	IMR1.6	Loop Down Code Detected. 0=interrupt masked 1=interrupt enabled					
LOT	IMR1.5	Loss of Transmit Clock. 0=interrupt masked 1=interrupt enabled					

SLIP	IMR1.4	Elastic Store Slip Occurrence. 0=interrupt masked 1=interrupt enabled
RBL	IMR1.3	Receive Blue Alarm. 0=interrupt masked 1=interrupt enabled
RYEL	IMR1.2	Receive Yellow Alarm. 0=interrupt masked 1=interrupt enabled
RCL	IMR1.1	Receive Carrier Loss. 0=interrupt masked 1=interrupt enabled
RLOS	IMR1.0	Receive Loss of Sync. 0=interrupt masked 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=6F Hex)

(MSB)		(LSB)					
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	—
SYMBOL	POSITION	NAME AND DESCRIPTION					
RMF	IMR2.7	Receive Multiframe. 0=interrupt masked 1=interrupt enabled					
TMF	IMR2.6	Transmit Multiframe. 0=interrupt masked 1=interrupt enabled					
SEC	IMR2.5	One Second Timer. 0=interrupt masked 1=interrupt enabled					
RFDL	IMR2.4	Receive FDL Buffer Full. 0=interrupt masked 1=interrupt enabled					
TFDL	IMR2.3	Transmit FDL Buffer Empty. 0=interrupt masked 1=interrupt enabled					
RMTCH	IMR2.2	Receive FDL Match Occurrence. 0=interrupt masked 1=interrupt enabled					
RAF	IMR2.1	Receive FDL Abort. 0=interrupt masked 1=interrupt enabled					
—	IMR2.0	Not Assigned. Should be set to zero when written to.					

5.0 ERROR COUNT REGISTERS

There are a set of three counters in the DS2151Q that record bipolar violations, excessive zeros, errors in the CRC6 code words, framing bit errors, and number of multiframes that the device is out of receive synchronization. Each of these three counters are automatically updated on one second boundaries as determined by the one second timer in Status Register 2 (SR2.5). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the one second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost. All three counters will saturate at their respective maximum counts and they

will not rollover (note: only the Line Code Violation Count Register has the potential to overflow).

5.1 Line Code Violation Count Register (LCVCR)

Line Code Violation Count Register 1 (LCVCR1) is the most significant word and LCVCR2 is the least significant word of a 16-bit counter that records code violations (CVs). CVs are defined as Bipolar Violations (BPVs) or excessive zeros. See Table 5-1 for details of exactly what the LCVCRs count. If the B8ZS mode is set for the receive side via CCR2.2, then B8ZS code words are not counted. This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS=1) conditions.

LCVCR1: LINE CODE VIOLATION COUNT REGISTER 1 (Address=23 Hex)

LCVCR2: LINE CODE VIOLATION COUNT REGISTER 2 (Address=24 Hex)

(MSB)				(LSB)				(MSB)
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	LCVCR1
LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	LCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
LCV15	LCVCR1.7	MSB of the 16-Bit code violation count
LCV0	LCVCR2.0	LSB of the 16-Bit code violation count

LINE CODE VIOLATION COUNTING ARRANGEMENTS Table 5-1

COUNT EXCESSIVE ZEROS? (RCR1.7)	B8ZS ENABLED? (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs
no	no	BPVs
yes	no	BPVs + 16 consecutive zeros
no	yes	BPVs (B8ZS code words not counted)
yes	yes	BPVs + 8 consecutive zeros

5.2 Path Code Violation Count Register (PCVCR)

When the receive side of the DS2151Q is set to operate in the ESF framing mode (CCR2.3=1), PCVCR will automatically be set as a 12-bit counter that will record errors in the CRC6 code words. When set to operate in the D4 framing mode (CCR2.3=0), PCVCR will auto-

matically count errors in the Ft framing bit position. Via the RCR2.1 bit, the DS2151Q can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5-2 for a detailed description of exactly what errors the PCVCR counts.

PCVCR1: PATH VIOLATION COUNT REGISTER 1 (Address=25 Hex)**PCVCR2: PATH VIOLATION COUNT REGISTER 2** (Address=26 Hex)

(MSB)				(LSB)				
(note 1)	(note 1)	(note 1)	(note 1)	CRC/FB11	CRC/FB10	CRC/FB9	CRC/FB8	PCVCR1
CRC/FB7	CRC/FB6	CRC/FB5	CRC/FB4	CRC/FB3	CRC/FB2	CRC/FB1	CRC/FB0	PCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC/FB11	PCVCR1.3	MSB of the 12–Bit CRC6 Error or Frame Bit Error Count (note 2)
CRC/FB0	PCVCR2.0	LSB of the 12–Bit CRC6 Error or Frame Bit Error Count (note 2)

NOTES:

- the upper nibble of the counter at address 25 is used by the Multiframe Out of Sync Count Register
- PCVCR counts either errors in CRC code words (in the ESF framing mode; CCR2.3=1) or errors in the framing bit position (in the D4 framing mode; CCR2.3=0).

PATH CODE VIOLATION COUNTING ARRANGEMENTS Table 5–2

FRAMING MODE (CCR2.3)	COUNT FS ERRORS? (RCR2.1)	WHAT IS COUNTED IN THE PCVCRs
D4	no	errors in the Ft pattern
D4	yes	errors in both the Ft and Fs patterns
ESF	don't care	errors in the CRC6 code words

5.3 Multiframe Out of Sync Count Register (MOSCR)

Normally the MOSCR is used to count the number of multiframe that the receive synchronizer is out of sync (RCR2.0=1). This number is useful in ESF applications needing to measure the parameters Loss Of Frame Count (LOFC) and ESF Error Events as described in AT&T publication TR54016. When the MOSCR is operated in this mode, it is not disabled during receive loss of

synchronization (RLOS=1) conditions. The MOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the MOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS=1) conditions. See Table 5–3 for a detailed description of what the MOSCR is capable of counting.

MOSCR1: MULTIFRAMES OUT OF SYNC COUNT REGISTER 1 (Address=25 Hex)**MOSCR2: MULTIFRAMES OUT OF SYNC COUNT REGISTER 2** (Address=27 Hex)

(MSB)				(LSB)				
MOS/FB11	MOS/FB10	MOS/FB9	MOS/FB8	(note 1)	(note 1)	(note 1)	(note 1)	MOSCR1
MOS/FB7	MOS/FB6	MOS/FB5	MOS/FB4	MOS/FB3	MOS/FB2	MOS/FB1	MOS/FB0	MOSCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
MOS/FB11	MOSCR1.7	MSB of the 12–Bit Multiframe Out of Sync or F–Bit Error Count (note 2)
MOS/FB0	MOSCR2.0	LSB of the 12–Bit Multiframe Out of Sync or F–Bit Error Count (note 2)

NOTES:

- the lower nibble of the counter at address 25 is used by the Path Code Violation Count Register
- MOSCR counts either errors in framing bit position (RCR2.0=0) or the number of multiframes out of sync (RCR2.0=1)

MULTIFRAMES OUT OF SYNC COUNTING ARRANGEMENTS Table 5-3

FRAMING MODE (CCR2.3)	COUNT MOS OR F-BIT ERRORS? (RCR2.0)	WHAT IS COUNTED IN THE MOSCRs
D4	MOS	number of multiframes out of sync
D4	F-Bit	errors in the Ft pattern
ESF	MOS	number of multiframes out of sync
ESF	F-Bit	errors in the FPS pattern

6.0 FDL/FS EXTRACTION AND INSERTION

The DS2151Q has the ability to extract/insert data from/into the Facility Data Link (FDL) in the ESF framing mode and from/into Fs bit position in the D4 framing mode. Since SLC-96 utilizes the Fs bit position, this capability can also be used in SLC-96 applications. The operation of the receive and transmit sections will be discussed separately.

6.1 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2ms (8 times 250us). The DS2151Q will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the INT2 pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR2.2 bit will be set to a one and the INT2 pin will

toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The DS2151Q also contains a zero destuffer which is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than 5 ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.0, the DS2151Q will automatically look for 5 ones in a row, followed by a zero. If it finds such a pattern, it will automatically remove the zero. If the zero destuffer sees six or more ones in a row followed by a zero, the zero is not removed. The CCR2.0 bit should always be set to a one when the DS2151Q is extracting the FDL. More on how to use the DS2151Q in FDL and SLC-96 applications is covered in a separate Application Note. **Also, contact the factory for C code software that implements both ANSI T1.403 and AT&T TR54016.**

RFDL: RECEIVE FDL REGISTER (Address=28 Hex)

(MSB)				(LSB)			
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	MSB of the Received FDL Code
RFDL0	RFDL.0	LSB of the Received FDL Code

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RFDLM1: RECEIVE FDL MATCH REGISTER 1 (Address=29 Hex)
RFDLM2: RECEIVE FDL MATCH REGISTER 2 (Address=2A Hex)

(MSB)				(LSB)			
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0
SYMBOL		POSITION		NAME AND DESCRIPTION			
RFDL7		RFDL.7		MSB of the FDL Match Code			
RFDL0		RFDL.0		LSB of the FDL Match Code			

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RFDLM1/RFDLM2), RSR2.2 will be set to a one and the INT2 will go active if enabled via IMR2.2.

is not updated, the old value in the TFDL will be transmitted once again.

6.2 Transmit Section

The transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full eight bits has been shifted out, the DS2151Q will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to a one. The INT2 will also toggle low if enabled via IMR2.3. The user has 2ms (1.5ms in SLC-96 applications) to update the TFDL with a new value. If the TFDL

The DS2151Q also contains a zero stuffer which is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than 5 ones should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the DS2151Q will automatically look for 5 ones in a row. If it finds such a pattern, it will automatically insert a zero after the five ones. The CCR2.4 bit should always be set to a one when the DS2151Q is inserting the FDL. More on how to use the DS2151Q in FDL and SLC-96 applications is covered in a separate Application Note.

TFDL: TRANSMIT FDL REGISTER (Address=7E Hex)

(MSB)				(LSB)			
TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0
SYMBOL		POSITION		NAME AND DESCRIPTION			
TFDL7		TFDL.7		MSB of the FDL code to be transmitted			
TFDL0		TFDL.0		LSB of the FDL code to be transmitted			

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a

byte basis into the outgoing T1 data stream. The LSB is transmitted first.

7.0 SIGNALING OPERATION

The robbed bit signaling bits in embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2151Q. There is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The

CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to zero, then the robbed signaling bits will appear at RSER in their proper position as they are received. If CCR1.5 is set to a one, then the robbed signaling bit positions will be forced to a one at RSER.

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (Address=60 to 6B Hex)

(MSB)				(LSB)				
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	RS7 (66)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	RS8 (67)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	RS9 (68)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	RS10 (69)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	RS11 (6A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	RS12 (6B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	RS12.7	Signaling Bit D in Channel 24
A(1)	RS1.0	Signaling Bit A in Channel 1

Each Receive Signaling Register (RS1 to RS12) reports the incoming robbed bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two framing bits per channel (A and B). In the D4 framing mode, the DS2151Q will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the DS2151Q is operated in either framing

mode, the user needs only to retrieve the signaling bits every 3ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0=1). They will contain the most recent signaling information before the "OOF" occurred.

TS1 TO TS12: TRANSMIT SIGNALING REGISTERS (Address=70 to 7B Hex)

(MSB)				(LSB)				
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	TS1 (70)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	TS2 (71)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	TS3 (72)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	TS4 (73)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	TS5 (74)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	TS6 (75)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	TS7 (76)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	TS8 (77)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	TS9 (78)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	TS10 (79)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	TS11 (7A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	TS12 (7B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	Signaling Bit D in Channel 24
A(1)	TS1.0	Signaling Bit A in Channel 1

Each Transmit Signaling Register (TS1 to TS12) contains the Robbed Bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). On multiframe boundaries, the DS2151Q will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits. In the ESF framing mode, the interrupt will come every 3ms and the user has a full 3ms to update the TSR's. In the D4 framing mode, there are only two framing bits per channel (A and B). However in the D4 framing mode, the DS2151Q uses the C and D

bit positions as the A and B bit positions for the next multiframe. The DS2151Q will load the values in the TSRs into the outgoing shift register every other D4 multiframe.

8.0 SPECIAL TRANSMIT SIDE REGISTERS

There is a set of seven registers in the DS2151Q that can be used to custom tailor the data that is to be transmitted onto the T1 line, on a channel by channel basis. Each of the 24 T1 channels can be either forced to be transparent or to have a user defined idle code inserted into them. Each of these special registers is defined below.

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code
TIDR0	TIDR.0	LSB of the Idle Code

Each of the bit positions in the Transmit Idle Registers (TIDR0-TIDR7) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTERS (Address=39 to 3B Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (39)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	Transmit Transparency Registers. 0=this DS0 channel is not transparent 1=this DS0 channel is transparent
CH1	TTR1.0	

Each of the bit positions in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel is transparent (or clear). If a DS0 is programmed to be clear, no robbed bit signaling will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, bit 2 will be overwritten by a zero when a Yellow Alarm is transmitted. Also the user has the option to prevent the TTR registers from determining which channels are to have Bit 7 stuffing performed. If the TCR2.0 and TCR1.3 bits are set to one, then all 24 T1 channels will have Bit 7 stuffing performed on them regardless of how the TTR registers are programmed. In this manner, the TTR registers are only affecting which channels are to have robbed bit signaling inserted into them. Please see Figure 13–9 for more details.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address=3C to 3E Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	Transmit Idle Registers. 0=do not insert the Idle Code into this DS0 channel 1=insert the Idle Code into this channel
CH1	TIR1.0	

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=3F Hex)

(MSB)	(LSB)
TIDR7	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code
TIDR0	TIDR.0	LSB of the Idle Code

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3) represent a DS0 channel in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3) control the RCHBLK and TCHCLK pins respectively. The RCHBLK and TCHCLK pins are user programmable outputs that can be forced either high or low during indi-

vidual channels. These outputs can be used to block clocks to a USART or LAPD controller in Fractional T1 or ISDN-PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 13 for an example.

RCBR1/RCBR2/RCBR3: RECEIVE CHANNEL BLOCKING REGISTERS (Address=6C to 6E Hex)

(MSB)

(LSB)

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)

SYMBOL POSITION

NAME AND DESCRIPTION

CH24 RCBR3.7

Receive Channel Blocking Registers.

0=force the RCHBLK pin to remain low during this channel time

CH1 RCBR1.0

1=force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3: TRANSMIT CHANNEL BLOCKING REGISTERS (Address=32 to 34 Hex)

(MSB)

(LSB)

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (34)

SYMBOL POSITION

NAME AND DESCRIPTION

CH24 TCBR3.7

Transmit Channel Blocking Registers.

0=force the TCHBLK pin to remain low during this channel time

CH1 TCBR1.0

1=force the TCHBLK pin high during this channel time

10.0 ELASTIC STORES OPERATION

The DS2151Q has two onboard two-frame (386 bits) elastic stores. These elastic stores have two main purposes. First, they can be used to rate convert the T1 data stream to 2.048Mbps (or a multiple of 2.048Mbps) which is the E1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e. not frequency locked) backplane clock. Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The receive side elastic store can be enabled via CCR1.2 and the transmit side elastic store is enabled via CCR1.7. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.6).

10.1 Receive Side

If the receive side elastic store is enabled (CCR1.2=1), then the user must provide either a 1.544 MHz (CCR1.3=0) or 2.048 MHz (CCR1.3=1) clock at the SYSCLK pin. The user has the option of either providing a frame sync at the RFSYNC pin (RCR2.3=1) or having the RFSYNC pin provide a pulse on frame boundaries (RCR2.3=0). If the user wishes to obtain pulses at the frame boundary, then RCR2.4 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR2.4 must be set to one. If the user selects to apply a 2.048 MHz clock to the SYSCLK pin, then the data output at RSER will be forced to all ones every fourth channel and the F-bit will be deleted. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be forced

to a one. Also, in 2.048 MHz applications, the RCHBLK output will be forced high during the same channels as the RSER pin. See Section 13 for more details. This is useful in T1 to CEPT (E1) conversion applications. If the 386-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (193 bits) will be repeated at RSER and the SR1.4 and RIR1.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR1.4 bits will be set to a one.

10.2 Transmit Side

The transmit side elastic store can only be used if the receive side elastic store is enabled. The operation of the transmit elastic store is very similar to the receive side; both have controlled slip operation and both can operate with either a 1.544 MHz or a 2.048 MHz SYSCLK. When the transmit elastic store is enabled, both the SYSCLK and RSYNC signals are shared by both the elastic stores. Hence, they will have the same backplane PCM frame and data structure. Controlled slips in the transmit elastic store are reported in the RIR2.5 bit and the direction of the slip is reported in the RIR2.3 and RIR2.4 bits.

10.3 Minimum Delay Synchronous SYSCLK Mode

In applications where the DS2151Q is connected to backplanes that are frequency locked to the recovered

T1 clock (i.e. the RCLK output), the full two frame depth of the onboard elastic stores is really not needed. In fact, in some delay sensitive applications, the normal two frame depth may be excessive. If the CCR3.7 bit is set to one, then the receive elastic store (and also the transmit elastic store if it is enabled) will be forced to a maximum depth of 32 bits instead of the normal 386 bits. In this mode, the SYSCLK must be frequency locked to RCLK and all of the slip contention logic in the DS2151Q is disabled (since slips cannot occur). Also, since the buffer depth is no longer two frames deep, the DS2151Q must be set up to source either a frame or multiframe pulse at the RSYNC pin. On power-up after the SYSCLK has locked to the RCLK signal, the elastic store reset bit (CCR3.6) should be toggled from a zero to a one to insure proper operation.

11.0 RECEIVE MARK REGISTERS

The DS2151Q has the ability to replace the incoming data, on a channel-by-channel basis with either an idle code (7F Hex) or the digital milliwatt code which is a eight byte repeating pattern that represents a 1 KHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). The RCR2.7 bit will determine which code is used. Each bit in the RMRs, represents a particular channel. If a bit is set to a one, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to zero, no replacement occurs.

RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (Address=2D to 2F Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1 (2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2 (2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3 (2F)

SYMBOL POSITION NAME AND DESCRIPTION

CH24 RMR3.7

Receive Channel Blocking Registers.

0=do not affect the receive data associated with this channel

CH1 RMR1.0

1=replace the receive data associated with this channel with either the idle code or the digital milliwatt code (depends on the RCR2.7 bit)

12.0 LINE INTERFACE FUNCTIONS

The line interface function in the DS2151Q contains three sections; (1) the receiver which handles clock and data recovery, (2) the transmitter which waveshapes

and drives the T1 line, and (3) the jitter attenuator. Each of these three sections is controlled by the Line Interface Control Register (LICR) which is described below.

LICR: LINE INTERFACE CONTROL REGISTER (Address=7C Hex)

(MSB)			(LSB)					
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD	LICR
SYMBOL	POSITION	NAME AND DESCRIPTION						
L2	LICR.7	Line Build Out Select Bit 2. Sets the transmitter build out; see the Table 12-2						
L1	LICR.6	Line Build Out Select Bit 2. Sets the transmitter build out; see the Table 12-2						
L0	LICR.5	Line Build Out Select Bit 2. Sets the transmitter build out; see the Table 12-2						
EGL	LICR.4	Receive Equalizer Gain Limit. 0=-36 dB 1=-30 dB						
JAS	LICR.3	Jitter Attenuator Select. 0=place the jitter attenuator on the receive side 1=place the jitter attenuator on the transmit side						
JABDS	LICR.2	Jitter Attenuator Buffer Depth Select . 0=128 bits 1=32 bits (use for delay sensitive applications)						
DJA	LICR.1	Disable Jitter Attenuator. 0=jitter attenuator enabled 1=jitter attenuator disabled						
TPD	LICR.0	Transmit Power Down. 0=normal transmitter operation 1=powers down the transmitter and 3-states the TTIP and TRING pins						

12.1 Receive Clock and Data Recovery

The DS2151Q contains a digital clock recovery system. See the DS2151Q Block Diagram in Section 1 and Figure 12-1 for more details. The DS2151Q couples to the receive T1 twisted pair via a 1:1 transformer. See Table 12-3 for transformer details. The DS2151Q automatically adjusts to the T1 signal being received at the RTIP and RRING pins and can handle T1 lines from 0 feet to over 6000 feet in length. The crystal attached at the XTAL1 and XTAL2 pins is multiplied by four via an internal PLL and fed to the clock recovery system. The clock recovery system uses both edges of the clock from the PLL circuit to form a 32 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance (see Figure 12-2). The EGL bit in the Line Interface Control Register is used to limit the sensitivity of the receiver in the

DS2151Q. For most CPE applications, a receiver sensitivity of -30 dB is wholly sufficient and hence the EGL bit should be set to one. In some applications, more sensitivity than -30 dB may be required and the DS2151Q will allow the receiver to go as low as -36 dB if the EGL bit is set to one. However when the EGL bit is set to zero, the DS2151Q will be more susceptible to crosstalk and its jitter tolerance will suffer.

Normally, the clock that is output at the RCLK pin is the recovered clock from the T1 AMI waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK can be sourced from either the ACLKI pin or from the crystal attached to the XTAL1 and XTAL2 pins. The DS2151Q will sense the ACLKI pin to determine if a clock is present. If no

clock is applied to the ACLKI pin, then it should be tied to RVSS to prevent the device from falsely sensing a clock. See Table 12–1. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit short high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry.

If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. Please see the Receive AC Timing Characteristics in Section 14 for more details.

SOURCE OF RCLK UPON RCL Table 12–1

ACLK PRESENT?	RECEIVE SIDE JITTER ATTENUATOR	TRANSMIT SIDE JITTER ATTENUATOR
Yes	ACLK via the jitter attenuator	ACLK
No	centered crystal	TCLK via the jitter attenuator

12.2 Transmit Waveshaping and Line Driving

The DS2151Q uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the T1 line. The waveforms created by the DS2151Q

meet the latest ANSI, AT&T, and CCITT specifications. See Figure 12–3. The user will select which waveform is to be generated by properly programming the L0 to L2 bits in the Line Interface Control Register (LICR).

LBO SELECT IN LICR Table 12–2

L2	L1	L0	LINE BUILD OUT	APPLICATION
0	0	0	0 to 133 feet/0 dB	DSX–1/CSU
0	0	1	133 to 266 feet	DSX–1
0	1	0	266 to 399 feet	DSX–1
0	1	1	399 to 533 feet	DSX–1
1	0	0	533 to 655 feet	DSX–1
1	0	1	–7.5 dB	CSU
1	1	0	–15 dB	CSU
1	1	1	–22.5 dB	CSU

Due to the nature of the design of the transmitter in the DS2151Q, very little jitter (less than 0.005UIpp broad-Band from 10Hz to 100 KHz) is added to the jitter present on TCLK. Also, the waveforms that they create are independent of the duty cycle of TCLK. The transmitter

in the DS2151Q couples to the T1 transmit twisted pair via a 1:1.15 or 1:1.36 step up transformer as shown in Figure 12–1. In order for the devices to create the proper waveforms, the transformer used must meet the specifications listed in Table 12–3.

TRANSFORMER SPECIFICATIONS Table 12–3

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:1.15 or 1:1.36 (transmit) $\pm 5\%$
Primary Inductance	600 μH minimum
Leakage Inductance	1.0 μH maximum
Interwinding Capacitance	40 pF maximum
DC Resistance	1.2 ohms maximum

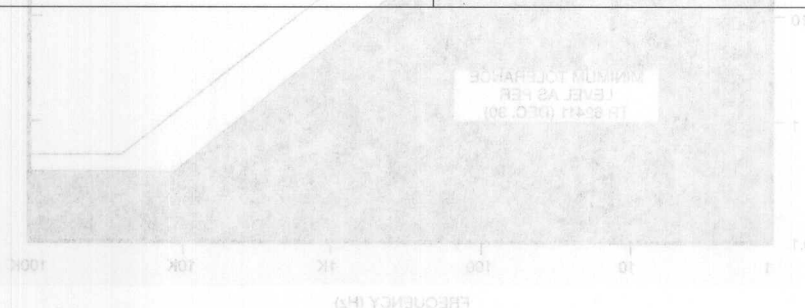
12.3 JITTER ATTENUATOR

The DS2151Q contains an onboard jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128 bit mode is used in applications where large excursions of wander are expected. The 32 bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 12–4. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit in the LICR. In order for the jitter attenuator to operate properly, a crystal with the specifications listed in Table 12–4 below must be connected to the XTAL1 and XTAL2 pins.

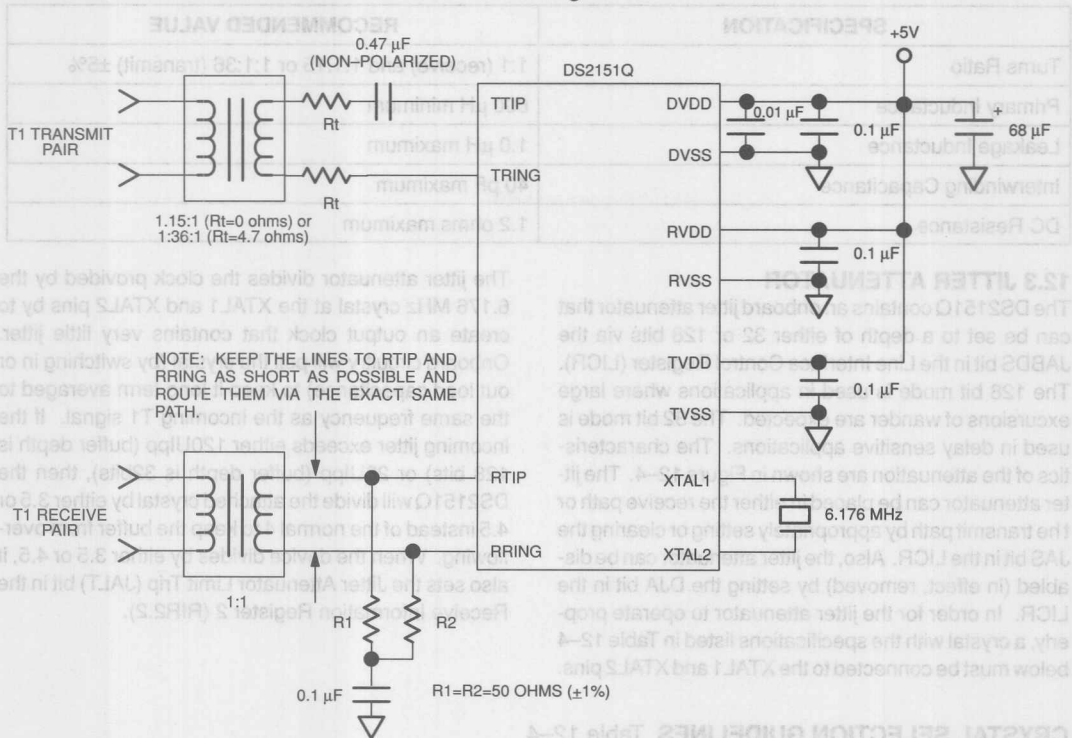
The jitter attenuator divides the clock provided by the 6.176 MHz crystal at the XTAL1 and XTAL2 pins by to create an output clock that contains very little jitter. Onboard circuitry will pull the crystal (by switching in or out load capacitance) to keep it long term averaged to the same frequency as the incoming T1 signal. If the incoming jitter exceeds either 120U1pp (buffer depth is 128 bits) or 28U1pp (buffer depth is 32bits), then the DS2151Q will divide the attached crystal by either 3.5 or 4.5 instead of the normal 4 to keep the buffer from overflowing. When the device divides by either 3.5 or 4.5, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register 2 (RIR2.2).

CRYSTAL SELECTION GUIDELINES Table 12–4

PARAMETER	SPECIFICATION
Parallel Resonant Frequency	6.176 MHz
Mode	Fundamental
Load Capacitance	18 pF to 20 pF (18.5 pF nominal)
Tolerance	± 50 ppm
Pullability	CL=10 pF, delta frequency=+175 to +250 ppm CL=45 pF, delta frequency=–175 to –250 ppm
Effective Series Resistance	40 ohms maximum
Crystal Cut	AT

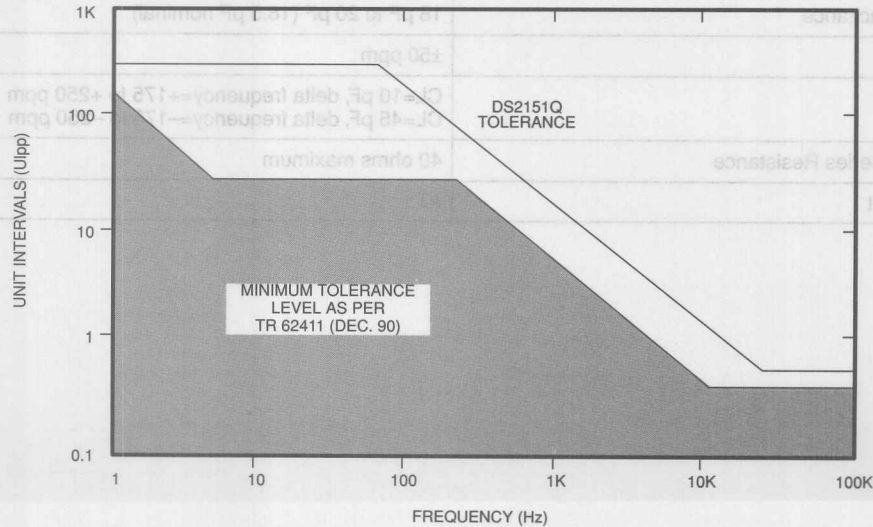


DS2151Q EXTERNAL ANALOG CONNECTIONS Figure 12-1

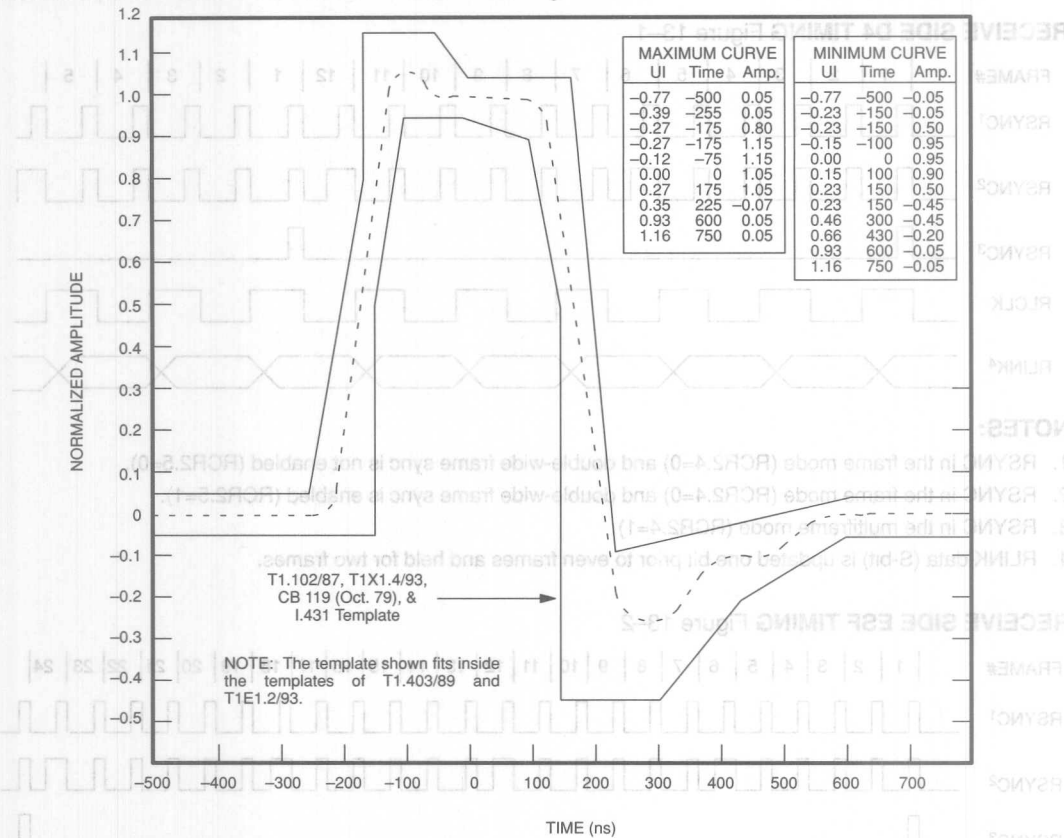


NOTE:
See the separate Application Note for details on how to construct a protected interface.

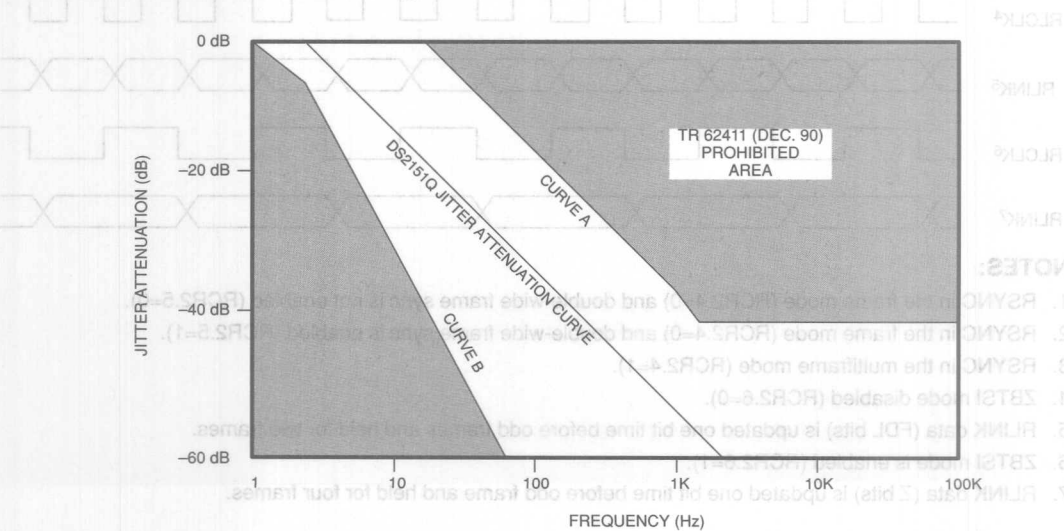
DS2151Q JITTER TOLERANCE Figure 12-2



DS2151Q TRANSMIT WAVEFORM TEMPLATE Figure 12-3

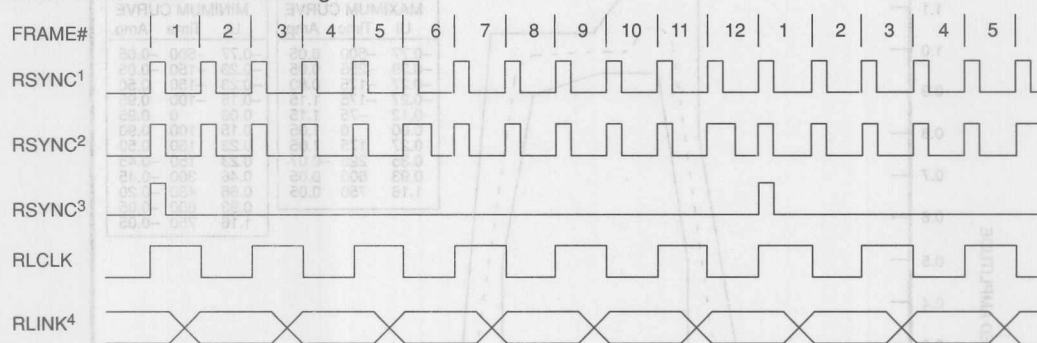


DS2151Q JITTER ATTENUATION Figure 12-4



13.0 TIMING DIAGRAMS

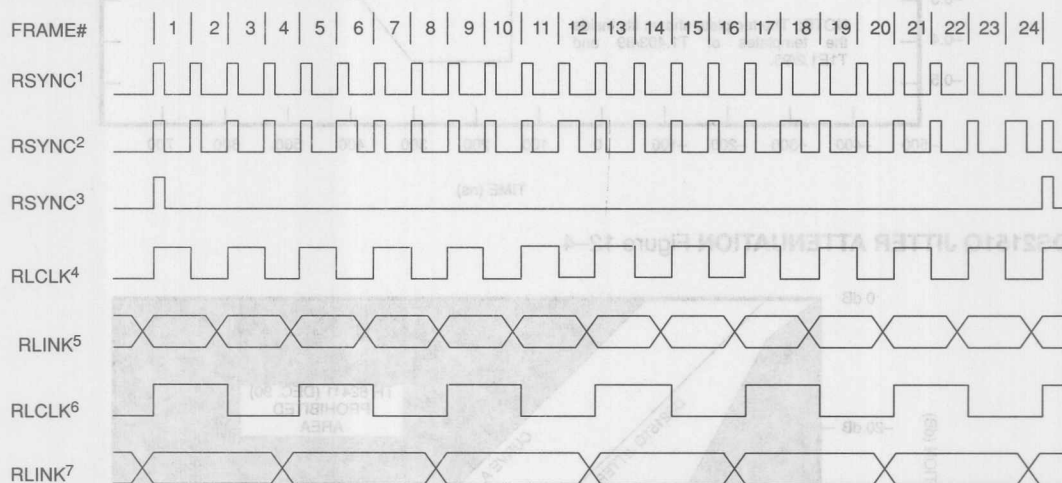
RECEIVE SIDE D4 TIMING Figure 13–1



NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. RLINK data (S-bit) is updated one bit prior to even frames and held for two frames.

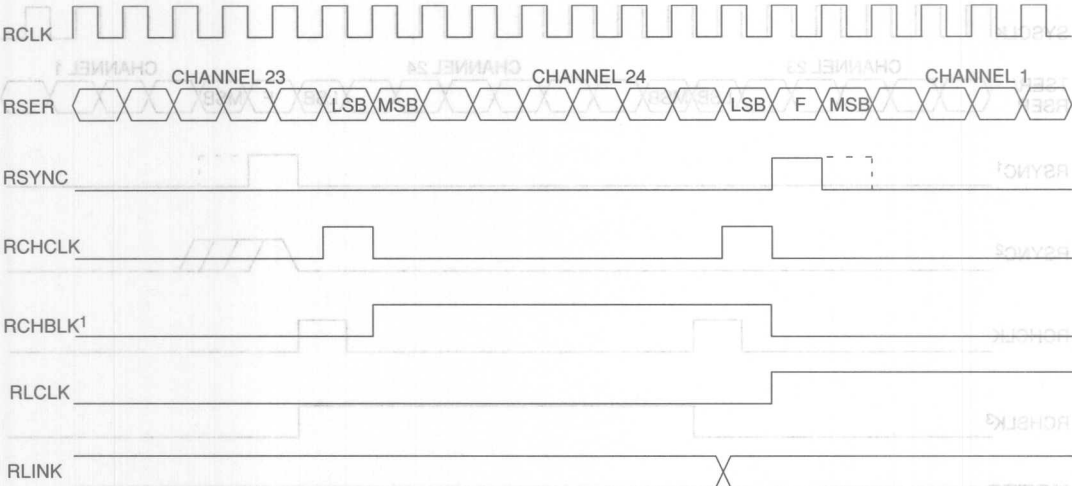
RECEIVE SIDE ESF TIMING Figure 13–2



NOTES:

1. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is not enabled (RCR2.5=0).
2. RSYNC in the frame mode (RCR2.4=0) and double-wide frame sync is enabled (RCR2.5=1).
3. RSYNC in the multiframe mode (RCR2.4=1).
4. ZBTISI mode disabled (RCR2.6=0).
5. RLINK data (FDL bits) is updated one bit time before odd frames and held for two frames.
6. ZBTISI mode is enabled (RCR2.6=1).
7. RLINK data (Z bits) is updated one bit time before odd frame and held for four frames.

RECEIVE SIDE BOUNDARY TIMING WITH ELASTIC STORE(S) DISABLED Figure 13-3

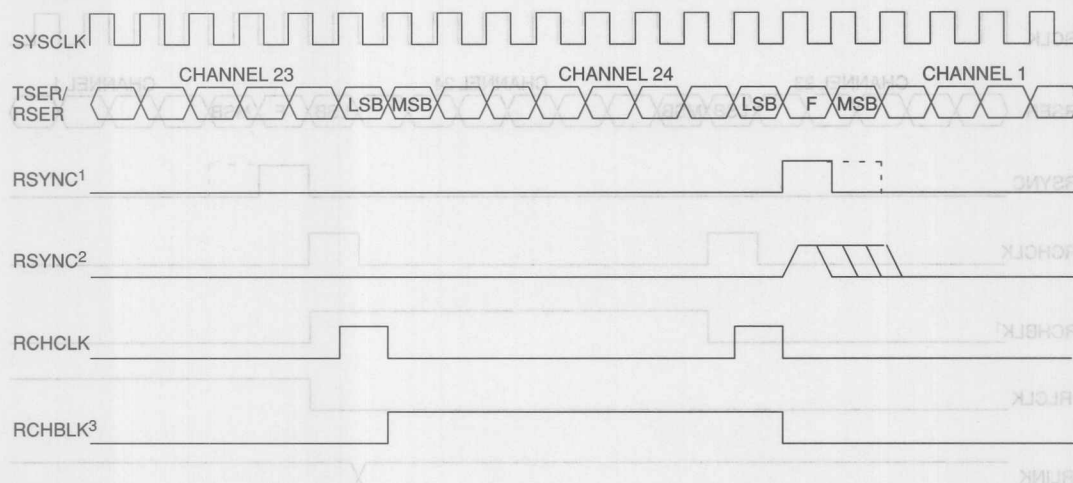


NOTES:

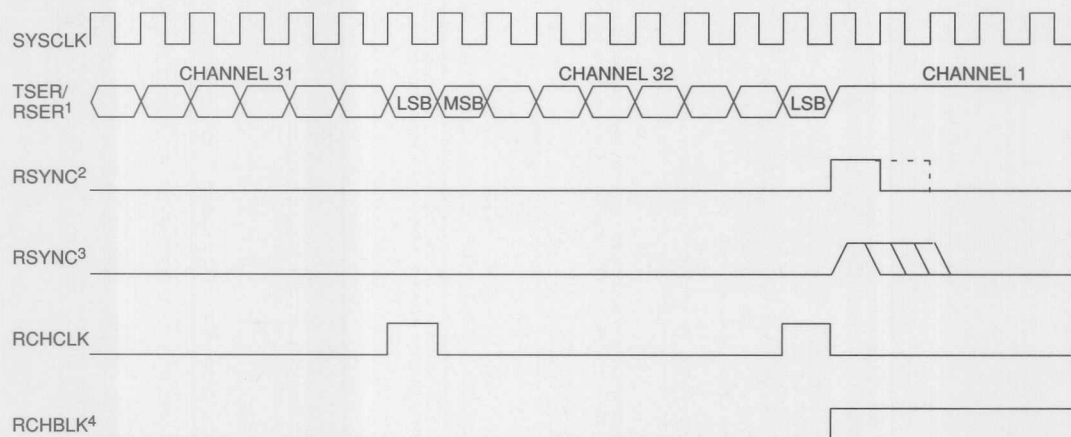
- 1. RCHBLK is programmed to block channel 24.



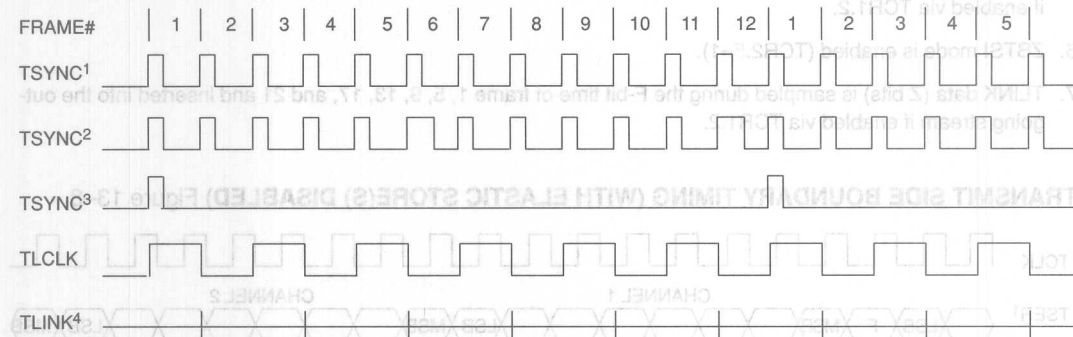
- NOTES:
- 1. RSER data in channels 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100 are forced to 1; TSEI ignored during these channels.
 - 2. RSYNC is in the output mode (RCSR3=0).
 - 3. RSYNC is in the input mode (RCSR3=1).
 - 4. RCHBLK is forced to 1 in the same channels as RSER (see Note 1).

1.544 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED Figure 13-4**NOTES:**

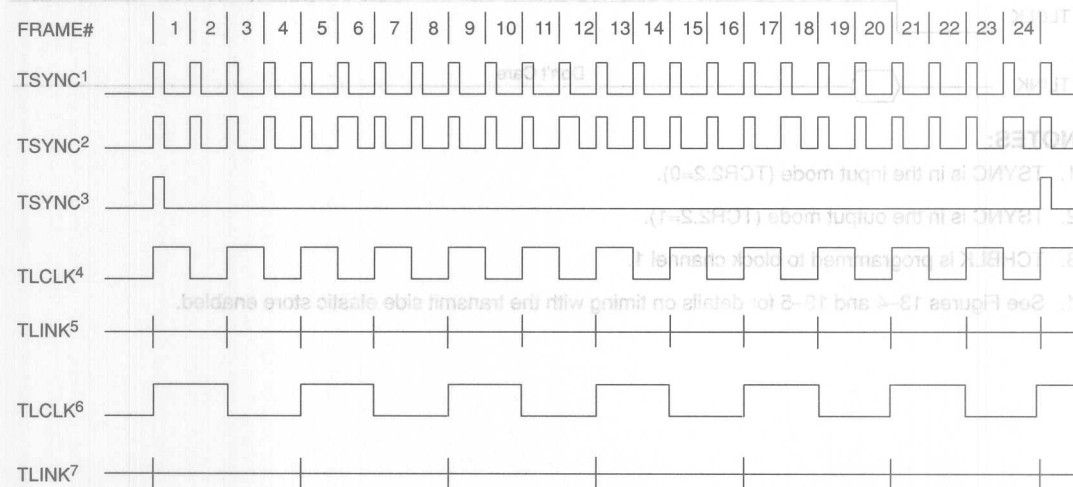
1. RSYNC is in the output mode (RCR2.3=0).
2. RSYNC is in the input mode (RCR2.3=1).
3. RCHBLK is programmed to block channel 24.

2.048 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED Figure 13-5**NOTES:**

1. RSER data in channels 1, 5, 9, 13, 17, 21, 25, and 29 are forced to 1; TSER ignored during these channels.
2. RSYNC is in the output mode (RCR2.3=0).
3. RSYNC is in the input mode (RCR2.3=1).
4. RCHBLK is forced to 1 in the same channels as RSER (see Note 1).

TRANSMIT SIDE D4 TIMING Figure 13–6**NOTES:**

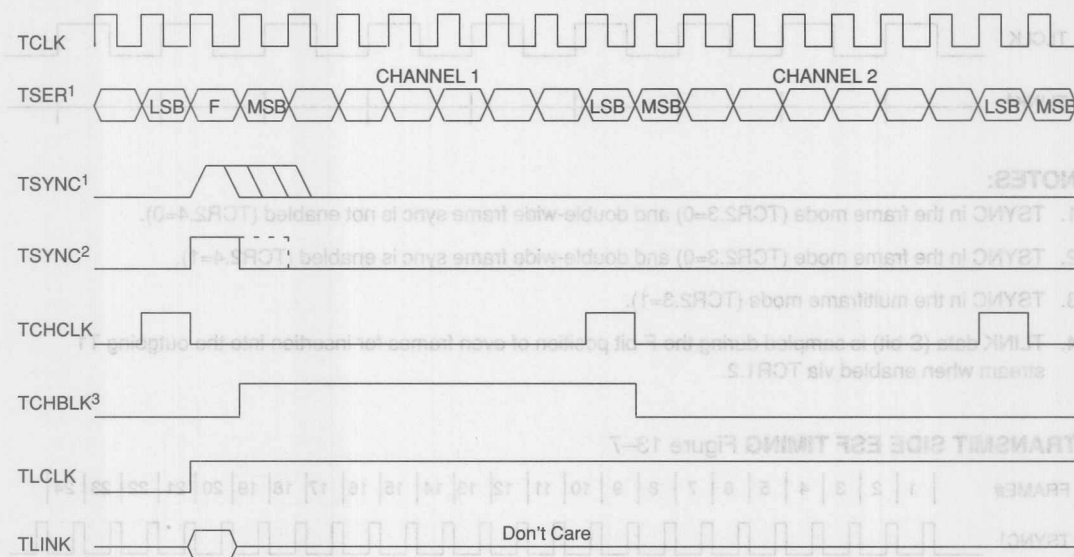
1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.3=1).
4. TLINK data (S-bit) is sampled during the F-bit position of even frames for insertion into the outgoing T1 stream when enabled via TCR1.2.

TRANSMIT SIDE ESF TIMING Figure 13–7**NOTES:**

1. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is not enabled (TCR2.4=0).
2. TSYNC in the frame mode (TCR2.3=0) and double-wide frame sync is enabled (TCR2.4=1).
3. TSYNC in the multiframe mode (TCR2.4=1).
4. ZBTSl mode disabled (TCR2.5=0).

5. TLINK data (FDL bits) is sampled during the F-bit time of odd frame and inserted into the outgoing T1 stream if enabled via TCR1.2.
6. ZBTSI mode is enabled (TCR2.5=1).
7. TLINK data (Z bits) is sampled during the F-bit time of frame 1, 5, 9, 13, 17, and 21 and inserted into the outgoing stream if enabled via TCR1.2.

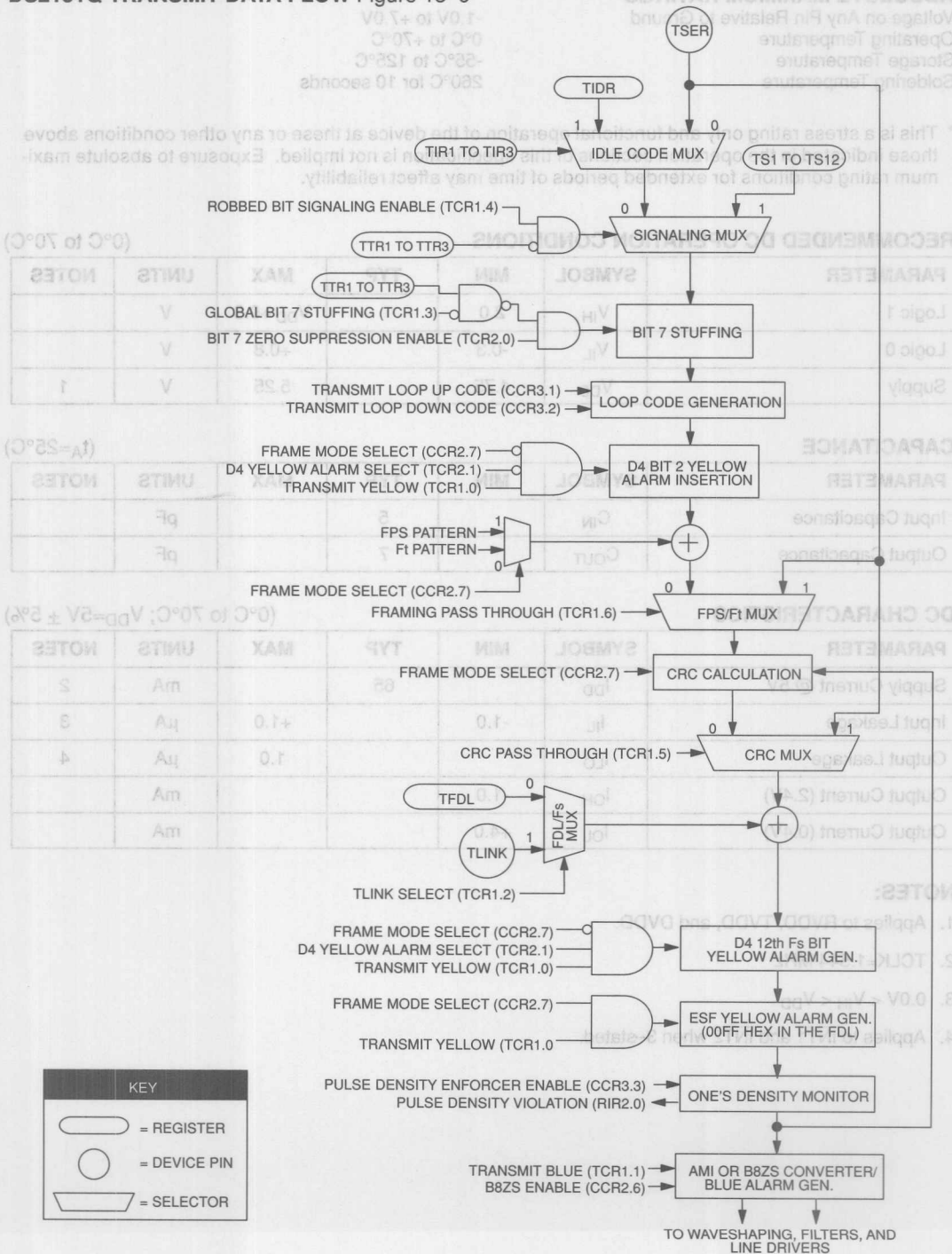
TRANSMIT SIDE BOUNDARY TIMING (WITH ELASTIC STORE(S) DISABLED) Figure 13–8



NOTES:

1. TSYNC is in the input mode (TCR2.2=0).
2. TSYNC is in the output mode (TCR2.2=1).
3. TCHBLK is programmed to block channel 1.
4. See Figures 13–4 and 13–5 for details on timing with the transmit side elastic store enabled.

DS2151Q TRANSMIT DATA FLOW Figure 13-9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground
 Operating Temperature
 Storage Temperature
 Soldering Temperature

-1.0V to +7.0V
 0°C to +70°C
 -55°C to 125°C
 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.75		5.25	V	1

CAPACITANCE(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

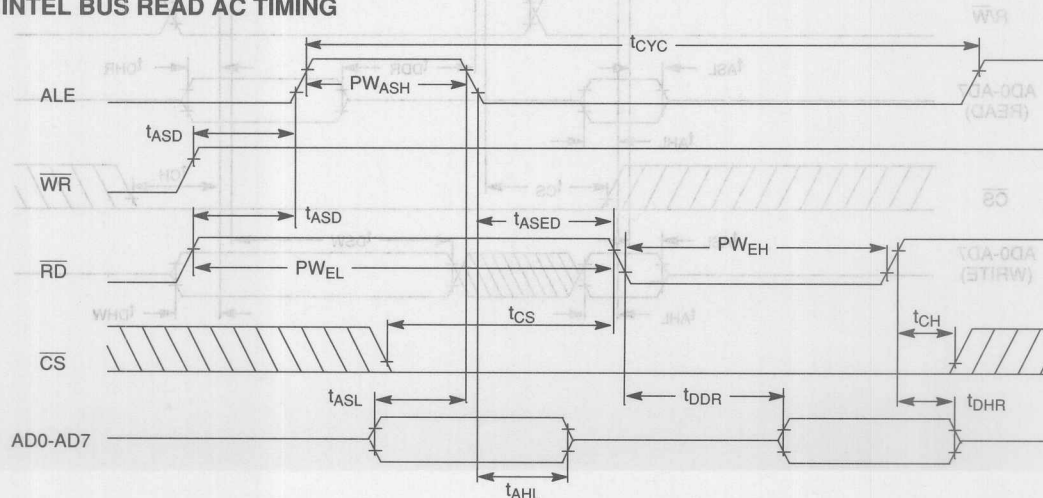
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		65		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	μA	3
Output Leakage	I_{LO}			1.0	μA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

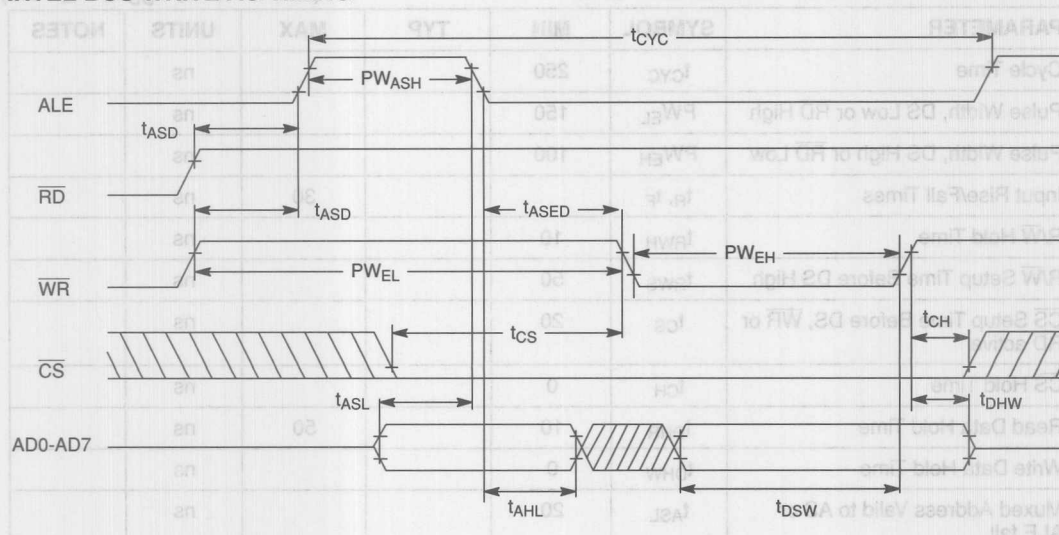
1. Applies to RVDD, TVDD, and DVDD.
2. TCLK=1.544 MHz
3. $0.0V < V_{IN} < V_{DD}$
4. Applies to INT1 and INT2 when 3—stated.

AC CHARACTERISTICS - PARALLEL PORT(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

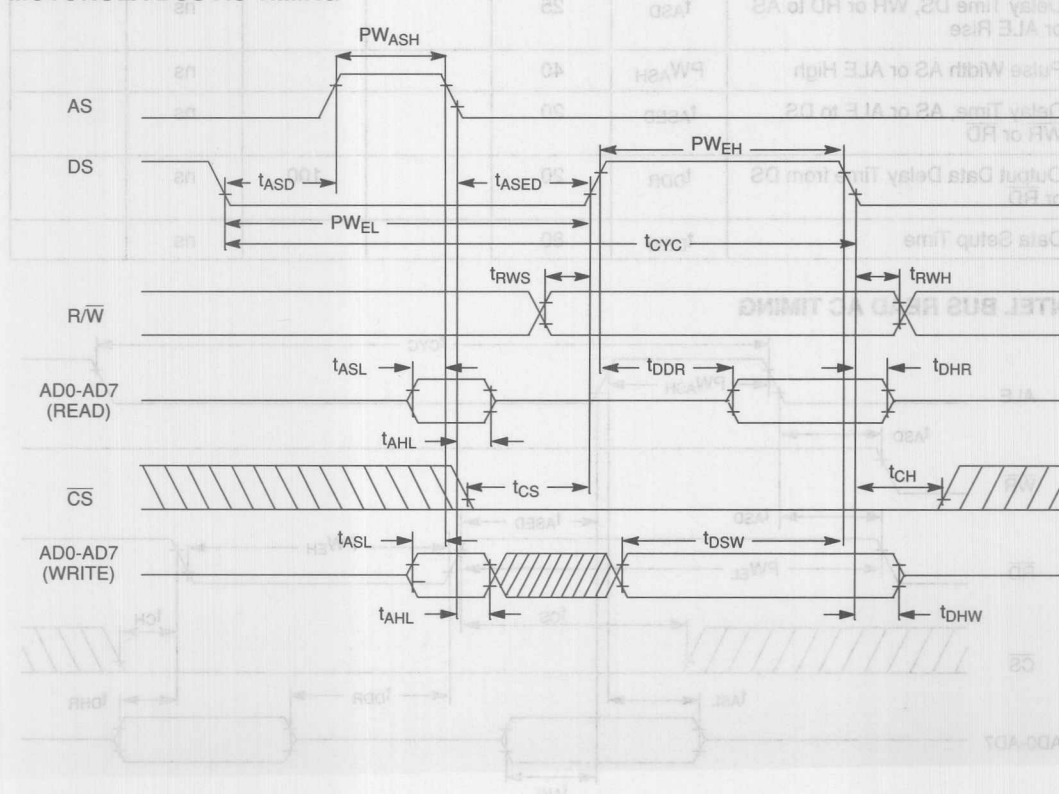
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	250			ns	
Pulse Width, DS Low or \overline{RD} High	PW_{EL}	150			ns	
Pulse Width, DS High or \overline{RD} Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			30	ns	
R/ \overline{W} Hold Time	t_{RWH}	10			ns	
R/ \overline{W} Setup Time Before DS High	t_{RWS}	50			ns	
\overline{CS} Setup Time Before DS, \overline{WR} or \overline{RD} active	t_{CS}	20			ns	
\overline{CS} Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE fall	t_{ASL}	20			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS, \overline{WR} or \overline{RD} to AS or ALE Rise	t_{ASD}	25			ns	
Pulse Width AS or ALE High	PW_{ASH}	40			ns	
Delay Time, AS or ALE to DS, \overline{WR} or \overline{RD}	t_{ASED}	20			ns	
Output Data Delay Time from DS or \overline{RD}	t_{DDR}	20		100	ns	
Data Setup Time	t_{DSW}	80			ns	

INTEL BUS READ AC TIMING

INTEL BUS WRITE AC TIMING



MOTOROLA BUS AC TIMING



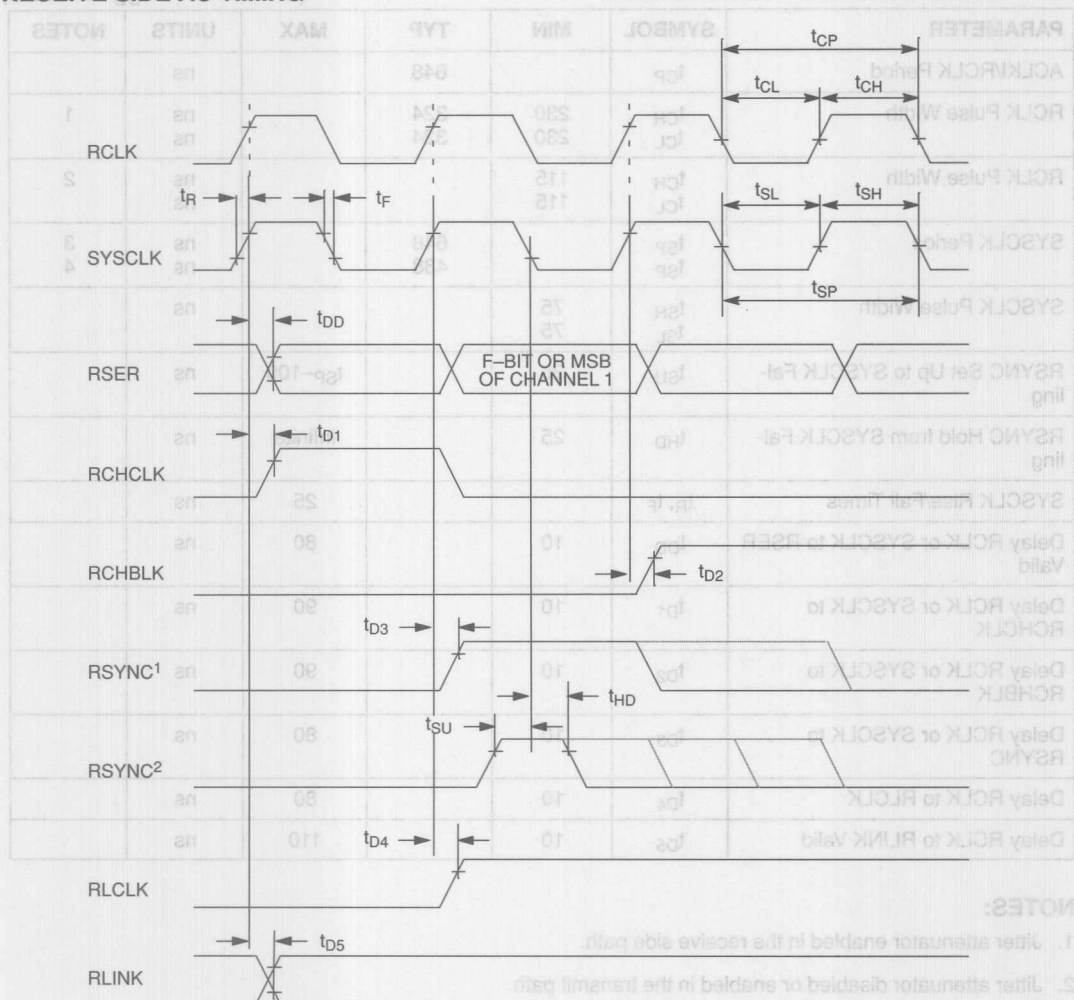
AC CHARACTERISTICS – RECEIVE SIDE(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ACLKI/RCLK Period	t_{CP}		648		ns	
RCLK Pulse Width	t_{CH} t_{CL}	230 230	324 324		ns ns	1
RCLK Pulse Width	t_{CH} t_{CL}	115 115			ns ns	2
SYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	3 4
SYSCLK Pulse Width	t_{SH} t_{SL}	75 75			ns	
RSYNC Set Up to SYSCLK Falling	t_{SU}	25		$t_{SP}-100$	ns	
RSYNC Hold from SYSCLK Falling	t_{HD}	25		infinite	ns	
SYSCLK Rise/Fall Times	t_R, t_F			25	ns	
Delay RCLK or SYSCLK to RSER Valid	t_{DD}	10		80	ns	
Delay RCLK or SYSCLK to RCHCLK	t_{D1}	10		90	ns	
Delay RCLK or SYSCLK to RCHBLK	t_{D2}	10		90	ns	
Delay RCLK or SYSCLK to RSYNC	t_{D3}	10		80	ns	
Delay RCLK to RLCLK	t_{D4}	10		80	ns	
Delay RCLK to RLINK Valid	t_{D5}	10		110	ns	

NOTES:

1. Jitter attenuator enabled in the receive side path.
2. Jitter attenuator disabled or enabled in the transmit path.
3. SYSCLK=1.544 MHz
4. SYSCLK=2.048 MHz

RECEIVE SIDE AC TIMING



NOTES:

1. RSYNC is in the output mode (RCR2.3=0).
2. RSYNC is in the input mode (RCR2.3=1).
3. RLCLK and RLINK only have a timing relationship to RCLK.
4. RCLK can exhibit a short high time if the jitter attenuator is either disabled or in the transmit path.

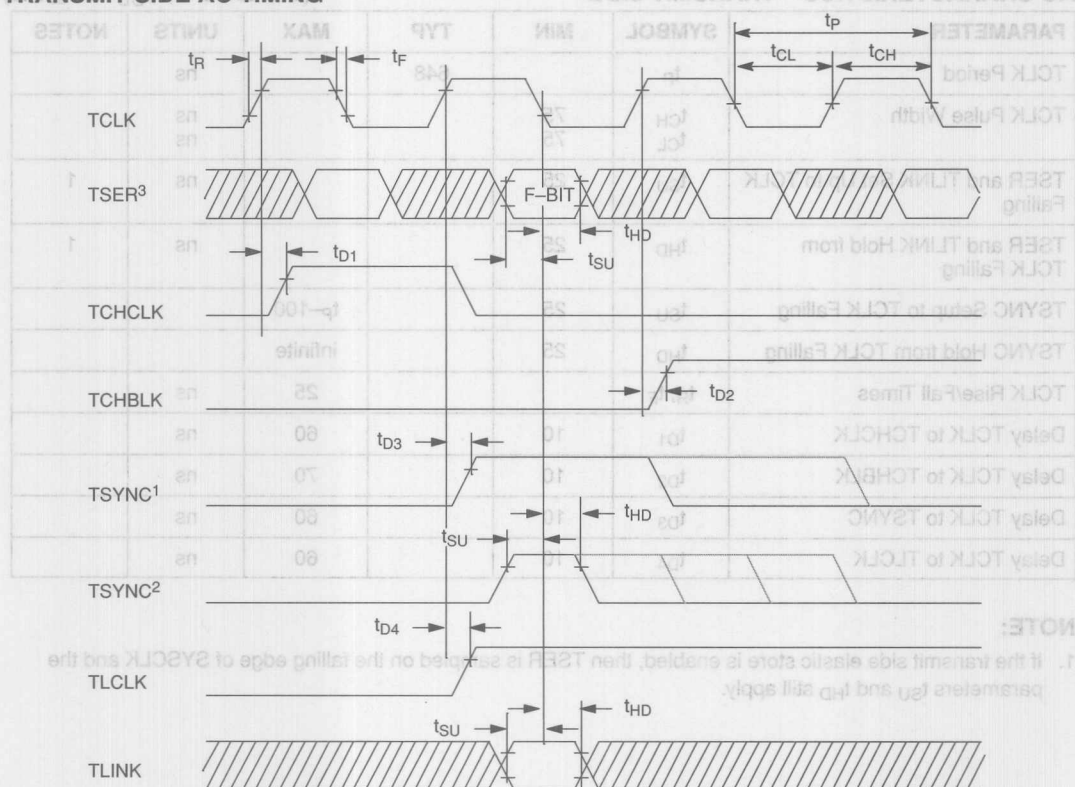
AC CHARACTERISTICS – TRANSMIT SIDE(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_p		648		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TSER and TLINK Set Up to TCLK Falling	t_{SU}	25			ns	1
TSER and TLINK Hold from TCLK Falling	t_{HD}	25			ns	1
TSYNC Setup to TCLK Falling	t_{SU}	25		t_p-100		
TSYNC Hold from TCLK Falling	t_{HD}	25		infinite		
TCLK Rise/Fall Times	t_R, t_F			25	ns	
Delay TCLK to TCHCLK	t_{D1}	10		60	ns	
Delay TCLK to TCHBLK	t_{D2}	10		70	ns	
Delay TCLK to TSYNC	t_{D3}	10		60	ns	
Delay TCLK to TLCLK	t_{D4}	10		60	ns	

NOTE:

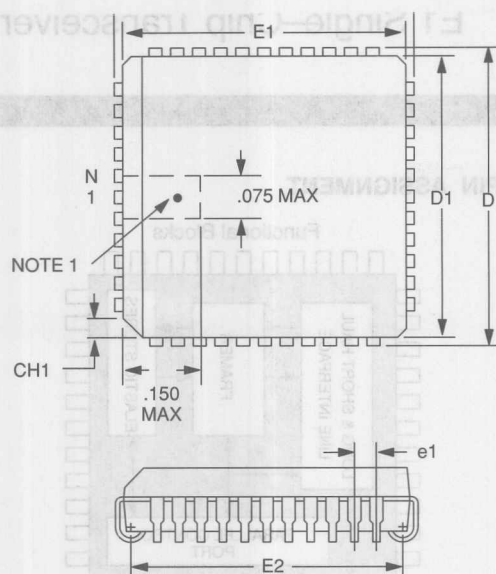
1. If the transmit side elastic store is enabled, then TSER is sampled on the falling edge of SYSCLK and the parameters t_{SU} and t_{HD} still apply.

TRANSMIT SIDE AC TIMING



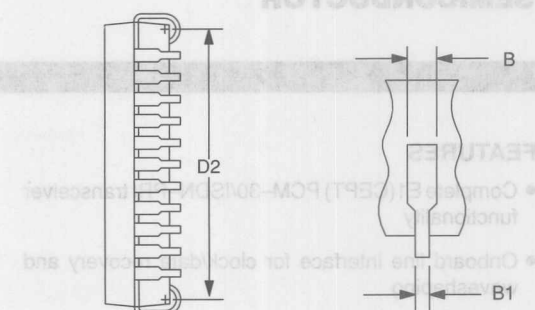
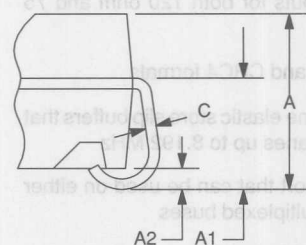
NOTES:

1. TSYNC is in the output mode (TCR2.2=1).
2. TSYNC is in the input mode (TCR2.2=0).
3. TSER is sampled on the falling edge of SYSCLK if the transmit side elastic store is enabled.



NOTE1: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	—



- 32-bit or 138-bit filter attenuator
- Generates line build outs for both 150 ohm and 75 ohm lines
- Frames to FAS, CAS, and CCL format
- Dual onboard two-term elastic buffers that can connect to backplanes up to 8 inches long
- 8-bit parallel control that can be either multiplexed or non-multiplexed buses
- Extracts and inserts CAS signaling
- Detects and generates Remote and AIS alarms
- Programmable output clocks for Fractional ET, H0, and H12 applications
- Fully independent transmit and receive functionality
- Full access to both S1 and S2 pins
- Three separate lookbacks for testing
- Large counters for bipolar and code violations, CRCM code word error, FAS error, and E-bits
- Pin compatible with DS15C01T1 Single-Chip Transceiver
- 5V supply; low power CMOS

DESCRIPTION

The DS15C01T1 Single-Chip Transceiver (SCT) contains all of the necessary functions for connection to E1 lines. The onboard recovery circuitry covers the AMRDS E1 waveform to a NRZ serial stream both 75 ohm and 150 ohm.

DALLAS

SEMICONDUCTOR

DS2153Q

E1 Single-Chip Transceiver

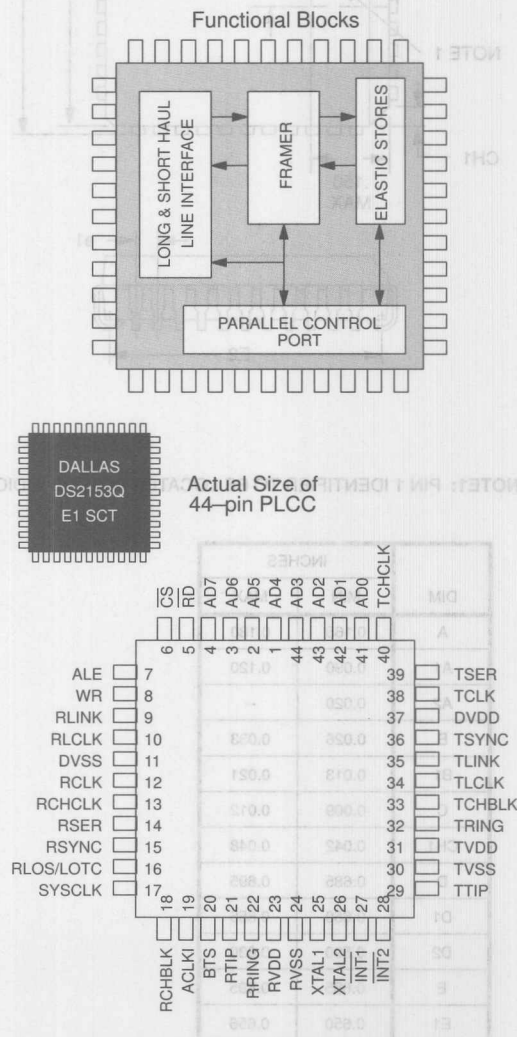
FEATURES

- Complete E1 (CEPT) PCM-30/ISDN-PRI transceiver functionality
- Onboard line interface for clock/data recovery and waveshaping
- 32-bit or 128-bit jitter attenuator
- Generates line build outs for both 120 ohm and 75 ohm lines
- Frames to FAS, CAS, and CRC4 formats
- Dual onboard two-frame elastic store slip buffers that can connect to backplanes up to 8.192 MHz
- 8-bit parallel control port that can be used on either multiplexed or non-multiplexed buses
- Extracts and inserts CAS signaling
- Detects and generates Remote and AIS alarms
- Programmable output clocks for Fractional E1, H0, and H12 applications
- Fully independent transmit and receive functionality
- Full access to both Si and Sa bits
- Three separate loopbacks for testing
- Large counters for bipolar and code violations, CRC4 code word errors, FAS errors, and E-bits
- Pin compatible with DS2151Q T1 Single-Chip Transceiver
- 5V supply; low power CMOS

DESCRIPTION

The DS2153Q T1 Single-Chip Transceiver (SCT) contains all of the necessary functions for connection to E1 lines. The onboard clock/data recovery circuitry converts the AMI/HDB3 E1 waveforms to a NRZ serial stream.

PIN ASSIGNMENT



attenuator (selectable to either 32-bits or 128-bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, Si, and Sa bit information. The device contains a set of 71 eight-bit internal registers which the user can access and control the operation of the unit. Quick access via the parallel control port allows a single micro to handle many E1 lines. The device fully meets all of the latest E1 specifications including ITU G.703, G.704, G.706, G.823, and I.431 as well as ETSI 300 011 and 300 233.

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1.0 INTRODUCTION

The analog AMI waveform off of the E1 line is transformer coupled into the RRING and RTIP pins of the DS2153Q. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing pattern. If

needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input.

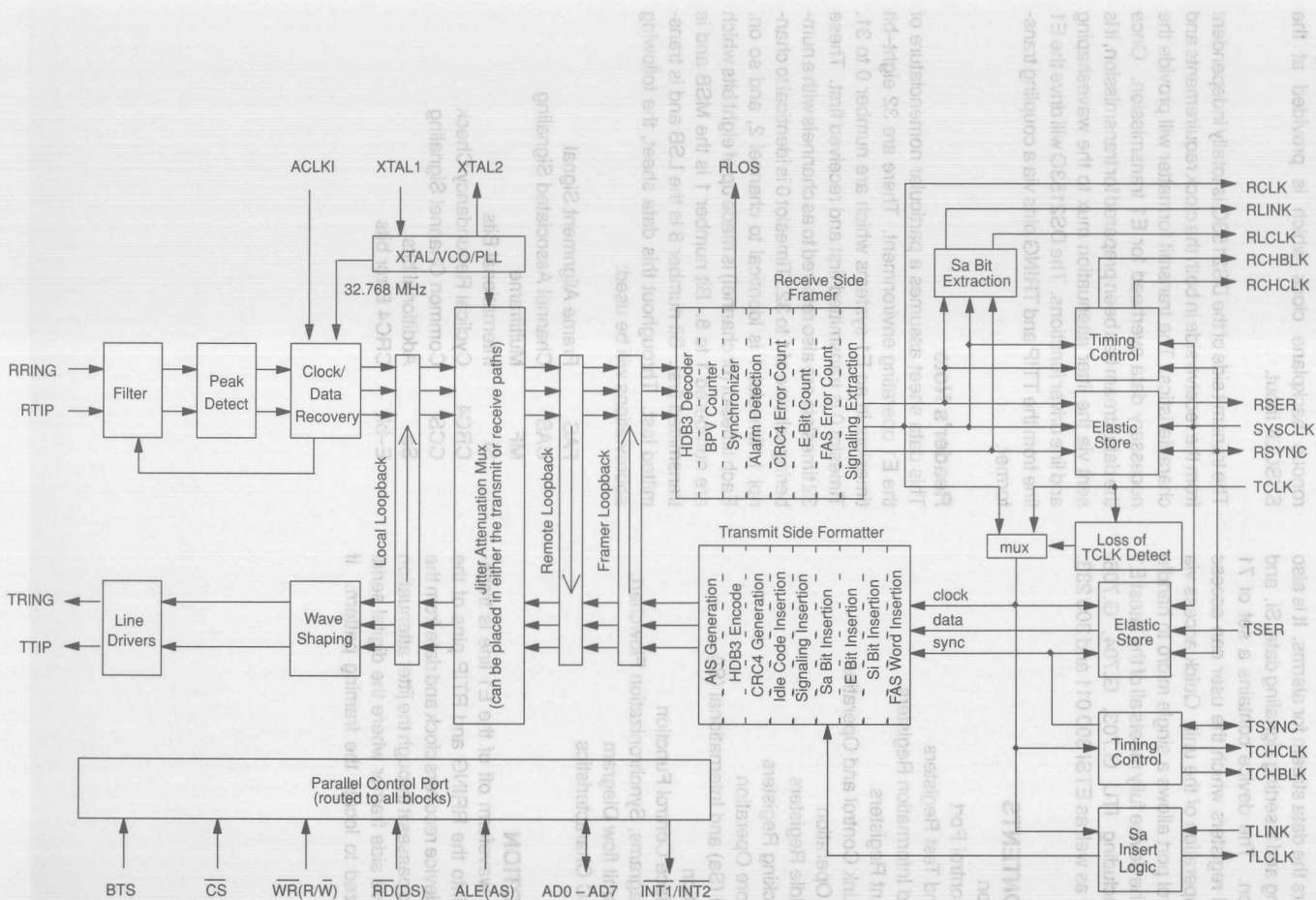
The transmit side of the DS2153Q is totally independent from the receive side in both the clock requirements and characteristics. The transmit formatter will provide the necessary data overhead for E1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2153Q will drive the E1 line from the TTIP and TRING pins via a coupling transformer.

Reader's Note

This data sheet assumes a particular nomenclature of the E1 operating environment. There are 32 eight-bit timeslots in an E1 systems which are number 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to channel 2, and so on. Each timeslot (or channel) is made up of eight bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment Signal
CAS	Channel Associated Signaling
MF	Multiframe
Si	International Bits
CRC4	Cyclical Redundancy Check
CCS	Common Channel Signaling
Sa	Additional bits
E-bit	CRC4 Error bits

DS2153Q BLOCK DIAGRAM Figure 1-1



1	AD4	I/O	Address/Data Bus. A 8-bit multiplexed address/data bus.
2	AD5		
3	AD6		
4	AD7		
5	$\overline{\text{RD}}(\text{DS})$	I	Read Input (Data Strobe).
6	$\overline{\text{CS}}$	I	Chip Select. Must be low to read or write the port.
7	ALE(AS)	I	Address Latch Enable (Address Strobe). A positive going edge serves to demultiplex the bus.
8	$\overline{\text{WR}}(\text{R/W})$	I	Write Input (Read/Write).
9	RLINK	O	Receive Link Data. Outputs the full receive data stream including the Sa bits. See Section 13 for timing details.
10	RLCLK	O	Receive Link Clock. 4 KHz to 20 KHz demand clock for the RLINK output; controlled by RCR2. See Section 13 for timing details.
11	DVSS	—	Digital Signal Ground. 0.0 volts. Should be tied to local ground plane.
12	RCLK	O	Receive Clock. Recovered 2.048 MHz clock.
13	RCHCLK	O	Receive Channel Clock. 256 KHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data. See Section 13 for timing details.
14	RSER	O	Receive Serial Data. Received NRZ serial data, updated on rising edges of RCLK or SYSCLK.
15	RSYNC	I/O	Receive Sync. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR1.6=0) or multiframe boundaries (RCR1.6=1). If the elastic store is enabled via the RCR2.1, then this pin can be enabled to be an input via RCR1.5 at which a frame boundary pulse is applied. See Section 13 for timing details.
16	RLOS/LOTC	O	Receive Loss of Sync/Loss of Transmit Clock. A dual function output. If TCR2.0=0, will toggle high when the synchronizer is searching for the E1 frame and multiframe; if TCR2.0=1, will toggle high if the TCLK pin has not toggled for 5 μs .
17	SYSCLK	I	System Clock. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store functions are enabled via RCR2.1. Should be tied low in applications that do not use the elastic store. If tied high for at least 100 μs , will force all output pins (including the parallel port) to 3-state.
18	RCHBLK	O	Receive Channel Block. A user programmable output that can be forced high or low during any of the 32 E1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384Kbps service (H0), 1920Kbps (H12), or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 13 for timing details.
19	ACLKI	I	Alternate Clock Input. Upon a receive carrier loss, the clock applied at this pin (normally 2.048 MHz) will be routed to the RCLK pin. If no clock is routed to this pin, then it should be tied to DVSS.

PIN	SYMBOL	TYPE	DESCRIPTION
20	BTS	I	Bus Type Select. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the \overline{RD} (DS), ALE(AS), and \overline{WR} (R/W) pins. If BTS=1, then these pins assume the function listed in parenthesis ().
21 22	RTIP RRING	—	Receive Tip and Ring. Analog inputs for clock recovery circuitry; connects to a 1:1 transformer (see Section 12 for details).
23	RVDD	—	Receive Analog Positive Supply. 5.0 volts. Should be tied to DVDD and TVDD pins.
24	RVSS	—	Receive Signal Ground. 0.0 volts. Should be tied to local ground plane
25 26	XTAL1 XTAL2	—	Crystal Connections. A pullable 8.192 MHz crystal must be applied to these pins. See Section 12 for crystal specifications.
27	$\overline{INT1}$	O	Receive Alarm Interrupt 1. Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
28	$\overline{INT2}$	O	Receive Alarm Interrupt 2. Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
29	TTIP	—	Transmit Tip. Analog line driver output; connects to a step-up transformer (see Section 12 for details).
30	TVSS	—	Transmit Signal Ground. 0.0 volts. Should be tied to local ground plane.
31	TVDD	—	Transmit Analog Positive Supply. 5.0 volts. Should be tied to DVDD and RVDD pins.
32	TRING	—	Transmit Ring. Analog line driver outputs; connects to a step-up transformer (see Section 12 for details).
33	TCHBLK	O	Transmit Channel Block. A user programmable output that can be forced high or low during any of the 32 E1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384Kbps service (H0), 1920Kbps (H12), or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 13 for timing details.
34	TLCLK	O	Transmit Link Clock. 4 KHz to 20 KHz demand clock for the TLINK input; controlled by TCR2. See Section 13 for timing details.
35	TLINK	I	Transmit Link Data. If enabled, this pin will be sampled on the falling edge of TCLK to insert the Sa bits. See Section 13 for timing details.
36	TSYNC	I/O	Transmit Sync. A pulse at this pin will establish either frame or multiframe boundaries for the DS2153Q. Via TCR1.1, the DS2153Q can be programmed to output either a frame or multiframe pulse at this pin. See Section 13 for timing details.
37	DVDD	—	Digital Positive Supply. 5.0 volts. Should be tied to RVDD and TVDD pins.
38	TCLK	I	Transmit Clock. 2.048 MHz primary clock.
39	TSER	I	Transmit Serial Data. Transmit NRZ serial data, sampled on the falling edge of TCLK.

PIN	SYMBOL	TYPE	DESCRIPTION
40	TCHCLK	O	Transmit Channel Clock. 256 KHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data. See Section 13 for timing details.
41	AD0	I/O	Address/Data Bus. A 8-bit multiplexed address/data bus.
42	AD1		
43	AD2		
44	AD3		

DS2153Q REGISTER MAP

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
00	R	BPV or Code Violation Count 1.	20	R/W	Transmit Align Frame.
01	R	BPV or Code Violation Count 2.	21	R/W	Transmit Non-Align Frame.
02	R	CRC4 Count 1/FAS Error Count 1.	22	R/W	Transmit Channel Blocking 1.
03	R	CRC4 Error Count 2.	23	R/W	Transmit Channel Blocking 2.
04	R	E-Bit Count 1/FAS Error Count 2.	24	R/W	Transmit Channel Blocking 3.
05	R	E-Bit Count 2.	25	R/W	Transmit Channel Blocking 4.
06	R	Status 1.	26	R/W	Transmit Idle 1.
07	R	Status 2.	27	R/W	Transmit Idle 2.
08	R/W	Receive Information.	28	R/W	Transmit Idle 3.
10	R/W	Receive Control 1.	29	R/W	Transmit Idle 4.
11	R/W	Receive Control 2.	2A	R/W	Transmit Idle Definition.
12	R/W	Transmit Control 1.	2B	R/W	Receive Channel Blocking 1.
13	R/W	Transmit Control 2.	2C	R/W	Receive Channel Blocking 2.
14	R/W	Common Control 1.	2D	R/W	Receive Channel Blocking 3.
15	R/W	Test 1.	2E	R/W	Receive Channel Blocking 4.
16	R/W	Interrupt Mask.	2F	R	Receive Align Frame.
17	R/W	Interrupt Mask.			
18	R/W	Line Interface Control.			
19	R/W	Test 2.			
1A	R/W	Common Control 2.			
1B	R/W	Common Control 3.			
1E	R	Synchronizer Status.			
1F	R	Receive Non-Align Frame.			

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
30	R	Receive Signaling 1.	40	R/W	Transmit Signaling 1.
31	R	Receive Signaling 2.	41	R/W	Transmit Signaling 2.
32	R	Receive Signaling 3.	42	R/W	Transmit Signaling 3.
33	R	Receive Signaling 4.	43	R/W	Transmit Signaling 4.
34	R	Receive Signaling 5.	44	R/W	Transmit Signaling 5.
35	R	Receive Signaling 6.	45	R/W	Transmit Signaling 6.
36	R	Receive Signaling 7.	46	R/W	Transmit Signaling 7.
37	R	Receive Signaling 8.	47	R/W	Transmit Signaling 8.
38	R	Receive Signaling 9.	48	R/W	Transmit Signaling 9.
39	R	Receive Signaling 10.	49	R/W	Transmit Signaling 10.
3A	R	Receive Signaling 11.	4A	R/W	Transmit Signaling 11.
3B	R	Receive Signaling 12.	4B	R/W	Transmit Signaling 12.
3C	R	Receive Signaling 13.	4C	R/W	Transmit Signaling 13.
3D	R	Receive Signaling 14.	4D	R/W	Transmit Signaling 14.
3E	R	Receive Signaling 15.	4E	R/W	Transmit Signaling 15.
3F	R	Receive Signaling 16.	4F	R/W	Transmit Signaling 16.

Note: the Test Registers 1 and 2 are used only by the factory; these registers must be cleared (set to all zeros) on power-up initialization to insure proper operation.

2.0 PARALLEL PORT

The DS2153Q is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2153Q can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the AC Electrical Characteristics for more details. The multiplexed bus on the DS2153Q saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the DS2153Q latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS WR pulses. In a read cycle, the DS2153Q outputs a byte of data during the latter portion of the DS or RD pulses. The read cycle is

terminated and the bus returns to a high impedance state as RD transitions high in Intel timing or as DS transitions low in Motorola timing.

3.0 CONTROL AND TEST REGISTERS

The operation of the DS2153Q is configured via a set of seven registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2153Q has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Register (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and three Common Control Registers (CCR1, CCR2 and CCR3). Each of the seven registers are described in this section.

The Test Registers at addresses 15 and 19 hex are used by the factory in testing the DS2153Q. On power-up, the Test Registers should be set to 00 hex in order for the DS2153Q to operate properly.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB)

(LSB)

RSMF	RSM	RSIO	—	—	FRC	SYNCE	RESYNC
------	-----	------	---	---	-----	-------	--------

SYMBOL	POSITION	NAME AND DESCRIPTION
RSMF	RCR1.7	RSYNC Multiframe Function. Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6=1). 0=RSYNC outputs CAS multiframe boundaries 1=RSYNC outputs CRC4 multiframe boundaries
RSM	RCR1.6	RSYNC Mode Select. 0=frame mode (see the timing in Section 13) 1=multiframe mode (see the timing in Section 13)
RSIO	RCR1.5	RSYNC I/O Select. 0=RSYNC is an output (depends on RCR1.6) 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to zero when RCR2.1=0)
—	RCR1.4	Not Assigned. Should be set to zero when written to.
—	RCR1.3	Not Assigned. Should be set to zero when written to.
FRC	RCR1.2	Frame Resync Criteria. 0=resync if FAS received in error 3 consecutive times 1=resync if FAS or bit 2 of non-FAS is received in error 3 consecutive times
SYNCE	RCR1.1	Sync Enable. 0=auto resync enabled 1=auto resync disabled
RESYNC	RCR1.0	Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

SYNC/RESYNC CRITERIA Table 3–1

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frames N and N + 2, and FAS not present in frame N + 1.	Three consecutive incorrect FAS received. Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non-FAS received.	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms.	915 or more CRC4 code words out of 1000 received in error.	G.706 4.2 4.3.2
CAS	Valid MP alignment word found and previous time slot 16 contains code other than all zeros.	Two consecutive MF alignment words received in error.	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB)				(LSB)			
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	RSCLKM	RESE	—

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	RCR2.7	Sa8 Bit Select. Set to one to report the Sa8 bit at the RLINK pin; set to zero to not report the Sa8 bit.
Sa7S	RCR2.6	Sa7 Bit Select. Set to one to report the Sa7 bit at the RLINK pin; set to zero to not report the Sa7 bit.
Sa6S	RCR2.5	Sa6 Bit Select. Set to one to report the Sa6 bit at the RLINK pin; set to zero to not report the Sa6 bit.
Sa5S	RCR2.4	Sa5 Bit Select. Set to one to report the Sa5 bit at the RLINK pin; set to zero to not report the Sa5 bit.
Sa4S	RCR2.3	Sa4 Bit Select. Set to one to report the Sa4 bit at the RLINK pin; set to zero to not report the Sa4 bit.
RSCLKM	RCR2.2	Receive Side SYSCLK Mode Select. 0=if SYSCLK is 1.544 MHz 1=if SYSCLK is 2.048 MHz
RESE	RCR2.1	Receive Side Elastic Store Enable. 0=elastic store is bypassed 1=elastic store is enabled
—	RCR2.0	Not Assigned. Should be set to zero when written to.

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)				(LSB)			
—	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOL	POSITION	NAME AND DESCRIPTION
—	TCR1.7	Not Assigned. Should be set to zero when written to.
TFPT	TCR1.6	Transmit Timeslot 0 Pass Through. 0=FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1=FAS bits/Sa bits/Remote Alarm sourced from TSER
T16S	TCR1.5	Transmit Timeslot 16 Data Select. 0=sample timeslot 16 at TSER pin 1=source timeslot 16 from TS1 to TS16 registers
TUA1	TCR1.4	Transmit Unframed All Ones. 0=transmit data normally 1=transmit an unframed all one's code at TPOS and TNEG
TSiS	TCR1.3	Transmit International Bit Select. 0=sample Si bits at TSER pin 1=source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)

TSA1	TCR1.2	Transmit Signaling All Ones. 0=normal operation 1=force timeslot 16 in every frame to all ones
TSM	TCR1.1	TSYNC Mode Select. 0=frame mode (see the timing in Section 13) 1=CAS and CRC4 multiframe mode (see the timing in Section 13)
TSIO	TCR1.0	TSYNC I/O Select. 0=TSYNC is an input 1=TSYNC is an output

Note: See Figure 13–9 for more details about how the Transmit Control Registers affect the operation of the DS2153Q.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)			(LSB)				
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	–	AEBE	P16F
SYMBOL	POSITION	NAME AND DESCRIPTION					
Sa8S	TCR2.7	Sa8 Bit Select. Set to one to source the Sa8 bit from the TLINK pin; set to zero to not source the Sa8 bit.					
Sa7S	TCR2.6	Sa7 Bit Select. Set to one to source the Sa7 bit from the TLINK pin; set to zero to not source the Sa7 bit.					
Sa6S	TCR2.5	Sa6 Bit Select. Set to one to source the Sa6 bit from the TLINK pin; set to zero to not source the Sa6 bit.					
Sa5S	TCR2.4	Sa5 Bit Select. Set to one to source the Sa5 bit from the TLINK pin; set to zero to not source the Sa5 bit.					
Sa4S	TCR2.3	Sa4 Bit Select. Set to one to source the Sa4 bit from the TLINK pin; set to zero to not source the Sa4 bit.					
–	TCR2.2	Not Assigned. Should be set to zero when written to.					
AEBE	TCR2.1	Automatic E–Bit Enable. 0=E–bits not automatically set in the transmit direction 1=E–bits automatically set in the transmit direction					
P16F	TCR2.0	Function of Pin 16. 0=Receive Loss of Sync (RLOS) 1=Loss of Transmit Clock (LOTCL)					

CCR1: COMMON CONTROL REGISTER 1 (Address=14 Hex)

(MSB)				(LSB)			
FLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4
SYMBOL	POSITION	NAME AND DESCRIPTION					
FLB	CCR1.7	Framer Loopback. 0=loopback disabled 1=loopback enabled					

THDB3	CCR1.6	Transmit HDB3 Enable. 0=HDB3 disabled 1=HDB3 enabled
TG802	CCR1.5	Transmit G.802 Enable. See Section 13 for details. 0=do not force TCHBLK high during bit 1 of timeslot 26 1=force TCHBLK high during bit 1 of timeslot 26
TCRC4	CCR1.4	Transmit CRC4 Enable. 0=CRC4 disabled 1=CRC4 enabled
RSM	CCR1.3	Receive Signaling Mode Select. 0=CAS signaling mode 1=CCS signaling mode
RHDB3	CCR1.2	Receive HDB3 Enable. 0=HDB3 disabled 1=HDB3 enabled
RG802	CCR1.1	Receive G.802 Enable. See Section 13 for details. 0=do not force RCHBLK high during bit 1 of timeslot 26 1=force RCHBLK high during bit 1 of timeslot 26
RCRC4	CCR1.0	Receive CRC4 Enable. 0=CRC4 disabled 1=CRC4 enabled

FRAMER LOOPBACK

When CCR1.7 is set to a one, the DS2153Q will enter a Framers LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS2153Q will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. data will be transmitted as normal at TTIP and TRING
2. data off the E1 line at RTIP and RRING will be ignored
3. the RCLK output will be replaced with the TCLK input.

CCR2: COMMON CONTROL REGISTER 2 (Address=1A Hex)

(MSB)				(LSB)			
ECUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	RLB	LLB
SYMBOL	POSITION	NAME AND DESCRIPTION					
ECUS	CCR2.7	Error Counter Update Select. 0=update error counters once a second 1=update error counters every 62.5 ms (500 frames)					
VCRFS	CCR2.6	VCR Function Select. 0=count BiPolar Violations (BPVs) 1=count Code Violations (CVs)					
AAIS	CCR2.5	Automatic AIS Generation. 0=disabled 1=enabled					
ARA	CCR2.4	Automatic Remote Alarm Generation. 0=disabled 1=enabled					

RSERC	CCR2.3	RSER Control. 0=allow RSER to output data as received under all conditions 1=force RSER to one under loss of frame alignment conditions
LOTCCMC	CCR2.2	Loss of Transmit Clock Mux Control. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK should fail to transition (see Figure 1.1). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
RLB	CCR2.1	Remote Loopback. 0=loopback disabled 1=loopback enabled
LLB	CCR2.0	Local Loopback. 0=loopback disabled 1=loopback enabled

REMOTE LOOPBACK

When CCR2.1 is set to a one, the DS2153Q will be forced into Remote LoopBack (RLB). In this loopback, data recovered off of the E1 line from the RTIP and RRING pins will be transmitted back onto the E1 line (with any BPV's that might have occurred intact) via the TTIP and TRING pins. Data will continue to pass through the receive side of the DS2153Q as it would normally and the data at the TSER pin will be ignored. Data in this loopback will pass through the jitter attenuator. Please see Figure 1.1 for more details.

LOCAL LOOPBACK

When CCR2.0 is set to a one, the DS2153Q will be forced into Local LoopBack (LLB). In this loopback, data will continue to be transmitted as normal through

the transmit side of the SCT. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator. Please see Figure 1.1 for more details.

AUTOMATIC ALARM GENERATION

When either CCR2.4 or CCR2.5 is set to one, the DS2153Q monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the DS2151Q will either force an AIS alarm (if CCR2.5=1) or a Remote Alarm (CCR2.4=1) to be transmitted via the TTIP and TRING pins. It is an illegal state to have both CCR2.4 and CCR2.5 set to one at the same time.

CCR3: COMMON CONTROL REGISTER 3 (Address=1B Hex)

(MSB)							(LSB)
TESE	TCBFS	TIRFS	ESR	LIRST	-	TSCLKM	-
SYMBOL	POSITION	NAME AND DESCRIPTION					
TESE	CCR3.7	Transmit Elastic Store Enable. 0 = elastic store is disabled. 1 = elastic store is enabled.					
TCBFS	CCR3.6	Transmit Channel Blocking Registers (TCBR) Function Select. 0=TCBRs define the operation of the TCHBLK output pin 1=TCBRs define which signaling bits are to be inserted					
TIRFS	CCR3.5	Transmit Idle Registers (TIR) Function Select. 0=TIRs define in which channels to insert idle code 1=TIRs define in which channels to insert data from RSER					
ESR	CCR3.4	Elastic Stores Reset. Setting this bit from a one to a zero will force the elastic stores to a known depth. Should be toggled after SYSCLK has been					

LIRST	CCR3.3	Line Interface Reset. Setting this bit from a zero to a one will initiate an internal reset that affects the slicer, AGC, clock recovery state machine, and jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.
—	CCR3.2	Not Assigned. Should be set to zero when written to.
TSCLKM	CCR3.1	Transmit Backplane Clock Select. Must be set like RCR2.2. 0 = 1.544 MHz 1 = 2.048 MHz
—	CCR3.0	Not Assigned. Should be set to zero when written to.

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS2153Q should be configured for operation by writing to all of the internal registers (this includes the Test Registers) since the contents of the internal registers cannot be predicted on power-up. Next, the LIRST bit should be toggled from zero to one to reset the line interface circuitry (it will take the DS2153Q about 40 ms to recover from the LIRST bit being toggled). Finally, after the SY-SCLK input is stable, the ESR bit should be toggled from a zero to a one and back to zero (this step can be skipped if the elastic store is not being used).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2153Q, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in these registers operate in a latched fashion (except for the SSR). This means that if an event occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm is still present.

The user will always precede a read of the SR1, SR2, and RIR registers with a write. The byte written to the register will inform the DS2153Q which bits the user wishes to read and have cleared. The user will write a

byte to one of these three registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2153Q with higher-order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this registers with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the INT1 and INT2 pins respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

RIR: RECEIVE INFORMATION REGISTER (Address=08 Hex)

(MSB)

(LSB)

TESF	TESE	JALT	RESF	RESE	CRCRC	FASRC	CASRC
------	------	------	------	------	-------	-------	-------

SYMBOL	POSITION	NAME AND DESCRIPTION
TESF	RIR.7	Transmit Elastic Store Full. Set when the elastic store fills and a frame is deleted.
TESE	RIR.6	Transmit Elastic Store Empty. Set when the elastic store empties and a frame is repeated.
JALT	RIR.5	Jitter Attenuator Limit Trip. Set when the jitter attenuator FIFO reaches to within 4-bits of it's limit; useful for debugging jitter attenuation operation.
RESF	RIR.4	Elastic Store Full. Set when the elastic store buffer fills and a frame is deleted.
RESE	RIR.3	Elastic Store Empty. Set when the elastic store buffer empties and a frame is repeated.
CRCRC	RIR.2	CRC Resync Criteria Met. Set when 915/1000 code words are received in error.
FASRC	RIR.1	FAS Resync Criteria Met. Set when three consecutive FAS words are received in error.
CASRC	RIR.0	CAS Resync Criteria Met. Set when two consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)

(LSB)

CSC5	CSC4	CSC3	CSC2	CSC1	FASSA	CASSA	CRC4SA
------	------	------	------	------	-------	-------	--------

SYMBOL	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	CRC4 Sync Counter Bit 5. MSB of the 6-bit counter.
CSC4	SSR.6	CRC4 Sync Counter Bit 4.
CSC3	SSR.5	CRC4 Sync Counter Bit 3.
CSC2	SSR.4	CRC4 Sync Counter Bit 2.
CSC1	SSR.3	CRC4 Sync Counter Bit 1. Next to LSB of the 6-bit counter. The LSB is not accessible.
FASSA	SSR.2	FAS Sync Active. Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	CAS MF Sync Active. Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	CRC4 MF Sync Active. Set while the synchronizer is searching for the CRC4 MF alignment word.

CRC4 SYNC COUNTER

The CRC4 Sync Counter increments each time the 8 ms CRC4 multiframe search times out. The counter is cleared when the DS2153Q has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0=0). This counter is useful for determining the

amount of time the DS2153Q has been searching for synchronization at the CRC4 level. Annex B of CCITT G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

SR1: STATUS REGISTER 1 (Address=06 Hex)

(MSB)				(LSB)			
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION					
RSA1	SR1.7	Receive Signaling All Ones. Set when the contents of timeslot 16 contains less than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.					
RDMA	SR1.6	Receive Distant MF Alarm. Set when bit 6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.					
RSA0	SR1.5	Receive Signaling All Zeros. Set when over a full MF, timeslot 16 contains all zeros.					
RSLIP	SR1.4	Receive Elastic Store Slip Occurrence. Set when the elastic store has either repeated or deleted a frame of data.					
RUA1	SR1.3	Receive Unframed All Ones. Set when an unframed all ones code is received at RTIP and RRING.					
RRA	SR1.2	Receive Remote Alarm. Set when a remote alarm is received at RTIP and RRING.					
RCL	SR1.1	Receive Carrier Loss. Set when 255 consecutive zeros have been detected at RTIP and RRING.					
RLOS	SR1.0	Receive Loss of Sync. Set when the device is not synchronized to the receive E1 stream.					

ALARM CRITERIA Table 4–1

ALARM	SET CRITERIA	CLEAR CRITERIA	CCITT SPEC.
RSA1 (receive signaling all ones)	over 16 consecutive frames (one full MF) timeslot 16 contains less than 3 zeros	over 16 consecutive frames (one full MF) timeslot 16 contains 3 or more zeros	G.732 4.2
RSA0 (receive signaling all zeros)	over 16 consecutive frames (one full MF) timeslot 16 contains all zeros	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to one for two consecutive MF	bit 6 in timeslot 16 of frame 0 set to zero for a two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all ones)	less than 3 zeros in two frames (512 bits)	more than 2 zeros in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non-align frame set to one for 3 consecutive occasions	bit 3 of non-align frame set to zero for 3 consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 consecutive zeros received	in 255 bit times, at least 32 ones are received	G.775

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB)				(LSB)			
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	Receive CAS Multiframe. Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	Receive Align Frame. Set every 250 μ s at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	Transmit Multiframe. Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	One Second Timer. Set on increments of one second based on RCLK. If CCR2.7=1, then this bit will be set every 62.5 ms instead of once a second.
TAF	SR2.3	Transmit Align Frame. Set every 250 μ s at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.
LOTC	SR2.2	Loss of Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 3.9 μ s). Will force pin 16 high if enabled via TCR2.0. Based on RCLK.
RCMF	SR2.1	Receive CRC4 Multiframe. Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.
TSLIP	SR2.0	Transmit Elastic Store Slip. Set when the elastic store has either repeated or deleted a frame of data.

IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)

(MSB)				(LSB)			
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS
SYMBOL	POSITION	NAME AND DESCRIPTION					
RSA1	IMR1.7	Receive Signaling All Ones. 0=interrupt masked 1=interrupt enabled					
RDMA	IMR1.6	Receive Distant MF Alarm. 0=interrupt masked 1=interrupt enabled					
RSA0	IMR1.5	Receive Signaling All Zeros. 0=interrupt masked 1=interrupt enabled					
RSLIP	IMR1.4	Receive Elastic Store Slip Occurrence. 0=interrupt masked 1=interrupt enabled					
RUA1	IMR1.3	Receive Unframed All Ones. 0=interrupt masked 1=interrupt enabled					
RRA	IMR1.2	Receive Remote Alarm. 0=interrupt masked 1=interrupt enabled					
RCL	IMR1.1	Receive Carrier Loss. 0=interrupt masked 1=interrupt enabled					
RLOS	IMR1.0	Receive Loss of Sync. 0=interrupt masked 1=interrupt enabled					

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)				(LSB)			
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP
SYMBOL	POSITION	NAME AND DESCRIPTION					
RMF	IMR2.7	Receive CAS Multiframe. 0=interrupt masked 1=interrupt enabled					
RAF	IMR2.6	Receive Align Frame. 0=interrupt masked 1=interrupt enabled					
TMF	IMR2.5	Transmit Multiframe. 0=interrupt masked 1=interrupt enabled					
SEC	IMR2.4	One Second Timer. 0=interrupt masked 1=interrupt enabled					
TAF	IMR2.3	Transmit Align Frame. 0=interrupt masked 1=interrupt enabled					
LOTC	IMR2.2	Loss Of Transmit Clock. 0=interrupt masked 1=interrupt enabled					
RCMF	IMR2.1	Receive CRC4 Multiframe. 0=interrupt masked 1=interrupt enabled					
TSLIP	IMR2.0	Transmit Side Elastic Store Slip. 0 = interrupt masked 1 = interrupt enabled					

5.0 ERROR COUNT REGISTERS

There are a set of four counters in the DS2153Q that record bipolar or code violations, errors in the CRC4 SMF code words, E-bits as reported by the far end, and word errors in the FAS. Each of these four counters are automatically updated on either one second boundaries (CCR2.7=0) or every 62.5 ms (CCR2.7=1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 62.5 ms. The user can use the interrupt from the timer to determine when to read these registers. The user has a full second (or 62.5 ms) to read the counters before the data is lost.

5.1 BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a

16-bit counter that records either BiPolar Violations (BPVs) or Code Violations (CVs). If CCR2.6=0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side via CCR1.2, then HDB3 code words are not counted as BPVs. If CCR2.6=1, then the VCR counts code violations as defined in CCITT O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the DS2153Q should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on a E1 line would have to be greater than 10⁻² before the VCR would saturate.

VCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)

VCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address=01 Hex)

(MSB)				(LSB)				
V15	V14	V13	V12	V11	V10	V9	V8	VCR1
V7	V6	V5	V4	V3	V2	V1	V0	VCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
V15	VCR1.7	MSB of the 16-bit bipolar or code violation count
V0	VCR2.0	LSB of the 16-bit bipolar or code violation count

5.2 CRC4 Error Counter

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 10-bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

CRCCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)

CRCCR2: CRC4 COUNT REGISTER 2 (Address=03 Hex)

(MSB)				(LSB)				
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	CRC9	CRC8	CRCCR1
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC9	CRCCR1.1	MSB of the 10-bit CRC4 error count
CRC0	CRCCR2.0	LSB of the 10-bit CRC4 error count

NOTES:

1. The upper six bits of CRCCR1 at address 02 are the most significant bits of the 12-bit FAS error counter.

5.3 E-Bit Counter

E-bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 10-bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E-bit is set to zero. Since the maximum E-bit count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

EBCR1: E-BIT COUNT REGISTER 1 (Address=04 Hex)**EBCR2: E-BIT COUNT REGISTER 2** (Address=05 Hex)

(MSB)						(LSB)		
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	EB9	EB8	EBCR1
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
EB9	EBCR1.1	MSB of the 10-bit E-Bit count
EB0	EBCR2.0	LSB of the 10-bit E-Bit count

NOTES:

1. The upper six bits of EBCR1 at address 04 are the least significant bits of the 12-bit FAS error counter.

5.4 FAS Bit Error Counter

FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 12-bit counter that records word errors in the Frame Alignment Signal in timeslot 0. This counter is disabled

during loss of frame synchronization conditions, it is not disabled during loss of synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one second period is 4000, this counter cannot saturate.

FASCR1: FAS BIT COUNT REGISTER 1 (Address=02 Hex)**FASCR2: FAS BIT COUNT REGISTER 2** (Address=04 Hex)

(MSB)						(LSB)		
FAS11	FAS10	FAS9	FAS8	FAS7	FAS6	(note 2)	(note 2)	FASCR1
FAS5	FAS4	FAS3	FAS2	FAS1	FAS0	(note 1)	(note 1)	FASCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
FAS11	FASCR1.7	MSB of the 12-bit FAS error count
FAS0	FASCR2.2	LSB of the 12-bit FAS error count

NOTES:

1. The lower two bits of FASCR1 at address 02 are the most significant bits of the 10-bit CRC4 error counter.
2. The lower two bits of FASCR2 at address 04 are the most significant bits of the 10-bit E-Bit counter.

6.0 Sa DATA LINK CONTROL AND OPERATION

The DS2153Q provides for access to the proposed E1 performance monitor data link in the Sa bit positions. The device allows access to the Sa bits either via a set of two internal registers (RNAF and TNAF) or via two external pins (RLINK and TLINK).

On the receive side, the Sa bits are always reported in the internal RNAF register (see Section 11 for more

details). All five Sa bits are always output at the RLINK pin. See Section 13 for detailed timing. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (TCR1.6=0) or from the external TLINK pin. Via TCR2, the DS2153Q can be programmed to source any combination of the

additional bits from the TLINK pin. If the user wishes to pass the Sa bits through the DS2153Q without them being altered, then the device should be set up to source all five Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Please see the timing diagrams and the transmit data flow diagram in Section 13 for examples.

7.0 SIGNALING OPERATION

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the

receive stream and inserted into the transmit stream by the DS2153Q. Each of the 30 channels has four signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the channel associated with a particular signaling bit. The channel numbers have been assigned as described in the CCITT documents. For example, channel 1 is associated with timeslot 1 and channel 30 is associated with timeslot 31. There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB)				(LSB)				
0	0	0	0	X	Y	X	X	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(31)	B(31)	C(31)	D(31)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(32)	B(32)	C(32)	D(32)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(33)	B(33)	C(33)	D(33)	RS4 (33)
A(4)	B(4)	C(4)	D(4)	A(34)	B(34)	C(34)	D(34)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(35)	B(35)	C(35)	D(35)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(36)	B(36)	C(36)	D(36)	RS7 (36)
A(7)	B(7)	C(7)	D(7)	A(37)	B(37)	C(37)	D(37)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(38)	B(38)	C(38)	D(38)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(39)	B(39)	C(39)	D(39)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(40)	B(40)	C(40)	D(40)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(41)	B(41)	C(41)	D(41)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(42)	B(42)	C(42)	D(42)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(43)	B(43)	C(43)	D(43)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(44)	B(44)	C(44)	D(44)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(45)	B(45)	C(45)	D(45)	RS16 (3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	Spare Bits
Y	RS1.2	Remote Alarm Bit (integrated and reported in SR1.6)
A(1)	RS2.7	Signaling Bit A for Channel 1
D(30)	RS16.0	Signaling Bit D for Channel 30

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling from two timeslots. The bits in the Receive Signaling Registers are updated on multi-frame boundaries so the user can utilize the Receive

Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all

conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be

informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)				(LSB)				
0	0	0	0	X	Y	X	X	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	Spare Bits
Y	TS1.2	Remote Alarm Bit
A(1)	TS2.7	Signaling Bit A for Channel 1
D(30)	TS16.0	Signaling Bit D for Channel 30

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the DS2153Q will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSR's before the old data will be retransmitted.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper nibble must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.5 bit should be set to a one. If no alarm is to be transmitted, then the TS1.5 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to one. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user

will be informed when the signaling registers need to be loaded with data. The user has 2 ms to load the data before the old data will be retransmitted. Via the CCR3.6 bit, the user has the option to use the Transmit Channel Blocking Registers (TCBRs) to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBRs=0). See the

Transmit Data Flow diagram in Section 13 for more details.

8.0 TRANSMIT IDLE REGISTERS

There is a set of five registers in the DS2153Q that can be used to custom tailor the data that is to be transmitted onto the E1 line, on a channel by channel basis. Each of the 32 E1 channels can be forced to have a user defined idle code inserted into them.

TIR1/TIR2/TIR3/TIR4: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TIR4.7	Transmit Idle Registers. 0=do not insert the Idle Code into this channel 1=insert the Idle Code into this channel
CH1	TIR1.0	

NOTE:

If CCR3.5=1, then a zero in the TIRs implies that channel data is to be sourced from TSER and a one implies that channel data is to be sourced from the RSER pin.

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)				(LSB)			
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code
TIDR0	TIDR.0	LSB of the Idle Code

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represent a timeslot in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). In the TIDR, the MSB is transmitted first. Via the CCR3.5 bit, the user has the option to use the TIRs to determine on a channel by channel basis, if data from the RSER pin should be substituted for data from the TSER pin. In this

mode, if the corresponding bit in the TIRs is set to one, then data will be sourced from the RSER pin. If the corresponding bit in the TIRs is set to zero, then data for that channel will sourced from the TSER pin. See the Transmit Data Flow diagram in Section 13 for more details.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3/RCBR4) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHCLK pins will be held

high during the entire corresponding channel time. See the timing in Section 13 for an example. The TCBRS have alternate mode of use. Via the CCR3.6 bit, the user has the option to use the TCBRS to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRS=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBR=0). See the Transmit Data Flow diagram in Section 13 for more details.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS

(Address=2B to 2E Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	RCBR4.7	Receive Channel Blocking Registers. 0=force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1=force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS

(Address=22 to 25 Hex)

(MSB)				(LSB)				
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TCBR4.7	Transmit Channel Blocking Registers. 0=force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1=force the TCHBLK pin high during this channel time

NOTE:

If CCR3.6=1, then a zero in the TCBRS implies that signaling data is to be sourced from TSER and a one implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See definition below.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6 = 1

(MSB)				(LSB)				
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4

* = CH1 and CH17 should be set to one to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

10.0 ELASTIC STORE OPERATION

The DS2153Q has an onboard two frame (512 bits) elastic store. This elastic store can be enabled via RCR2.1. If the elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2=0) or 2.048 MHz (RCR2.2=1) clock at the SYSCLK pin. If the elastic store is enabled, then the user has the option of either providing a frame sync at the RFSYNC pin (RCR1.5=1) or having the RFSYNC pin provide a pulse on frame or multiframe boundaries (RCR1.5=0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to one. If the user selects to apply a 1.544 MHz clock to the SYSCLK pin, then every fourth channel will be deleted and the F-bit position inserted (forced to one). Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted. Also, in 1.544 MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). See Section 13 for more details. If the 512-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

11.0 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS2153Q provides for access to both the Additional (Sa) and International (Si) bits. On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 μ s to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 μ s to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the DS2153Q is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to one. Please see the register descriptions for TCR1 and TCR2 and the Transmit Data Flow diagram in Section 13 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB)				(LSB)			
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
--------	----------	----------------------

Si	RAF.7	International Bit.
0	RAF.6	Frame Alignment Signal Bit.
0	RAF.5	Frame Alignment Signal Bit.
1	RAF.4	Frame Alignment Signal Bit.
1	RAF.3	Frame Alignment Signal Bit.
0	RAF.2	Frame Alignment Signal Bit.
1	RAF.1	Frame Alignment Signal Bit.
1	RAF.0	Frame Alignment Signal Bit.

RNAF: RECEIVE NON-ALIGN FRAME REGISTER (Address=1F Hex)

(MSB)				(LSB)			
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
--------	----------	----------------------

Si	RNAF.7	International Bit.
1	RNAF.6	Frame Non-Alignment Signal Bit.
A	RNAF.5	Remote Alarm.
Sa4	RNAF.4	Additional Bit 4.
Sa5	RNAF.3	Additional Bit 5.
Sa6	RNAF.2	Additional Bit 6.
Sa7	RNAF.1	Additional Bit 7.
Sa8	RNAF.0	Additional Bit 8.

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB)				(LSB)			
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
--------	----------	----------------------

Si	TAF.7	International Bit.
0	TAF.6	Frame Alignment Signal Bit.
0	TAF.5	Frame Alignment Signal Bit.
1	TAF.4	Frame Alignment Signal Bit.

1	TAF.3	Frame Alignment Signal Bit.
0	TAF.2	Frame Alignment Signal Bit.
1	TAF.1	Frame Alignment Signal Bit.
1	TAF.0	Frame Alignment Signal Bit.

TNAF: TRANSMIT NON-ALIGN FRAME REGISTER (Address=21 Hex)

(MSB)				(LSB)			
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
SYMBOL	POSITION	NAME AND DESCRIPTION					
Si	TNAF.7	International Bit.					
1	TNAF.6	Frame Non-Alignment Signal Bit.					
A	TNAF.5	Remote Alarm.					
Sa4	TNAF.4	Additional Bit 4.					
Sa5	TNAF.3	Additional Bit 5.					
Sa6	TNAF.2	Additional Bit 6.					
Sa7	TNAF.1	Additional Bit 7.					
Sa8	TNAF.0	Additional Bit 8.					

12.0 LINE INTERFACE FUNCTIONS

The line interface function in the DS2153Q contains three sections; (1) the receiver which handles clock and data recovery, (2) the transmitter which waveshapes

and drives the E1 line, and (3) the jitter attenuator. Each of these three sections is controlled by the Line Interface Control Register (LICR) which is described below.

LICR: LINE INTERFACE CONTROL REGISTER (Address=18 Hex)

(MSB)				(LSB)			
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD
SYMBOL	POSITION	NAME AND DESCRIPTION					
LB2	LICR.7	Line Build Out Bit 2. Transmit waveshape setting; see Table 12.2.					
LB1	LICR.6	Line Build Out Bit 1. Transmit waveshape setting; see Table 12.2.					
LB0	LICR.5	Line Build Out Bit 0. Transmit waveshape setting; see Table 12.2. 0=75 ohm COAX (2.37V _{peak} pulse) 1=120 ohm shielded twisted pair (3.00V _{peak} pulse)					
EGL	LICR.4	Receive Equalizer Gain Limit. 0 = -12 dB 1 = -30 dB					
JAS	LICR.3	Jitter Attenuator Select. 0=place the jitter attenuator on the receive side 1=place the jitter attenuator on the transmit side					

JABDS	LICR.2	Jitter Attenuator Buffer Depth Select .
		0=128 bits
		1=32 bits (use for delay sensitive applications)
DJA	LICR.1	Disable Jitter Attenuator.
		0=jitter attenuator enabled
		1=jitter attenuator disabled
TPD	LICR.0	Transmit Power Down.
		0=normal transmitter operation
		1=powers down the transmitter and 3-states the TTIP and TRING pins

12.1 Receive Clock and Data Recovery

The DS2153Q contains a digital clock recovery system. See the DS2153Q Block Diagram in Section 1 and Figure 12.1 for more details. The DS2153Q couples to the receive E1 shielded twisted pair or COAX via a 1:1 transformer. See Table 12.3 for transformer details. The DS2153Q automatically adjusts to the E1 signal being received at the RTIP and RRING pins and can handle E1 twisted pair cables of 0.6 mm (22 AWG) from 0 to 1.5 KM in length. The crystal attached at the XTAL1 and XTAL2 pins is multiplied by four via an internal PLL and fed to the clock recovery system. The clock recovery system uses both edges of the clock from the PLL circuit to form a 32 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance (see Figure 12.2).

Normally, the clock that is output at the RCLK pin is the recovered clock from the E1 AMI/HDB3 waveform pres-

ented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK can be sourced from either the ACLKI pin or from the crystal attached to the XTAL1 and XTAL2 pins. The DS2153Q will sense the ACLKI pin to determine if a clock is present. If no clock is applied to the ACLKI pin, then it should be tied to RVSS to prevent the device from falsely sensing a clock. See Table 12.1. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit short high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. Please see the Receive AC Timing Characteristics in Section 14 for more details.

SOURCE OF RCLK UPON RCL Table 12-1

ACLKI PRESENT?	RECEIVE SIDE JITTER ATTENUATOR	TRANSMIT SIDE JITTER ATTENUATOR
yes	ACLKI via the jitter attenuator	ACLKI
no	centered crystal	TCLK via the jitter attenuator

12.2 Transmit Waveshaping and Line Driving

The DS2153Q uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the E1 line. The waveforms created by the DS2153Q meet the ITU specifications. See Figure 12.3. The user

will select which waveform is to be generated by properly programming the L2/L1/L0 bits in the Line Interface Control Register (LICR). The DS2153Q can set up in a number of various configurations depending on the application. See Table 12.2 and Figure 12.1.

LINE BUILD OUT SELECT IN LICR Table 12-2

L2	L1	L0	APPLICATION	TRANSFORMER	RETURN LOSS	Rt
0	0	0	75 ohm normal	1:1.15 step-up	NM	0 ohms
0	0	1	120 ohm normal	1:1.15 step-up	NM	0 ohms
0	1	0	75 ohm normal with protection resistors	1:1.15 step-up	NM	8.2 ohms
0	1	1	120 ohm normal with protection resistors	1:1.15 step-up	NM	8.2 ohms
1	0	0	75 ohm with high return loss	1:1.15 step-up	21 dB	27 ohms
1	1	0	75 ohm with high return loss	1:1.36 step-up	21 dB	18 ohms
1	0	0	120 ohm with high return loss	1:1.36 step-up	21 dB	27 ohms

NM=Not Meaningful

Due to the nature of the design of the transmitter in the DS2153Q, very little jitter (less than 0.005UIpp broadband from 10Hz to 100 KHz) is added to the jitter present on TCLK. Also, the waveforms that they create are independent of the duty cycle of TCLK. The transmitter in the DS2153Q couples to the E1 transmit shielded

twisted pair or COAX via a 1:1.15 or 1:1.36 step up transformer as shown in Figure 12.1. In order for the devices to create the proper waveforms, this transformer used must meet the specifications listed in Table 12.3.

TRANSFORMER SPECIFICATIONS Table 12.3

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:1.15 or 1:1.36 (transmit) ±5%
Primary Inductance	600 µH minimum
Leakage Inductance	1.0 µH maximum
Interwinding Capacitance	40 pF maximum
DC Resistance	1.2 ohms maximum

12.3 Jitter Attenuator

The DS2153Q contains an onboard jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128 bit mode is used in applications where large excursions of wander are expected. The 32 bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 12.4. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit in the

LICR. In order for the jitter attenuator to operate properly, a crystal with the specifications listed in Table 12.4 below must be connected to the XTAL1 and XTAL2 pins.

The jitter attenuator divides the clock provided by the 8.192 MHz crystal at the XTAL1 and XTAL2 pins by to create an output clock that contains very little jitter. Onboard circuitry will pull the crystal (by switching in or out load capacitance) to keep it long term averaged to the same frequency as the incoming E1 signal. If the incoming jitter exceeds either 120UIpp (buffer depth is 128 bits) or 28UIpp (buffer depth is 32bits), then the

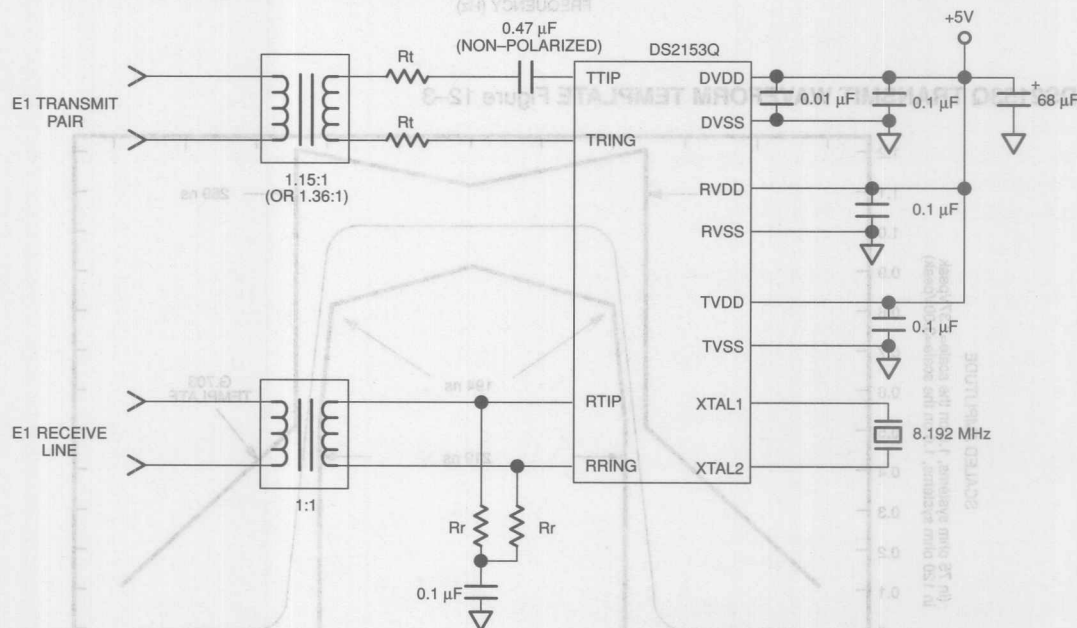
DS2153Q will divide the attached crystal by either 3.5 or 4.5 instead of the normal 4 to keep the buffer from overflowing. When the device divides by either 3.5 or 4.5, it

also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register (RIR.5).

CRYSTAL SELECTION GUIDELINES Table 12-4

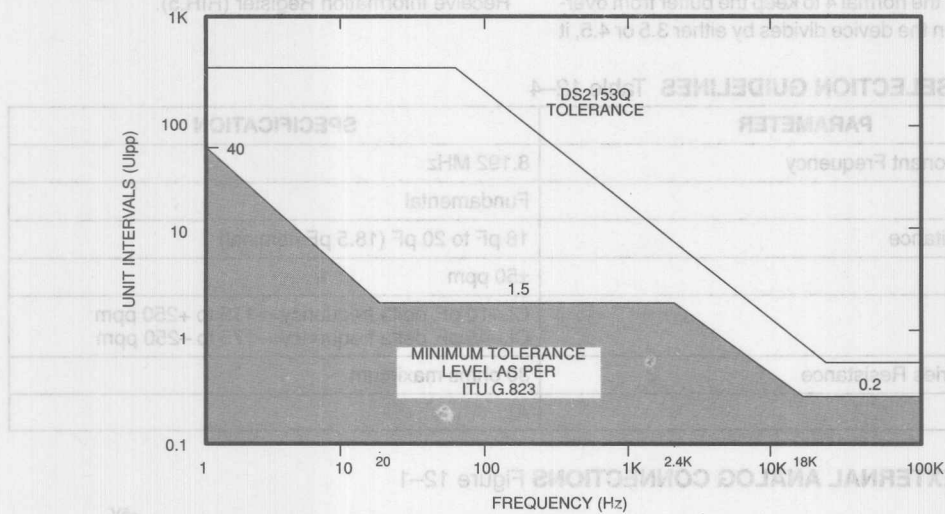
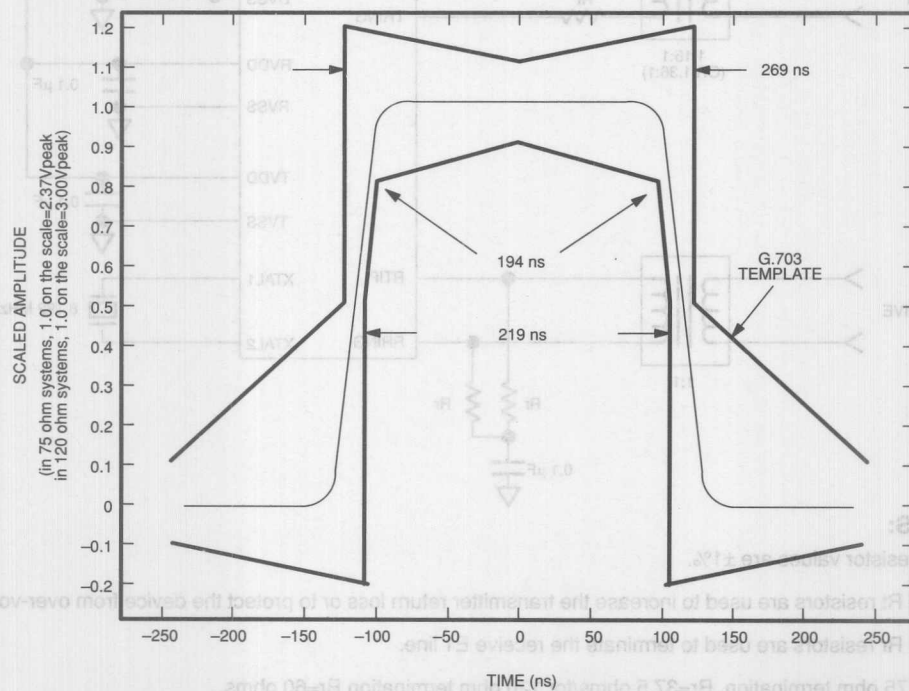
PARAMETER	SPECIFICATION
Parallel Resonant Frequency	8.192 MHz
Mode	Fundamental
Load Capacitance	18 pF to 20 pF (18.5 pF nominal)
Tolerance	±50 ppm
Pullability	CL=10 pF, delta frequency=+175 to +250 ppm CL=45 pF, delta frequency=-175 to -250 ppm
Effective Series Resistance	30 ohms maximum
Crystal Cut	AT

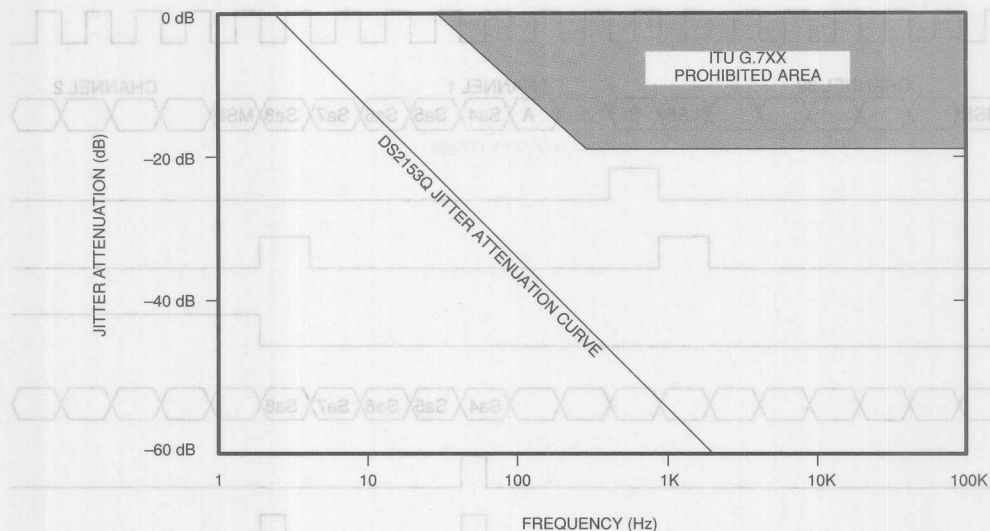
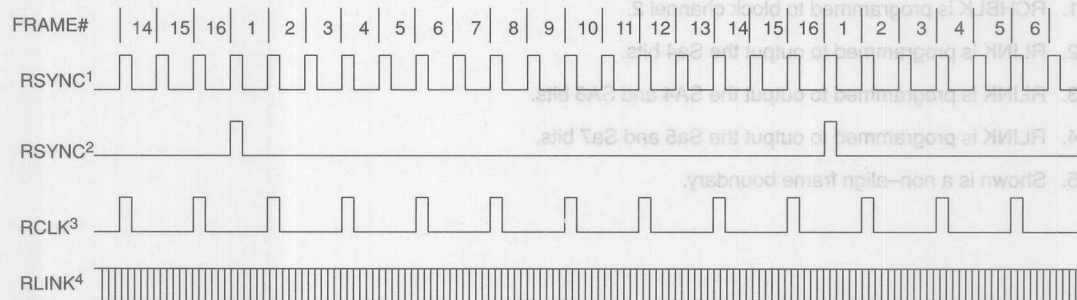
DS2153Q EXTERNAL ANALOG CONNECTIONS Figure 12-1



NOTES:

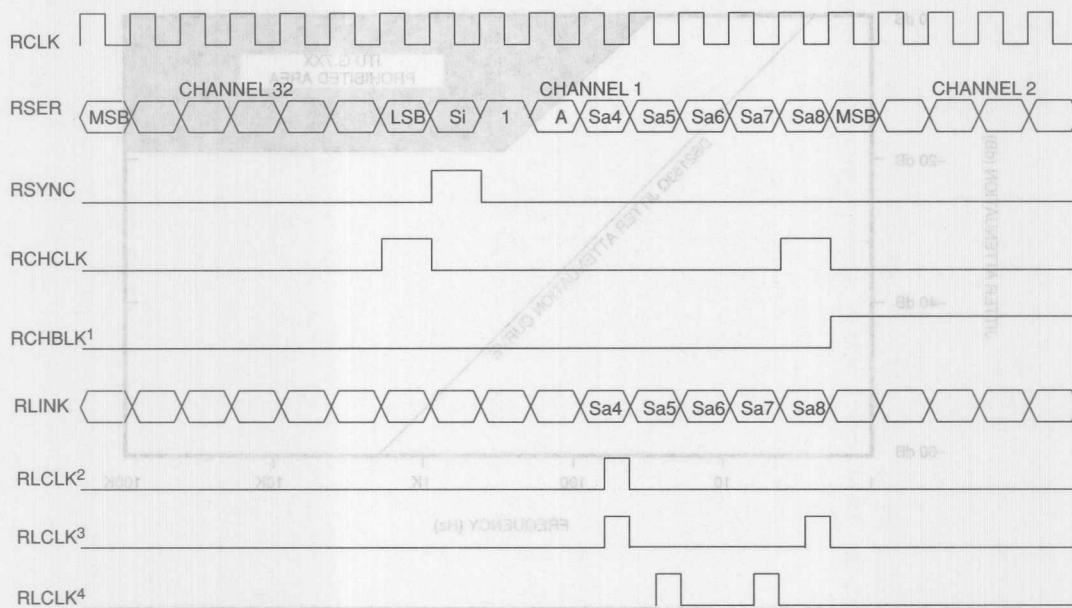
1. All resistor values are ±1%.
2. The Rt resistors are used to increase the transmitter return loss or to protect the device from over-voltage.
3. The Rr resistors are used to terminate the receive E1 line.
4. For 75 ohm termination, Rr=37.5 ohms/for 120 ohm termination Rr=60 ohms.
5. See the separate Application Note for details on how to construct a protected interface.

DS2153Q JITTER TOLERANCE Figure 12-2**DS2153Q TRANSMIT WAVEFORM TEMPLATE** Figure 12-3

DS2153Q JITTER ATTENUATION Figure 12-4**13.0 TIMING DIAGRAMS/SYNCHRONIZATION FLOWCHART/TRANSMIT DATA FLOW DIAGRAM****RECEIVE SIDE TIMING** Figure 13-1**NOTES:**

1. RSYNC in the frame mode (RCR1.6=0).
2. RSYNC in the multiframe mode (RCR1.6=1).
3. RCLK is programmed to output just the Sa4 bit.
4. RLINK will always output all five Sa bits as well as the rest of the receive data stream.
5. This diagram assumes the CAS MF begins with the FAS word.

RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORES DISABLED) Figure 13-2



NOTES:

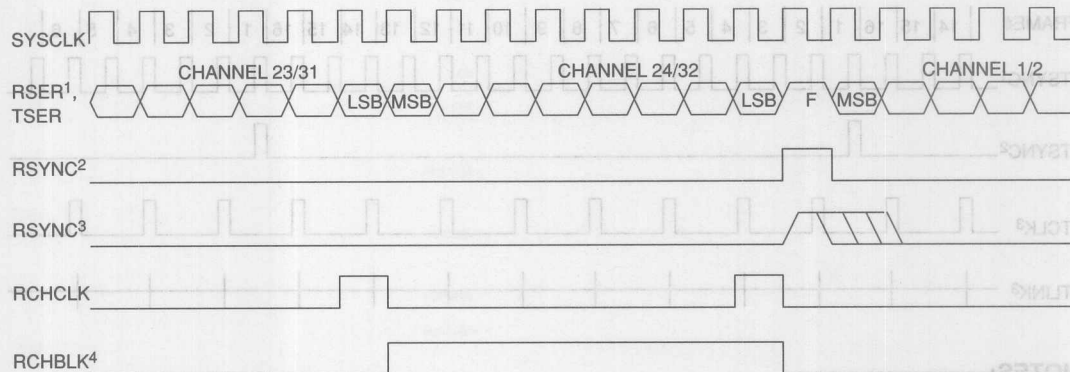
1. RCHBLK is programmed to block channel 2.
2. RLINK is programmed to output the Sa4 bits.
3. RLINK is programmed to output the SA4 and SA8 bits.
4. RLINK is programmed to output the Sa5 and Sa7 bits.
5. Shown is a non-align frame boundary.

RLINK

NOTES:

1. RSYNC in the frame mode (RCR1.8=0).
2. RSYNC in the multiframe mode (RCR1.8=1).
3. RCLK is programmed to output just the Sa4 bit.
4. RLINK will always output all five Sa bits as well as the rest of the receive data stream.
5. This diagram assumes the CAS MP begins with the FAS word.

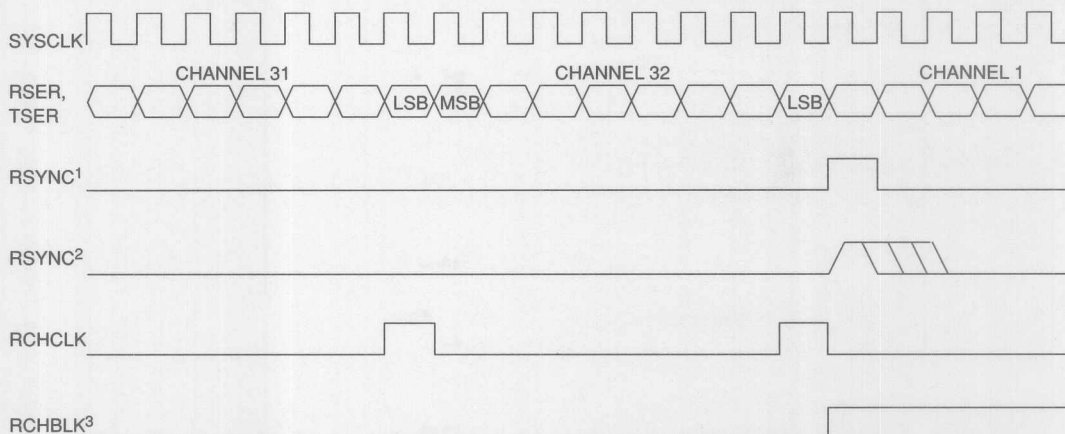
1.544 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED Figure 13–3



NOTES:

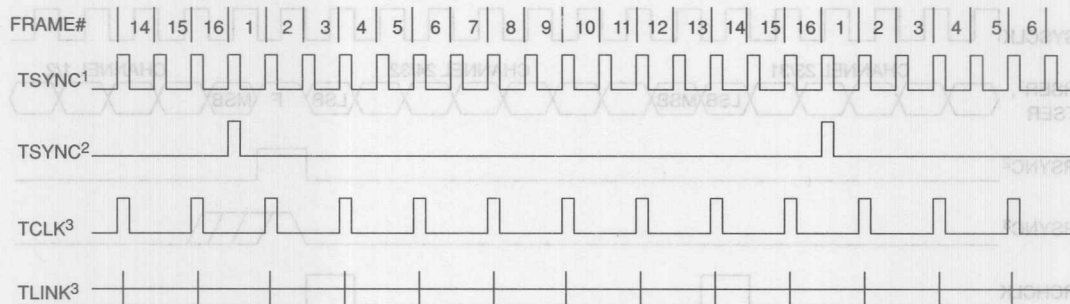
1. Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to one).
2. RSYNC is in the output mode (RCR1.5=0).
3. RSYNC is in the input mode (RCR1.5=1).
4. RCHBLK is programmed to block channel 24.

2.048 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED Figure 13–4

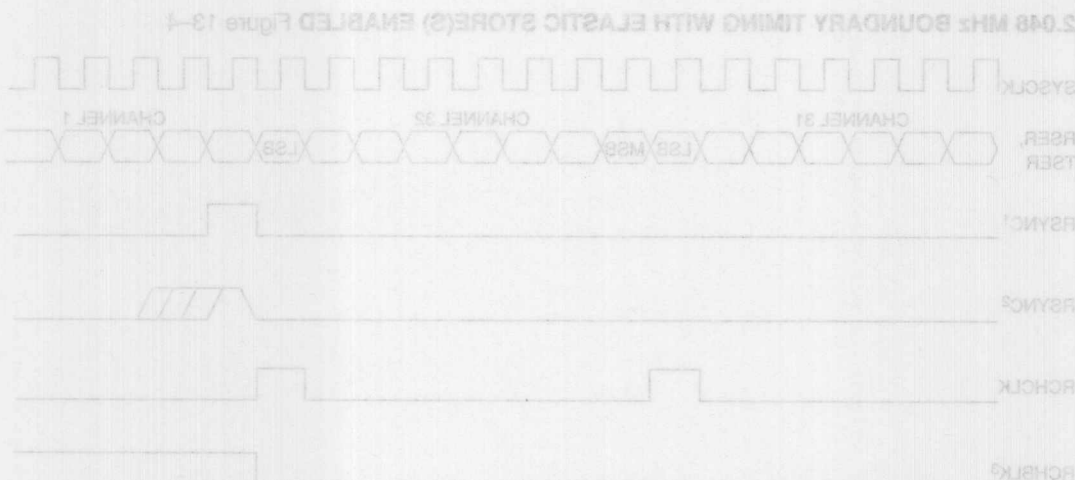


NOTES:

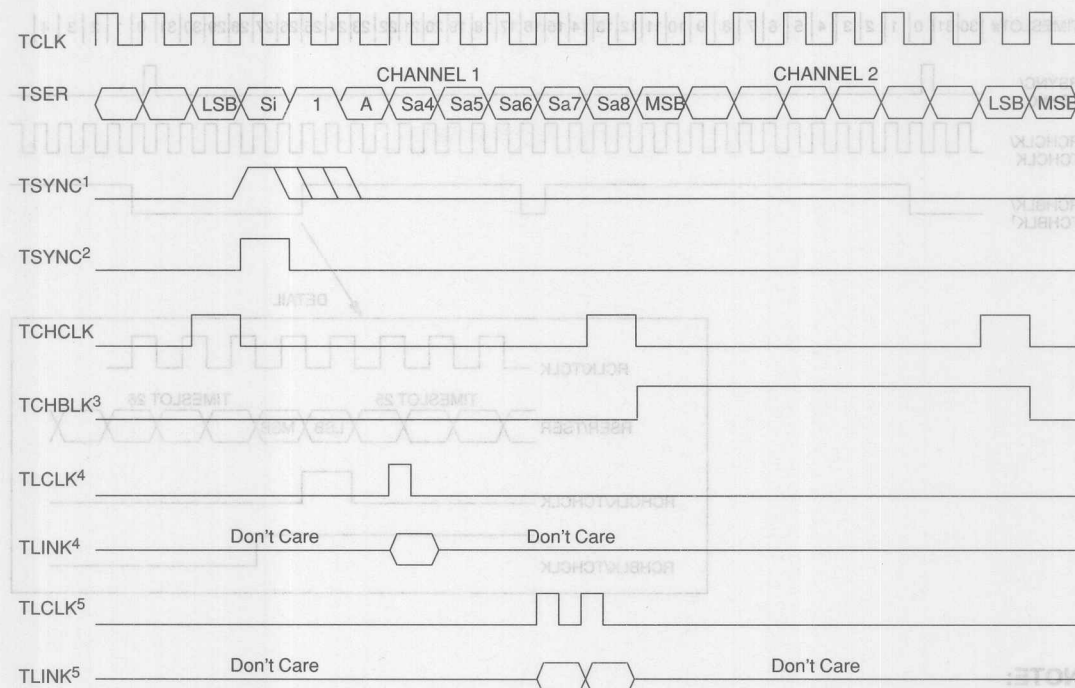
1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RCHBLK is programmed to block channel 1.

TRANSMIT SIDE TIMING Figure 13-5**NOTES:**

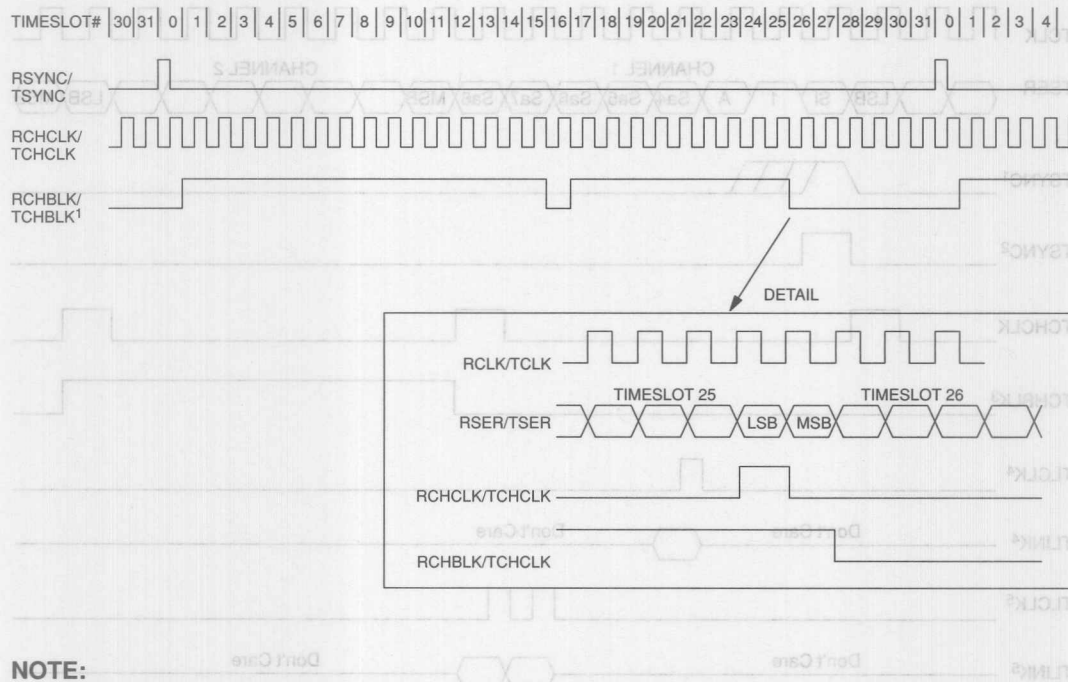
1. TSYNC in the frame mode (TCR1.1=0).
2. TSYNC in the multiframe mode (TCR1.1=1).
3. TLINK is programmed to source only the Sa4 bit.
4. This diagram assumes both the CAS MF and the CRC4 begin with the align frame.

**NOTES:**

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RCLK is programmed to block channel 1.

TRANSMIT SIDE BOUNDARY TIMING Figure 13–6**NOTES:**

1. TSYNC is in the input mode (TCR1.0=0).
2. TSYNC is in the output mode (TCR1.0=1).
3. TCHBLK is programmed to block channel 2.
4. TLINK is programmed to source the Sa4 bits.
5. TLINK is programmed to source the Sa7 and Sa8 bits.
6. Shown is a non-align frame boundary.
7. See Figures 13.3 and 13.4 for details on timing with the transmit side elastic store enabled.

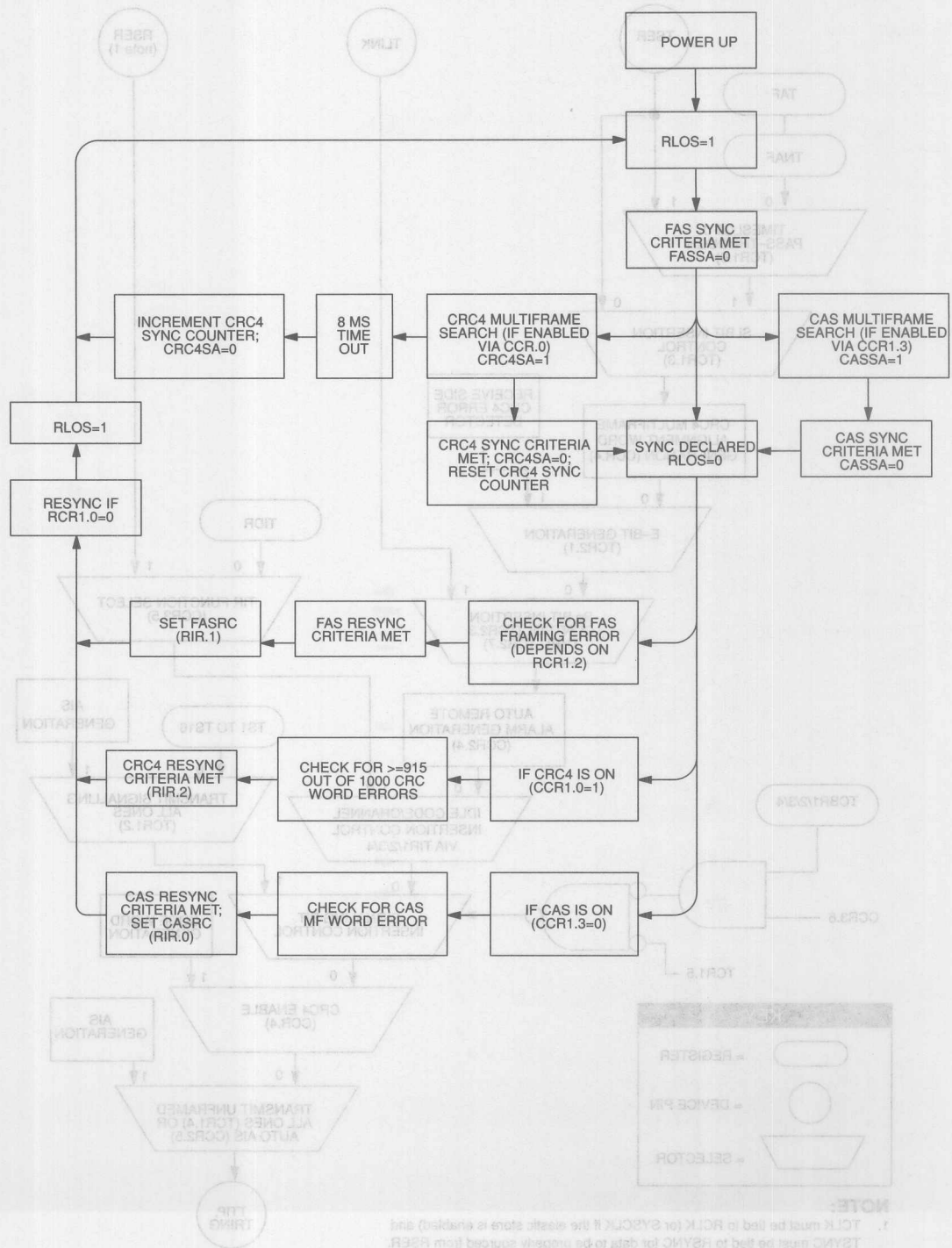
G.802 TIMING Figure 13-7**NOTE:**

1. RCHBLK or TCHBLK is programmed to pulse high during timeslots 1 to 15, 17 to 25, and during bit 1 of timeslot 26.

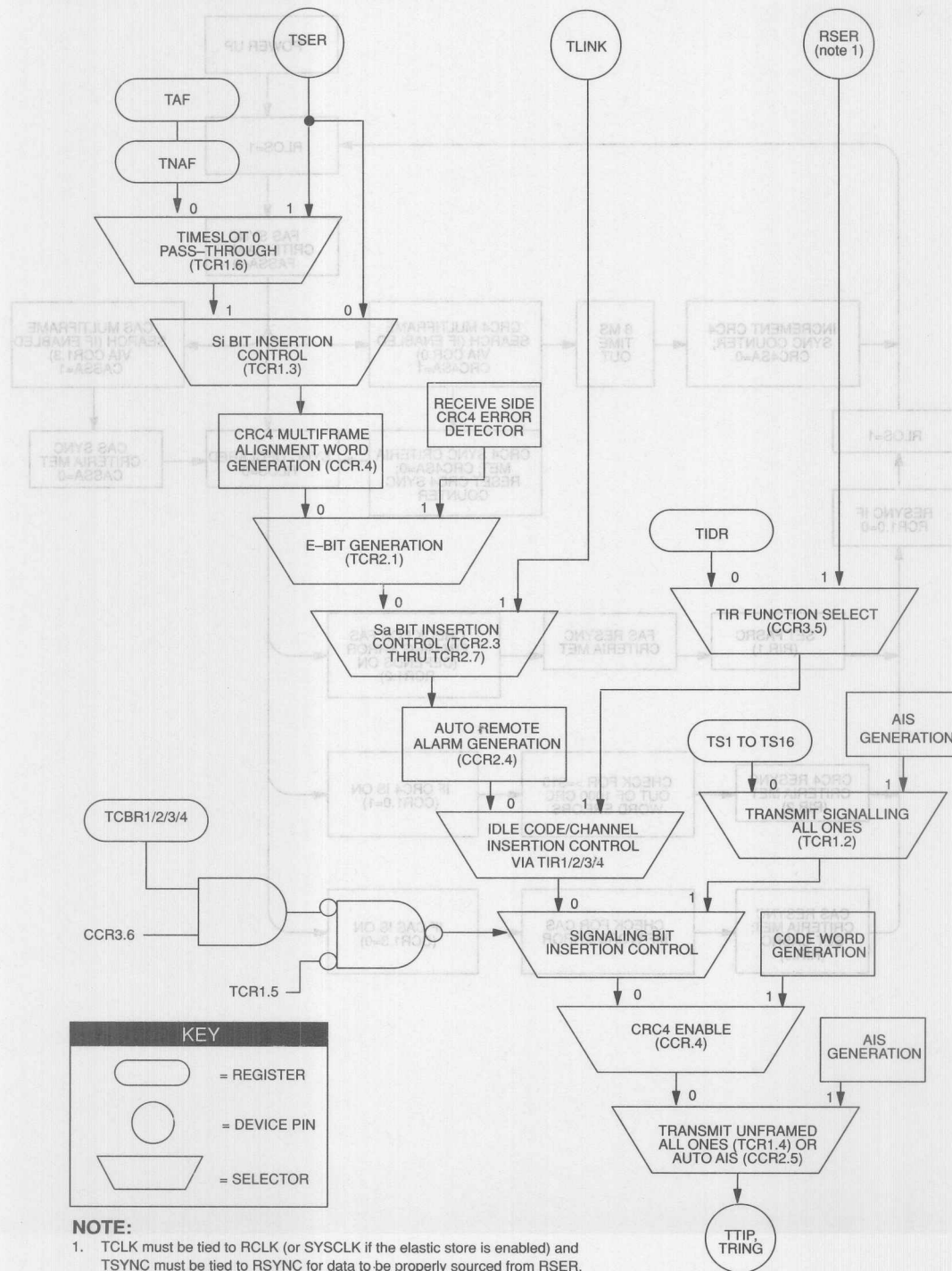
NOTES:

1. TSYNC is the input mode (TCR1 0=0).
2. TSYNC is the output mode (TCR1 0=1).
3. TCHBLK is programmed to block channel 2.
4. TLINK is programmed to source the 256 bits.
5. TLINK is programmed to source the 256 and 258 bits.
6. Shown is a non-align frame boundary.
7. See Figures 13.3 and 13.4 for details on timing with the transmit side elastic store enabled.

DS2153Q SYNCHRONIZATION FLOWCHART Figure 13–8



DS2153Q TRANSMIT DATA FLOW Figure 13–9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.75		5.25	V	1

CAPACITANCE(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		60		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	μA	3
Output Leakage	I_{LO}			1.0	μA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

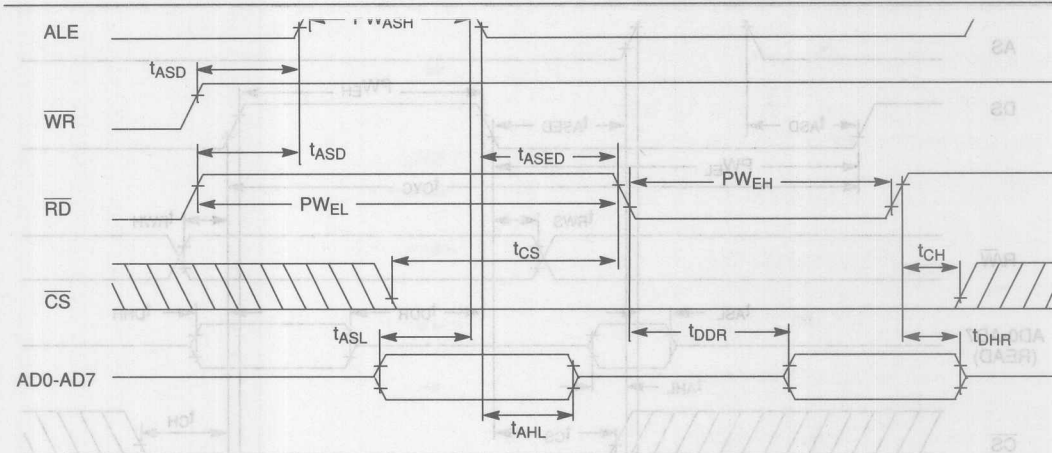
1. Applies to RVDD, TVDD, and DVDD.
2. TCLK=2.048 MHz.
3. $0.0V < V_{IN} < V_{DD}$.
4. Applies to $\overline{INT1}$ and $\overline{INT2}$ when 3-stated.

AC CHARACTERISTICS - PARALLEL PORT

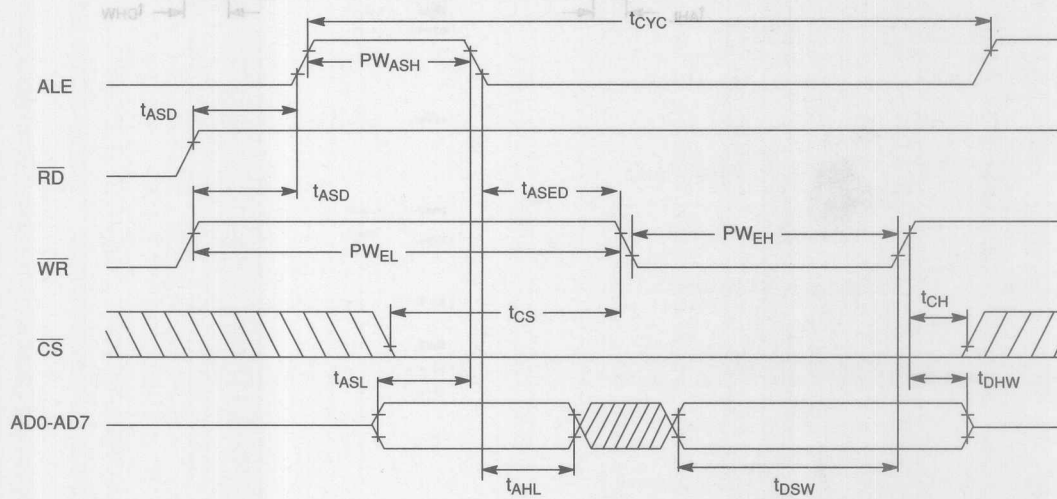
(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t _{CYC}	250			ns	
Pulse Width, DS Low or $\overline{\text{RD}}$ High	PW _{EL}	150			ns	
Pulse Width, DS High or $\overline{\text{RD}}$ Low	PW _{EH}	100			ns	
Input Rise/Fall Times	t _R , t _F			30	ns	
R/W Hold Time	t _{RWH}	10			ns	
R/W Setup Time Before DS High	t _{RWS}	50			ns	
$\overline{\text{CS}}$ Setup Time Before DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$ active	t _{CS}	20			ns	
$\overline{\text{CS}}$ Hold Time	t _{CH}	0			ns	
Read Data Hold Time	t _{DHR}	10		50	ns	
Write Data Hold Time	t _{DHW}	0			ns	
Muxed Address Valid to AS or ALE fall	t _{ASL}	20			ns	
Muxed Address Hold Time	t _{AHL}	10			ns	
Delay Time DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$ to AS or ALE Rise	t _{ASD}	25			ns	
Pulse Width AS or ALE High	PW _{ASH}	40			ns	
Delay Time, AS or ALE to DS, $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{ASED}	20			ns	
Output Data Delay Time from DS or $\overline{\text{RD}}$	t _{DDR}	20		100	ns	
Data Setup Time	t _{DSW}	80			ns	

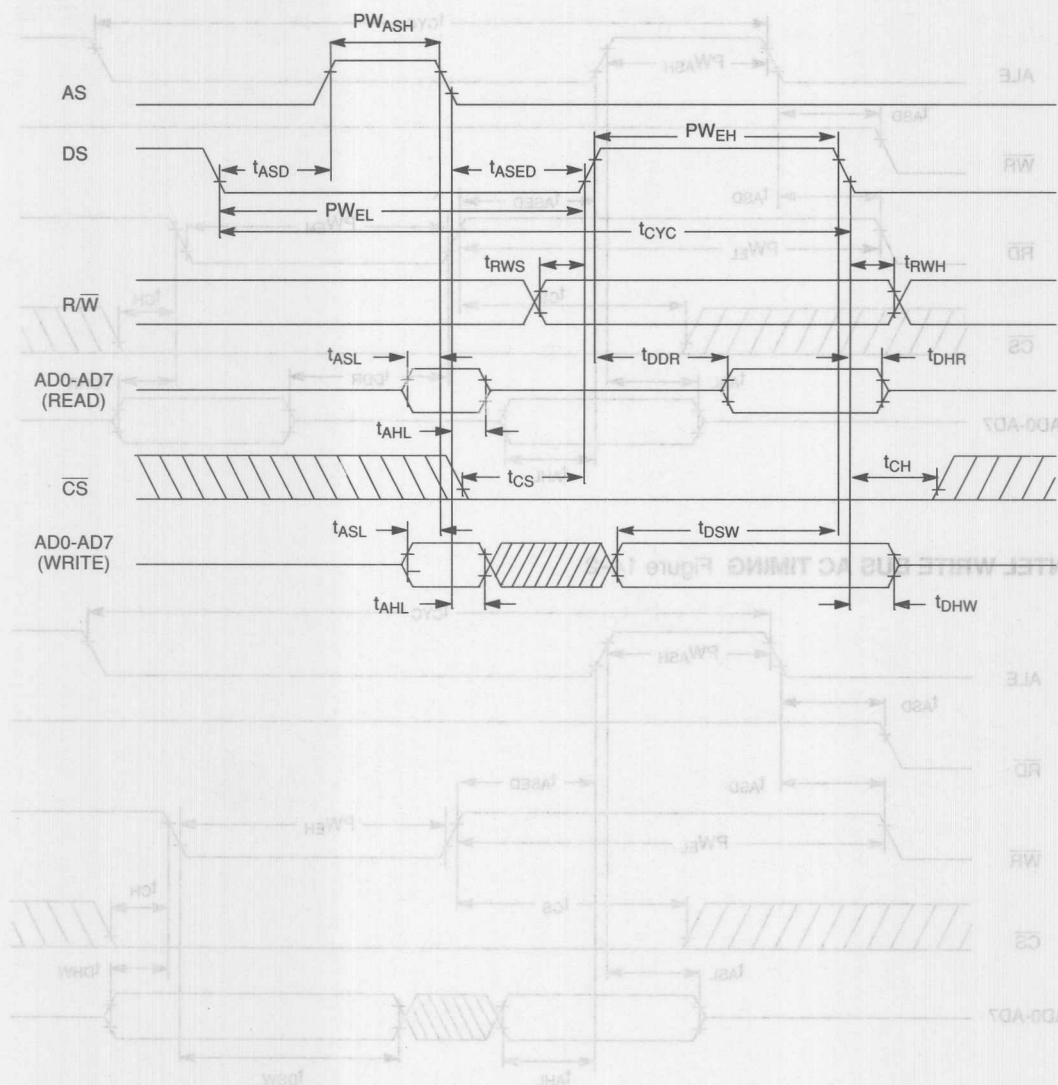
NOTES:
1. Applies to RVDD, TVDD, and DVDD.
2. TCLK=2.048 MHz.
3. 0.0V < V_{IN} < V_{DD}.
4. Applies to INT1 and INT2 when 3-stated.



INTEL WRITE BUS AC TIMING Figure 14-2



MOTOROLA BUS AC TIMING Figure 14-3



AC CHARACTERISTICS – RECEIVE SIDE(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ALCKI/RCLK Period	t_{CP}		488		ns	
RCLK Pulse Width	t_{CH} t_{CL}	180 180	244 244		ns ns	1
RCLK Pulse Width	t_{CH} t_{CL}	90 200	244 244		ns ns	2
SYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	3 4
SYSCLK Pulse Width	t_{SH} t_{SL}	75 75			ns	
RSYNC Set Up to SYSCLK Falling	t_{SU}	25		$t_{SP}-100$	ns	
RSYNC Hold from SYSCLK Falling	t_{HD}	25		infinite	ns	
SYSCLK Rise/Fall Times	t_R, t_F			25	ns	
Delay RCLK or SYSCLK to RSER Valid	t_{DD}			70	ns	
Delay RCLK or SYSCLK to RCHCLK	t_{D1}			50	ns	
Delay RCLK or SYSCLK to RCHBLK	t_{D2}			50	ns	
Delay RCLK or SYSCLK to RSYNC	t_{D3}			50	ns	
Delay RCLK to RLCLK	t_{D4}			50	ns	
Delay RCLK to RLINK Valid	t_{D5}			50	ns	

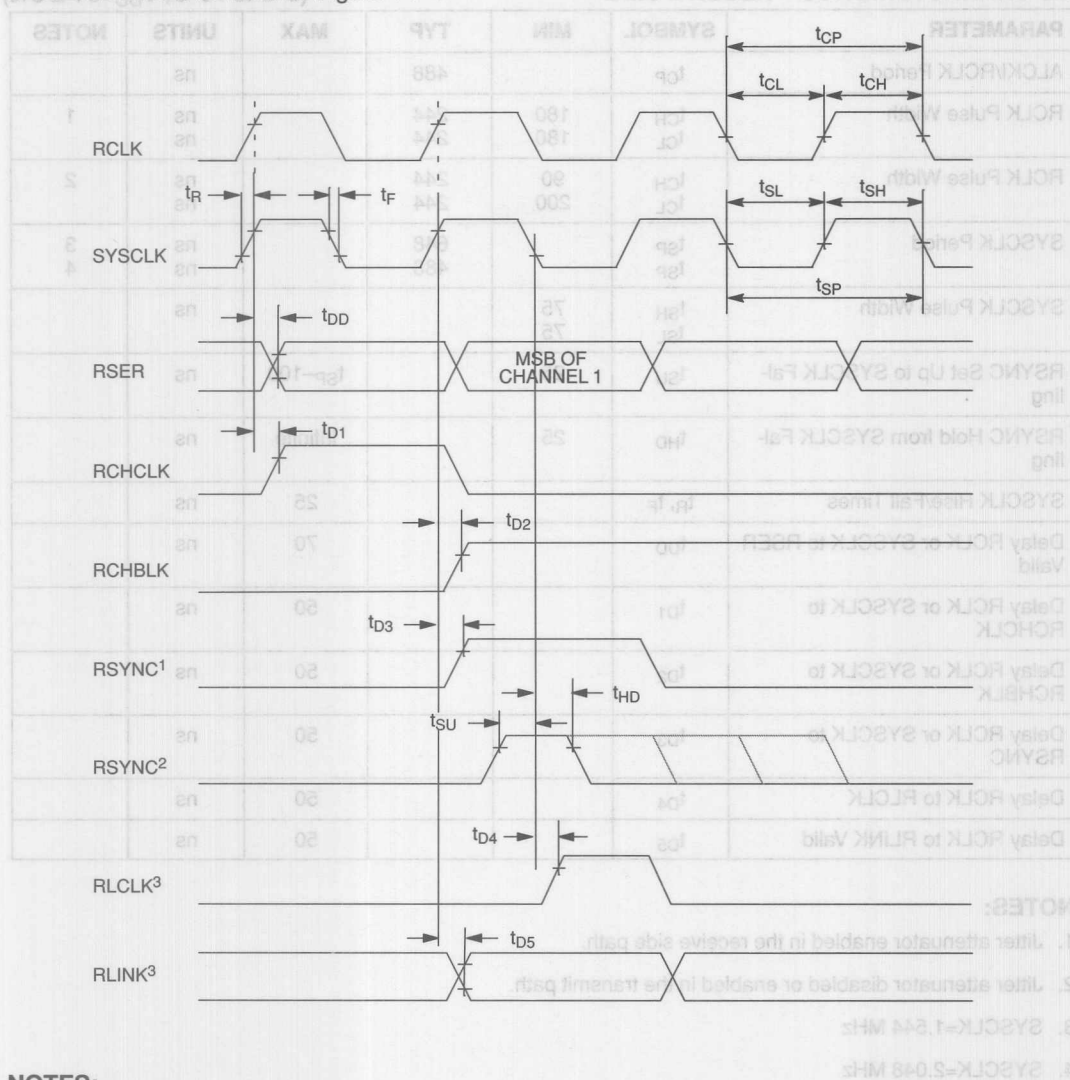
NOTES:

1. Jitter attenuator enabled in the receive side path.
2. Jitter attenuator disabled or enabled in the transmit path.
3. SYSCLK=1.544 MHz
4. SYSCLK=2.048 MHz

NOTES:

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RLCLK and RLINK only have a timing relationship to RCLK; no timing relationship between RLCLK/RLINK and RSYNC is implied.
4. RLCLK can exhibit a short high time if the jitter attenuator is either disabled or in the transmit path.

RECEIVE SIDE AC TIMING Figure 14-4

**NOTES:**

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RLCLK and RLINK only have a timing relationship to RCLK; no timing relationship between RLCLK/RLINK and RSYNC is implied.
4. RCLK can exhibit a short high time if the jitter attenuator is either disabled or in the transmit path.

AC CHARACTERISTICS – TRANSMIT SIDE(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

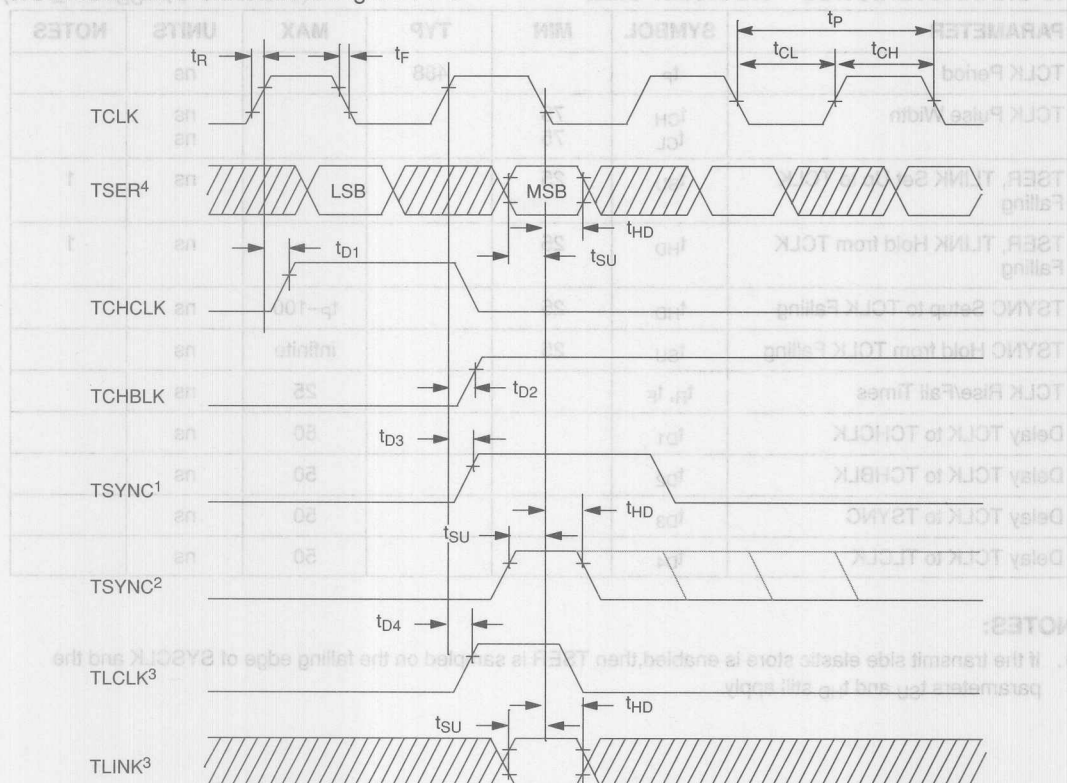
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P		488		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TSER, TLINK Set Up to TCLK Falling	t_{SU}	25			ns	1
TSER, TLINK Hold from TCLK Falling	t_{HD}	25			ns	1
TSYNC Setup to TCLK Falling	t_{HD}	25		$t_P - 100$	ns	
TSYNC Hold from TCLK Falling	t_{SU}	25		infinite	ns	
TCLK Rise/Fall Times	t_R, t_F			25	ns	
Delay TCLK to TCHCLK	t_{D1}			50	ns	
Delay TCLK to TCHBLK	t_{D2}			50	ns	
Delay TCLK to TSYNC	t_{D3}			50	ns	
Delay TCLK to TLCLK	t_{D4}			50	ns	

NOTES:

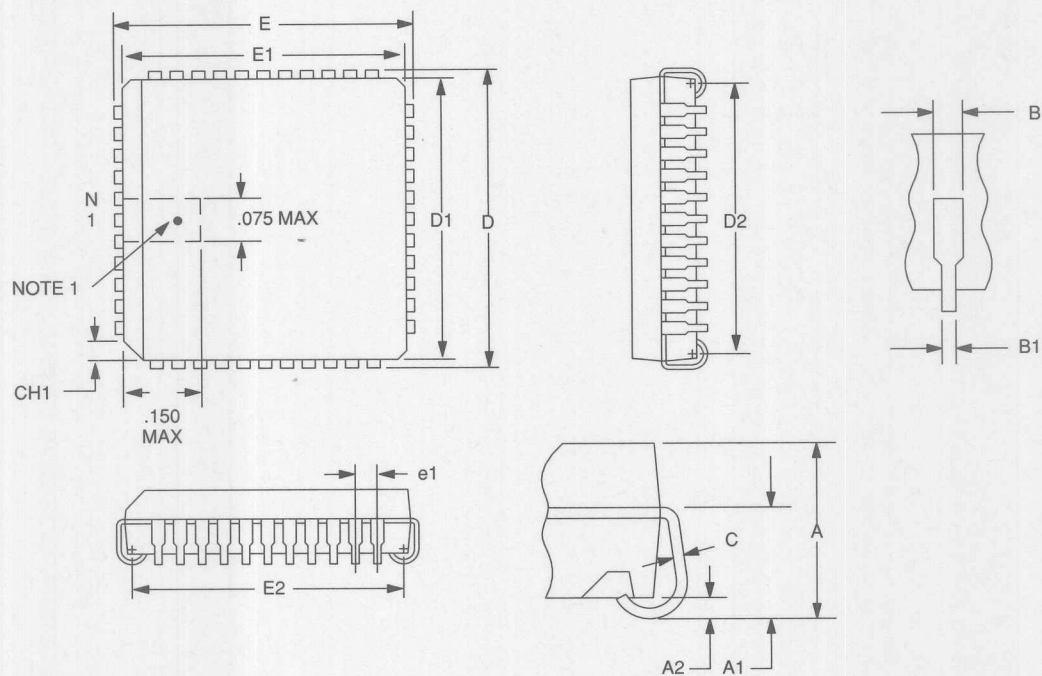
1. If the transmit side elastic store is enabled, then TSER is sampled on the falling edge of SYSCLK and the parameters t_{SU} and t_{HD} still apply.

**NOTES:**

1. TSYNC is in the output mode (TCHT=0=1).
2. TSYNC is in the input mode (TCHT=0=0).
3. No timing relationship between TSYNC and TLCLK/TLINK is implied.
4. TSER is sampled on the falling edge of SYSCLK if the transmit side elastic store is enabled.

TRANSMIT SIDE AC TIMING Figure 14-5

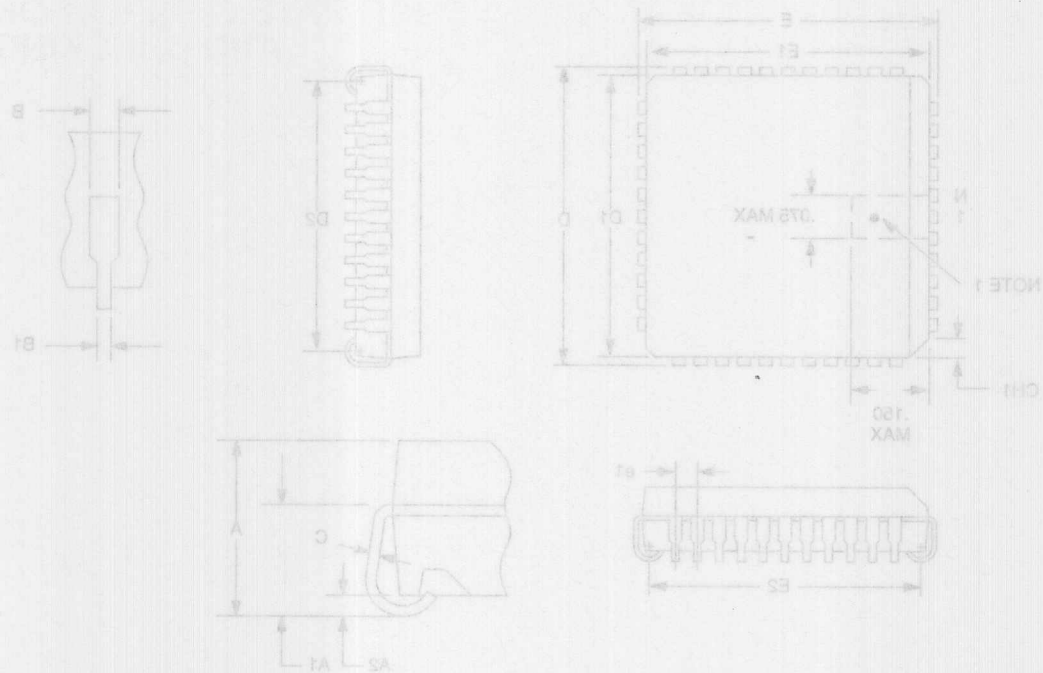
DS2153Q T1 SINGLE-CHIP TRANSCEIVER 44-PIN PLCC



NOTE1: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	-
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	-

0231230 T1 SINGLE-CHIP TRANSCEIVER 44-PIN PLCC



NOTE: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.

DIM	INCHES	
	MIN	MAX
A	0.188	0.190
AI	0.000	0.150
AS	0.000	-
B	0.008	0.008
BI	0.013	0.051
C	0.008	0.015
CHI	0.045	0.048
D	0.855	0.855
DI	0.850	0.850
DS	0.850	0.850
E	0.865	0.865
ES	0.850	0.850
ES	0.850	0.850
44	0.000 BSC	
44	-	-

DIGITAL BIT ERROR RATE GENERATION AND CHECKING

DS2172
Bit Error Rate Tester (BERT)

FEATURES

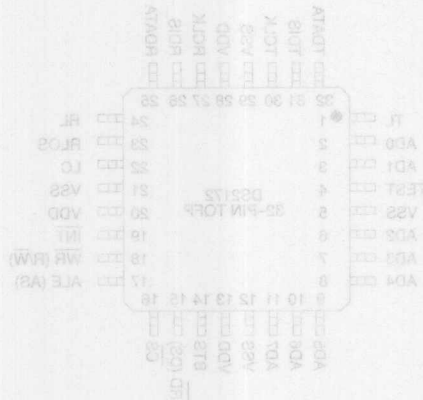
- Generates/detects digital bit patterns for analyzing, evaluating and troubleshooting digital communications systems
- Operates at speeds from DC to 52 MHz
- Programmable polynomial length and feedback taps for generation of any other pseudorandom pattern up to 32 bits in length including: $2^{15}-1$, $2^{16}-1$, $2^{17}-1$, $2^{18}-1$, $2^{19}-1$, and $2^{20}-1$
- Programmable user-defined pattern and length for generation of any repetitive pattern up to 32 bits in length
- Large 32-bit error count and bit count registers
- Software programmable bit error insertion
- Fully independent transmit and receive sections
- 8-bit parallel control port
- Detects test patterns with bit error rates up to 10^{-8}

DESCRIPTION

The DS2172 Bit Error Rate Tester (BERT) is a software programmable test pattern generator, receiver, and analyzer capable of meeting the most stringent error performance requirements of digital transmission facilities. Two categories of test pattern generation (Pseudo-random and Repetitive) conform to CCITT/ITU O.151, O.152, O.153, and O.154 standards. The DS2172 operates at clock rates ranging from DC to 52 MHz. This wide range of operating frequency allows the DS2172 to be used in existing and future test equipment, transmission facilities, switching equipment, multiplexers, DACs, Routers, Bridges, CSUs, DSUs, and CPE equipment.

The DS2172 uses programmable pattern registers providing the unique ability to generate feedback patterns required for T1, Fractional-T1, Smart Jack, and other

PIN ASSIGNMENT



test procedures. Hence the DS2172 can initiate the test, run the test, check for errors, and finally deactivate the test.

The DS2172 consists of four functional blocks: the pattern generator, pattern detector, error counter, and control interface. The DS2172 can be programmed to generate any pseudorandom pattern with length up to 32 bits or any user programmable bit pattern from 1 to 32 bits in length. Logic inputs can be used to configure the DS2172 for applications requiring gap clocking such as Fractional-T1, Switched-56, DDS, normal framing requirements, and per-channel test procedures. In addition, the DS2172 can insert single or 10^{-8} bit errors to verify equipment operation and connectivity.

DALLAS

SEMICONDUCTOR

DS2172

Bit Error Rate Tester (BERT)

FEATURES

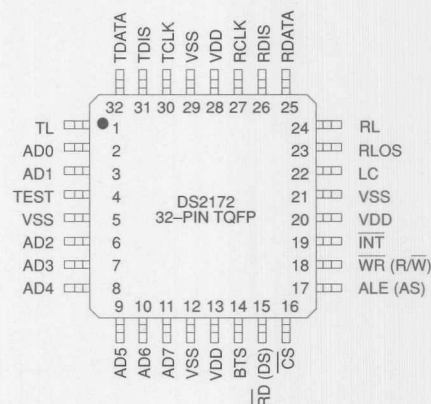
- Generates/Detects digital bit patterns for analyzing, evaluating and troubleshooting digital communications systems
- Operates at speeds from DC to 52 MHz
- Programmable polynomial length and feedback taps for generation of any other pseudorandom pattern up to 32 bits in length including: 2^6-1 , 2^9-1 , $2^{11}-1$, $2^{15}-1$, $2^{20}-1$, $2^{23}-1$, and $2^{32}-1$
- Programmable user-defined pattern and length for generation of any repetitive pattern up to 32 bits in length
- Large 32-bit error count and bit count registers
- Software programmable bit error insertion
- Fully independent transmit and receive sections
- 8-bit parallel control port
- Detects test patterns with bit error rates up to 10^{-2}

DESCRIPTION

The DS2172 Bit Error Rate Tester (BERT) is a software programmable test pattern generator, receiver, and analyzer capable of meeting the most stringent error performance requirements of digital transmission facilities. Two categories of test pattern generation (Pseudorandom and Repetitive) conform to CCITT/ITU O.151, O.152, O.153, and O.161 standards. The DS2172 operates at clock rates ranging from DC to 52 MHz. This wide range of operating frequency allows the DS2172 to be used in existing and future test equipment, transmission facilities, switching equipment, multiplexers, DACs, Routers, Bridges, CSUs, DSUs, and CPE equipment.

The DS2172 user programmable pattern registers provide the unique ability to generate loopback patterns required for T1, Fractional-T1, Smart Jack, and other

PIN ASSIGNMENT



test procedures. Hence the DS2172 can initiate the loopback, run the test, check for errors, and finally deactivate the loopback.

The DS2172 consists of four functional blocks: the pattern generator, pattern detector, error counter, and control interface. The DS2172 can be programmed to generate any pseudorandom pattern with length up to 32 bits or any user programmable bit pattern from 1 to 32 bits in length. Logic inputs can be used to configure the DS2172 for applications requiring gap clocking such as Fractional-T1, Switched-56, DDS, normal framing requirements, and per-channel test procedures. In addition, the DS2172 can insert single or 10^{-1} to 10^{-7} bit errors to verify equipment operation and connectivity.

1.0 GENERAL OPERATION

1.1 Pattern Generation

The DS2172 is programmed to generate a particular test pattern by programming the following registers:

- Pattern Set Registers (PSR)
- Pattern Length Register (PLR)
- Polynomial Tap Register (PTR)
- Pattern Control Register (PCR)
- Error Insertion Register (EIR).

Please see Tables 4 and 5 for examples of how to program these registers in order to generate some standard test patterns. Once these registers are programmed, the user will then toggle the TL (Transmit Load) bit or pin to load the pattern into the onboard pattern generation circuitry and the pattern will begin appearing at the TDATA pin.

1.2 Pattern Synchronization

The DS2172 expects to receive the same pattern that it generates. The DS2172 will synchronize to the pattern after it receives the pattern for 32 consecutive bit positions without any errors. The user can control the onboard synchronizer circuitry with the Sync Enable and Resync bits in the Pattern Control Register. Status

of the synchronizer is available in the Status Register. The user can also access the raw receive data stream via the Pattern Receive Registers (PRR).

1.3 BER Calculation

Users can calculate the actual Bit Error Rate (BER) of the digital communications channel by reading the bit error count out of the Bit Error Count Register (BECR) and reading the bit count out of the Bit Count Register (BCR) and then dividing the BECR value with the BCR value. The user has total control over the integration period of the measurement. The LC (Load Count) bit or pin is used to set the integration period.

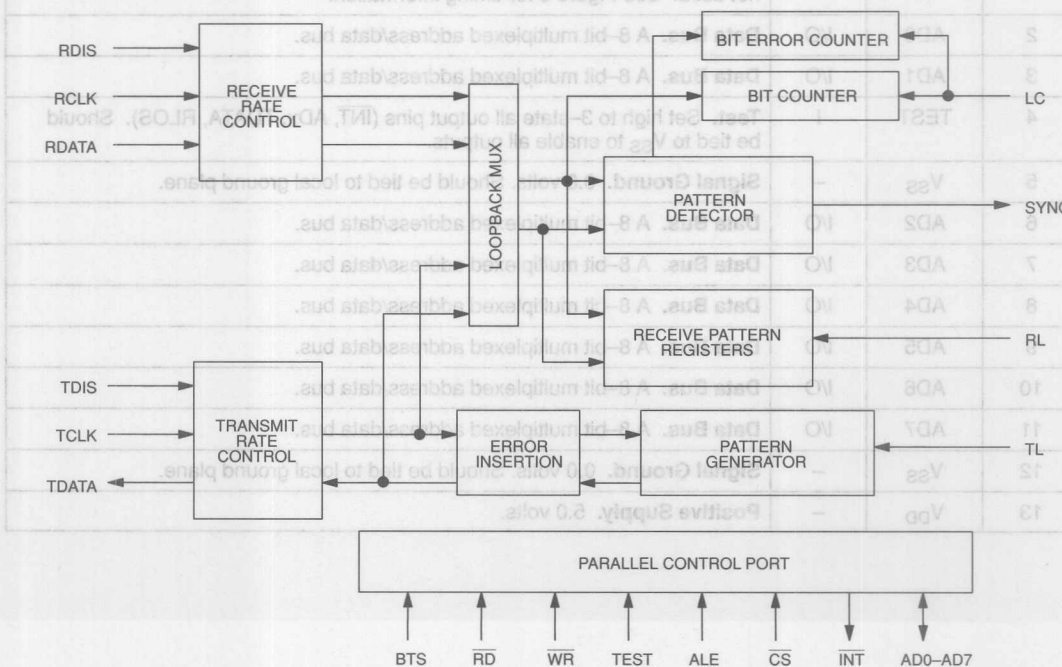
1.4 Generating Errors

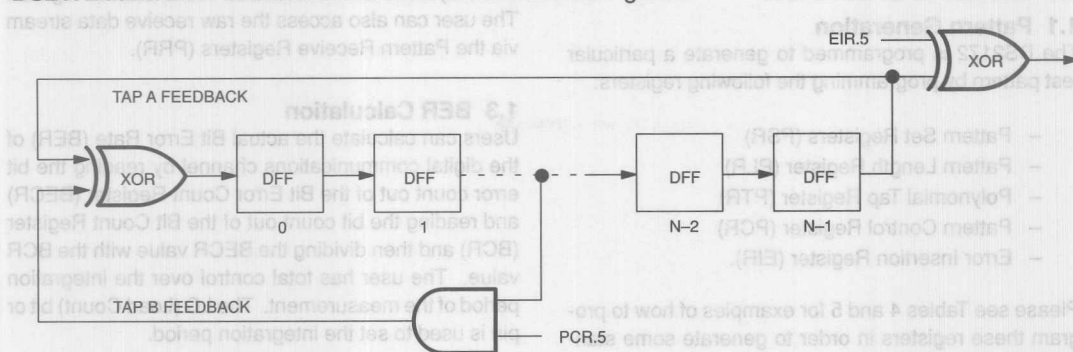
Via the Error Insertion Register (EIR), the user can intentionally inject a particular error rate into the transmitted data stream. Injecting errors allows users to stress communication links and to check the functionality of error monitoring equipment along the path.

1.5 Power-Up Sequence

On power-up, the registers in the DS2172 will be in a random state. The user must program all the internal registers to a known state before proper operation can be insured.

DS2172 FUNCTIONAL BLOCK DIAGRAM Figure 1



DS2172 PATTERN GENERATION BLOCK DIAGRAM Figure 2**NOTES:**

1. Tap A always equals length (N-1) of pseudorandom or repetitive pattern.
2. Tap B can be programmed to any feedback tap for pseudorandom pattern generation.

DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TL	I	Transmit Load. A positive-going edge loads the pattern generator with the contents of the Pattern Set Registers. The MSB of the repetitive or pseudorandom pattern appears at TDATA after the third positive edge of TCLK from asserting TL. TL is logically OR'ed with PCR.7 and should be tied to V _{SS} if not used. See Figure 8 for timing information.
2	AD0	I/O	Data Bus. A 8-bit multiplexed address/data bus.
3	AD1	I/O	Data Bus. A 8-bit multiplexed address/data bus.
4	TEST	I	Test. Set high to 3-state all output pins (INT, ADx, TDATA, RLOS). Should be tied to V _{SS} to enable all outputs.
5	V _{SS}	—	Signal Ground. 0.0 volts. Should be tied to local ground plane.
6	AD2	I/O	Data Bus. A 8-bit multiplexed address/data bus.
7	AD3	I/O	Data Bus. A 8-bit multiplexed address/data bus.
8	AD4	I/O	Data Bus. A 8-bit multiplexed address/data bus.
9	AD5	I/O	Data Bus. A 8-bit multiplexed address/data bus.
10	AD6	I/O	Data Bus. A 8-bit multiplexed address/data bus.
11	AD7	I/O	Data Bus. A 8-bit multiplexed address/data bus.
12	V _{SS}	—	Signal Ground. 0.0 volts. Should be tied to local ground plane.
13	V _{DD}	—	Positive Supply. 5.0 volts.

PIN	SYMBOL	TYPE	DESCRIPTION
14	BTS	I	Bus Type Select. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD(DS), ALE(AS), and WR(R/W) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().
15	RD (DS)	I	Read Input (Data Strobe).
16	CS	I	Chip Select. Must be low to read or write the port.
17	ALE (AS)	I	Address Latch Enable (Address Strobe). A positive going edge serves to demultiplex the bus.
18	WR (R/W)	I	Write Input (Read/Write).
19	INT	O	Alarm Interrupt. Flags host controller during conditions defined in Status Register. Active low, open drain output.
20	V _{DD}	—	Positive Supply. 5.0 volts.
21	V _{SS}	—	Signal Ground. 0.0 volts. Should be tied to local ground plane.
22	LC	I	Load Count. A positive-going edge latches the current bit and bit error count into the user accessible BCR and BECR registers and clears the internal count registers. LC is logically OR'ed with control bit PCR.4. Should be tied to V _{SS} if not used.
23	RLOS	O	Receive Loss Of Sync. Indicates the real time status of the receive synchronizer. Active high output; transitions low after receiving 32 matching bits.
24	RL	I	Receive Load. A positive-going edge loads the previous 32 bits of data received at RDATA into the Pattern Receive Registers. RL is logically OR'ed with control bit PCR.3. Should be tied to V _{SS} if not used.
25	RDATA	I	Receive Data. Received NRZ serial data, sampled on the rising edge of RCLK.
26	RDIS	I	Receive Disable. Set high to prevent the data at RDATA from being sampled. Set low to allow bits at RDATA to be sampled. Should be tied to V _{SS} if not used. See Figure 6 for timing information.
27	RCLK	I	Receive Clock. Input clock from transmission link. 0 to 52 MHz. Can be a gapped clock. Fully independent from TCLK.
28	V _{DD}	—	Positive Supply. 5.0 volts.
29	V _{SS}	—	Signal Ground. 0.0 volts. Should be tied to local ground plane.
30	TCLK	I	Transmit Clock. Transmit demand clock. 0 to 52 MHz. Can be a gapped clock. Fully independent of RCLK.
31	TDIS	I	Transmit Disable. Set high to hold the current bit being transmitted at TDATA. Set low to allow the next bit to appear at TDATA. Should be tied to V _{SS} if not used. See Figure 7 for timing information.
32	TDATA	O	Transmit Data. Transmit NRZ serial data, updated on the rising edge of TCLK.

DS2172 REGISTER MAP Table 2

ADDRESS	R/W	REGISTER NAME
00	R/W	Pattern Set Register 3.
01	R/W	Pattern Set Register 2.
02	R/W	Pattern Set Register 1.
03	R/W	Pattern Set Register 0.
04	R/W	Pattern Length Register.
05	R/W	Polynomial Tap Register.
06	R/W	Pattern Control Register.
07	R/W	Error Insert Register.
08	R	Bit Counter Register 3.
09	R	Bit Counter Register 2.
0A	R	Bit Counter Register 1.
0B	R	Bit Counter Register 0.
0C	R	Bit Error Counter Register 3.
0D	R	Bit Error Counter Register 2.
0E	R	Bit Error Counter Register 1.
0F	R	Bit Error Counter Register 0.
10	R	Pattern Receive Register 3.
11	R	Pattern Receive Register 2.
12	R	Pattern Receive Register 1.
13	R	Pattern Receive Register 0.
14	R	Status Register.
15	R/W	Interrupt Mask Register.
1C	R/W	Test Register (see note 1)

NOTE:

1. The Test Register must be set to 00 hex to insure proper operation of the DS2172.

2.0 PARALLEL CONTROL INTERFACE

The DS2172 is controlled via a multiplexed bi-directional address/data bus by an external microcontroller or microprocessor. The DS2172 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the A.C. Electrical Characteristics for more details. The multiplexed bus on the DS2172 saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the DS2172 latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or \overline{WR} pulses. In a read cycle, the DS2172 outputs a byte of data during the latter portion of the DS or \overline{RD} pulses. The read cycle is terminated and the bus returns to a high impedance state as RD transitions high in Intel timing or as DS transitions low in Motorola timing. The DS2172 can also be easily connected to non-multiplexed buses.

3.0 PATTERN SET REGISTERS

The Pattern Set Registers (PSR) are loaded each time a new pattern (whether it be pseudorandom or repetitive) is to be generated. When a pseudorandom pattern is generated, all four PSRs must be loaded with FF Hex. When a repetitive pattern is to be created, the four PSRs are loaded with the pattern that is to be repeated. Please see Tables 4 and 5 for some programming examples.

PATTERN SET REGISTERS

(MSB)				(LSB)				
PS31	PS30	PS29	PS28	PS27	PS26	PS25	PS24	PSR3 (addr.=00 Hex)
PS23	PS22	PS21	PS20	PS19	PS18	PS17	PS16	PSR2 (addr.=01 Hex)
PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	PSR1 (addr.=02 Hex)
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	PSR0 (addr.=03 Hex)

4.0 PATTERN LENGTH REGISTER

Length Bits LB4 to LB0 determine the length of the pseudorandom polynomial or programmable repetitive pattern that is generated and detected. With the pseudorandom patterns, the "Tap A" feedback position

of the pattern generator is always equal to the value in the Pattern Length Register (PLR). Please refer to Figure 2 for a block diagram of the pattern generator and to Tables 4 and 5 for some programming examples.

PLR: PATTERN LENGTH REGISTER (Address=04 Hex)

(MSB)				(LSB)				
				LB4	LB3	LB2	LB1	LB0

SYMBOL	POSITION	NAME AND DESCRIPTION
—	PLR1.7	Not Assigned. Should be set to 0 when written to.
—	PLR1.6	Not Assigned. Should be set to 0 when written to.
—	PLR1.5	Not Assigned. Should be set to 0 when written to.
LB4	PLR1.4	Length Bit 4.
LB3	PLR1.3	Length Bit 3.
LB2	PLR1.2	Length Bit 2.
LB1	PLR1.1	Length Bit 1.
LB0	PLR1.0	Length Bit 0.

5.0 POLYNOMIAL TAP REGISTER

Polynomial Tap Bits PT4 – PT0 determine the feedback position of Tap B connected to the XOR input of the pattern generator. Feedback Tap B provides one of two

feedback paths within the pattern generator. Please refer to Figure 2 for a block diagram of the pattern generator and to Tables 4 and 5 for register programming examples.

PTR: POLYNOMIAL TAP REGISTER (Address=05 Hex)

(MSB)				(LSB)			
—	—	PT4	PT3	PT2	PT1	PT0	

SYMBOL	POSITION	NAME AND DESCRIPTION
—	PTR.7	Not Assigned. Should be set to 0 when written to.
—	PTR.6	Not Assigned. Should be set to 0 when written to.
—	PTR.5	Not Assigned. Should be set to 0 when written to.
PT4	PTR.4	Polynomial Tap Bit 4.

PT3	PTR.3	Polynomial Tap Bit 3.				
PT2	PTR.2	Polynomial Tap Bit 2.				
PT1	PTR.1	Polynomial Tap Bit 1.				
PT0	PTR.0	Polynomial Tap Bit 0.				

6.0 PATTERN CONTROL REGISTER

The Pattern Control Register (PCR) is used to configure the operating parameters of the DS2172 and to control

the patterns being generated and received. Also the PCR is used to control the pattern synchronizer and the error and bit counters.

PCR: PATTERN CONTROL REGISTER (Address=06 Hex)

(MSB)								(LSB)
TL	QRSS	PS	LC	RL	SYNCE	RESYNC	LPBK	
SYMBOL	POSITION	NAME AND DESCRIPTION						
TL	PCR.7	Transmit Load. A low to high transition loads the pattern generator with the contents of the Pattern Set Registers. PCR.7 is logically OR'ed with the input pin TL. Must be cleared and set again for subsequent loads.						
QRSS	PCR.6	Zero Suppression Select. Forces a "one" into the pattern whenever the next 14 bit positions are all "zeros". Should only be set when using the QRSS pattern. 0 = Zero suppression disabled 1 = Zero suppression enabled						
PS	PCR.5	Pattern Select. 0 = Repetitive Pattern 1 = Pseudorandom Pattern						
LC	PCR.4	Latch Count Registers. A low to high transition latches the bit and error counts into the user accessible registers BCR and BECR and clears the internal register count. PCR.4 is logically OR'ed with input pin LC. Must be cleared and set again for subsequent loads.						
RL	PCR.3	Receive Data Load. A transition from low to high loads the previous 32 bits of data received at RDATA into the Pattern Receive Registers (PRR). PCR.3 is logically OR'ed with input pin RL. Must be cleared and set again for subsequent latches.						
SYNCE	PCR.2	SYNC Enable. 0 = auto resync is enabled. 1 = auto resync is disabled.						
RESYNC	PCR.1	Initiate Manual Resync Process. A low to high transition will force the DS2172 to resynchronize to the incoming pattern at RDATA. Must be cleared and set again for a subsequent resync.						
LPBK	PCR.0	Transmit/Receive Loopback Select. When enabled, the RDATA input is disabled; TDATA continues to output data as normal. See Figure 1. 0 = loopback disabled 1 = loopback enabled						

7.0 ERROR INSERT REGISTER

The Error Insertion Register (EIR) controls circuitry within the DS2172 that allows the generated pattern to be intentionally corrupted. Bit errors can be inserted

automatically at regular intervals by properly programming the EIR0 to EIR2 bits or bit errors can be inserted at random (under microcontroller control) via the EIR.3 bit.

EIR: ERROR INSERT REGISTER (Address=07 Hex)

(MSB)								(LSB)
—	—	TINV	RINV	SBE	EIR2	EIR1	EIR0	
SYMBOL	POSITION	NAME AND DESCRIPTION						
—	EIR.7	Not Assigned. Should be set to 0 when written to.						
—	EIR.6	Not Assigned. Should be set to 0 when written to.						
TINV	EIR.5	Transmit Data Inversion Select. 0 = do not invert data to be transmitted at TDATA 1 = invert data to be transmitted at TDATA						
RINV	EIR.4	Receive Data Inversion Select. 0 = do not invert data received at RDATA 1 = invert data received at RDATA						
SBE	EIR.3	Single Bit Error Insert. A low to high transition will create a single bit error. Must be cleared and set again for a subsequent bit error to be inserted. Can be used to accomplish rates not addressed in Table 3 (e.g. BER of less than 10^{-7}).						
EIB2	EIR.2	Error Insert Bit 2. See Table 3.						
EIB1	EIR.1	Error Insert Bit 1. See Table 3.						
EIB0	EIR.0	Error Insert Bit 0. See Table 3.						

ERROR BIT INSERTION Table 3

EIB2	EIB1	EIB0	ERROR RATE INSERTED
0	0	0	no errors automatically inserted
0	0	1	10^{-1}
0	1	0	10^{-2}
0	1	1	10^{-3}
1	0	0	10^{-4}
1	0	1	10^{-5}
1	1	0	10^{-6}
1	1	1	10^{-7}

PSEUDORANDOM PATTERN GENERATION (PCR.5=1) Table 4

PATTERN TYPE	PTR	PLR	PSR3	PSR2	PSR1	PSR0	TINV	RINV
$2^3 - 1$	00	02	FF	FF	FF	FF	0	0
$2^4 - 1$	00	03	FF	FF	FF	FF	0	0
$2^5 - 1$	01	04	FF	FF	FF	FF	0	0
$2^6 - 1$	04	05	FF	FF	FF	FF	0	0
$2^7 - 1$	00	06	FF	FF	FF	FF	0	0
$2^7 - 1$ Fractional T1 LB Activate	03	06	FF	FF	FF	FF	0	0
$2^7 - 1$ Fractional T1 LB Deactivate	03	06	FF	FF	FF	FF	1	1
$2^9 - 1$ O.153 (511 ytpc)	04	08	FF	FF	FF	FF	0	0
$2^{10} - 1$	02	09	FF	FF	FF	FF	0	0
$2^{11} - 1$ O.152 and O.153 (2047 type)	08	0A	FF	FF	FF	FF	0	0
$2^{15} - 1$ O.151	0D	0E	FF	FF	FF	FF	1	1
$2^{17} - 1$	02	10	FF	FF	FF	FF	0	0
$2^{18} - 1$	06	11	FF	FF	FF	FF	0	0
$2^{20} - 1$ O.153	02	13	FF	FF	FF	FF	0	0
$2^{20} - 1$ O.151 QRSS (PCR.6=1)	10	13	FF	FF	FF	FF	0	0
$2^{21} - 1$	01	14	FF	FF	FF	FF	0	0
$2^{22} - 1$	00	15	FF	FF	FF	FF	0	0
$2^{23} - 1$ O.151	11	16	FF	FF	FF	FF	1	1
$2^{25} - 1$	02	18	FF	FF	FF	FF	0	0
$2^{28} - 1$	02	1B	FF	FF	FF	FF	0	0
$2^{29} - 1$	01	1C	FF	FF	FF	FF	0	0
$2^{31} - 1$	02	1E	FF	FF	FF	FF	0	0
$2^{32} - 1$ (see note below)	10	1F	FF	FF	FF	FF	0	0

REPETITIVE PATTERN GENERATION (PCR.5=0) Table 5

PATTERN TYPE	PTR	PLR	PSR3	PSR2	PSR1	PSR0	TINV	RINV
all ones	00	00	FF	FF	FF	FF	0	0
all zeros	00	00	FF	FF	FF	FE	0	0
alternating ones and zeros	00	01	FF	FF	FF	FE	0	0
double alternating ones and zeros	00	03	FF	FF	FF	FC	0	0
3 in 24	00	17	FF	20	00	22	0	0
1 in 16	00	0F	FF	FF	00	01	0	0
1 in 8	00	07	FF	FF	FF	01	0	0
1 in 4	00	03	FF	FF	FF	F1	0	0
D4 Line Loopback Activate	00	04	FF	FF	FF	F0	0	0
D4 Line Loopback Deactivate	00	02	FF	FF	FF	FC	0	0

NOTES FOR TABLES 4 AND 5:

1. PTR = Polynomial Tap Register (address = 05)
2. PLR = Pattern Length Register (address = 04)
3. PSR3 = Pattern Set Register 3 (address = 00)
4. PSR2 = Pattern Set Register 2 (address = 01)
5. PSR1 = Pattern Set Register 1 (address = 02)
6. PSR0 = Pattern Set Register 0 (address = 03)
7. TINV = Transmit Data Inversion Select Bit (EIR.5)
8. RINV = Receive Data Inversion Select Bit (EIR.4)
9. For the $2^{32}-1$ pattern, the random pattern actually repeats every $(4093 \times 2^{20}) + 1046529$ bits instead of $2^{32}-1$.

8.0 BIT COUNT REGISTERS

The Bit Count Registers (BCR3 to BCR0) comprise a 32-bit count of bits (actually RCLK cycles) received at RDATA. BC31 is the MSB of the 32 bit count. The bit counter increments for each cycle of RCLK when input pin RDIS is low. The Status Register bit BCOF is set when this 32-bit register overflows. Upon an overflow

condition, the user must clear the BCR by either toggling the LC bit or pin. The DS2172 latches the bit count into the BCR registers and clears the internal bit count when either the PCR.4 bit or the LC input pin toggles from low to high. The bit count and bit error count (available via the BECRs) are used by an external processor to compute the BER performance on a loop or channel basis.

BIT COUNT REGISTERS

(MSB)								(LSB)	
BC31	BC30	BC29	BC28	BC27	BC26	BC25	BC24	BCR3 (addr.=08 Hex)	
BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16	BCR2 (addr.=09 Hex)	
BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BCR1 (addr.=0A Hex)	
BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	BCR0 (addr.=0B Hex)	

9.0 BIT ERROR COUNT REGISTERS

The Bit Error Count Registers (BECR3 to BECR0) comprise a 32-bit count of bits received in error at RDATA. BECR31 is the MSB of the 32 bit count. The Status Register bit BECOF is set when this 32-bit register overflows. Upon an overflow condition, the user must clear the BECR by either toggling the LC bit or pin. The DS2172

latches the bit error count into the BECR registers and clears the internal bit error count when either the PCR.4 bit or the LC input pin toggles from low to high. The bit count (available via the BCRs) and bit error count are used by an external processor to compute the BER performance on a loop or channel basis.

BIT ERROR COUNT REGISTERS

(MSB)				(LSB)				
BEC31	BEC30	BEC29	BEC28	BEC27	BEC26	BEC25	BEC24	BECR3 (addr.=0C Hex)
BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16	BECR2 (addr.=0D Hex)
BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8	BECR1 (addr.=0E Hex)
BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0	BECR0 (addr.=0F Hex)

10.0 PATTERN RECEIVE REGISTERS

The Pattern Receive Registers (PRR) provide access to the data patterns received at RDATA. The DS2172

latches the previous 32 bits of data received when either the RL bit (PCR.3) or pin is toggled from a zero to a one. PRR0 contains the last bit received.

PATTERN RECEIVE REGISTERS

(MSB)				(LSB)				
PR31	PR30	PR29	PR28	PR27	PR26	PR25	PR24	PRR3 (addr.=10 Hex)
PR23	PR22	PR21	PR20	PR19	PR18	PR17	PR16	PRR2 (addr.=11 Hex)
PR15	PR14	PR13	PR12	PR11	PR10	PR9	PR8	PRR1 (addr.=12 Hex)
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	PRR0 (addr.=13 Hex)

11.0 STATUS REGISTER AND INTERRUPT MASK REGISTER

The Status Register (SR) contains information on the current real time status of the DS2172. When a particular event has occurred, the appropriate bit in the register will be set to a one. All of the bits in these registers (except for the SYNC bit) operate in a latched fashion. This means that if an event occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. For the BED, BCOF, and BECOF status

bits, they will be cleared when read and will not be set again until the event has occurred again. For RLOS, RA0, and RA1 status bits, they will be cleared when read if the condition no longer persists.

The SR register has the unique ability to initiate a hardware interrupt via the INT pin. Each of the alarms and events in the SR can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register (IMR).

SR: STATUS REGISTER (Address=14 Hex)

(MSB)				(LSB)			
RA1	RA0	RLOS	BED	BCOF	BECOF	SYNC	
SYMBOL	POSITION	NAME AND DESCRIPTION					
SR.7		Not Assigned. Could be any value when read.					

RA1	SR.6	Receive All Ones. Set when 32 consecutive ones are received; allowed to be cleared when a zero is received.
RA0	SR.5	Receive All Zeros. Set when 32 consecutive zeros are received; allowed to be cleared when a one is received.
RLOS	SR.4	Receive Loss Of Sync. Set when the device is searching for synchronization. Once sync is achieved, will remain set until read.
BED	SR.3	Bit Error Detection. Set when bit errors are detected.
BCOF	SR.2	Bit Counter Overflow. Set when the 32-bit BCR overflows.
BECOF	SR.1	Bit Error Count Overflow. Set when the 32-bit BECR overflows.
SYNC	SR.0	Sync. Real time status of the synchronizer (this bit is not latched). Will be set when the incoming pattern at RDATA matches for 32 consecutive bit positions. Will be cleared when 6 or more bits out of 64 are received in error (if PCR.2 = 0).

IMR: INTERRUPT MASK REGISTER (Address=15 Hex)

(MSB)								(LSB)	
—	RA1	RA0	RLOS	BED	BCOF	BECOF	SYNC		
SYMBOL	POSITION	NAME AND DESCRIPTION							
—	IMR.7	Not Assigned. Should be set to zero when written to.							
RA1	IMR.6	Receive All Ones. 0 = interrupt masked 1 = interrupt enabled							
RA0	IMR.5	Receive All Zeros. 0 = interrupt masked 1 = interrupt enabled							
RLOS	IMR.4	Receive Loss Of Sync. 0 = interrupt masked 1 = interrupt enabled							
BED	IMR.3	Bit Error Detection. 0 = interrupt masked 1 = interrupt enabled							
BCOF	IMR.2	Bit Counter Overflow. 0 = interrupt masked 1 = interrupt enabled							
BECOF	IMR.1	Bit Error Count Overflow. 0 = interrupt masked 1 = interrupt enabled							
SYNC	IMR.0	Sync. 0 = interrupt masked 1 = interrupt enabled							

12.0 AC TIMING AND DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply	V_{DD}	4.50		5.50	V	

CAPACITANCE

($t_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

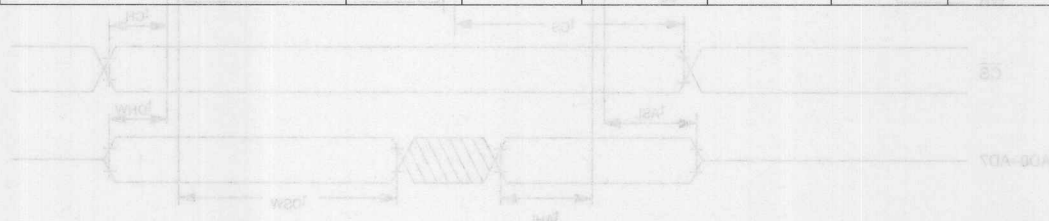
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		10		mA	1
Input Leakage	I_{IL}	–1.0		+1.0	μA	2
Output Leakage	I_{LO}			1.0	μA	3
Output Current @ 2.4V	I_{OH}	–1.0			mA	
Output Current @ 0.4V	I_{OL}	+4.0			mA	

NOTES:

1. TCLK = RCLK = 1.544 MHz; outputs open circuited.
2. $0.0V < V_{IN} < V_{DD}$
3. Applies to \overline{INT} when tri-stated.

AC CHARACTERISTICS – PARALLEL PORT(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS Low or \overline{RD} High	PW_{EL}	100			ns	
Pulse Width, DS High or \overline{RD} Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			20	ns	
R/W Hold Time	t_{RWH}	10			ns	
R/W Setup Time Before DS High	t_{RWS}	50			ns	
\overline{CS} Setup Time Before DS, \overline{WR} or \overline{RD} Active	t_{CS}	20			ns	
\overline{CS} Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	5		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Mux'ed Address Valid to AS or ALE Fall	t_{ASL}	15			ns	
Mux'ed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS, \overline{WR} or \overline{RD} to AS or ALE Rise	t_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, \overline{WR} or \overline{RD}	t_{ASED}	10			ns	
Output Data Delay Time from DS or \overline{RD}	t_{DDR}	5		50	ns	
Data Setup Time	t_{DSW}	50			ns	



AC CHARACTERISTICS – RECEIVE SIDE(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

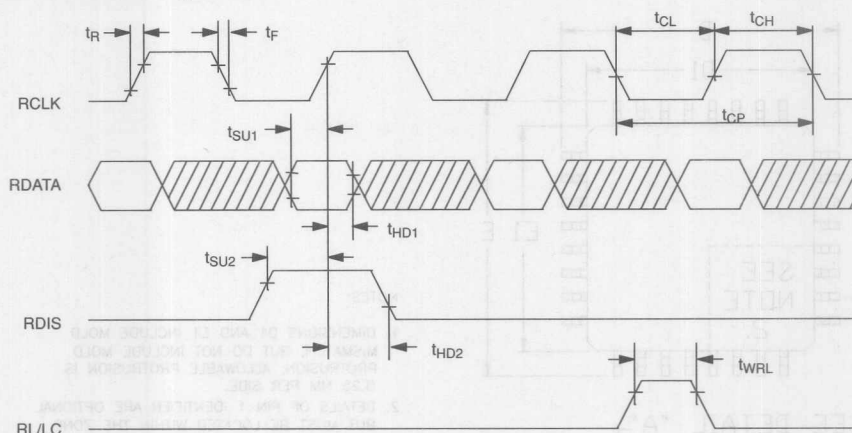
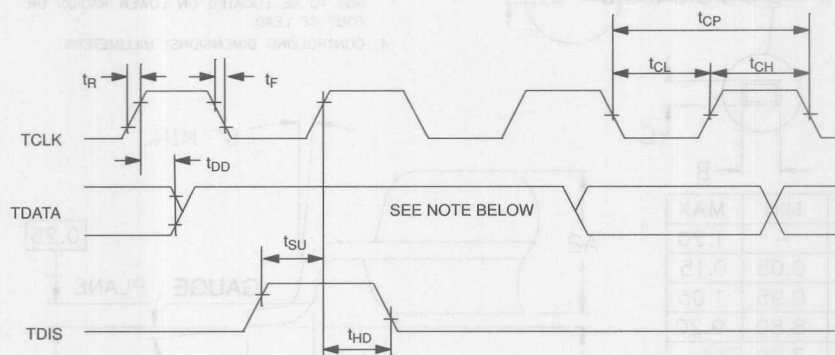
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{CP}	19			ns	
RCLK Pulse Width	t_{CH} t_{CL}	8 8			ns ns	
RDATA Set Up to RCLK Rising	t_{SU1}	4			ns	
RDATA Hold from RCLK Rising	t_{HD1}	0			ns	
REDIS Set Up to RCLK Rising	t_{SU2}	4			ns	
REDIS Hold from RCLK Rising	t_{HD2}	0			ns	
RL and LC Pulse Width	t_{WRL}	25			ns	
RLCK Rise and Fall Times	t_R, t_F			10	ns	1

AC CHARACTERISTICS – TRANSMIT SIDE(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

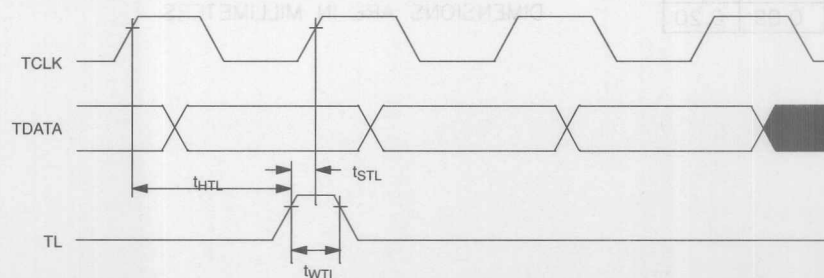
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}	19			ns	
TCLK Pulse Width	t_{CH} t_{CL}	8 8			ns ns	
TDATA Delay from TCLK Rising	t_{DD}			9	ns	
TDIS Set Up to TCLK Rising	t_{SU}	4			ns	
TDIS Hold from TCLK Rising	t_{HD}	0			ns	
TL Pulse Width	t_{WTL}	15			ns	
TL Set Up to TCLK Rising	t_{STL}	4			ns	
TL Hold Off from TCLK Rising	t_{HTL}	0			ns	
TCLK Rise and Fall Time	t_R, t_F			10	ns	1

NOTE:

1. The maximum rise and fall time is either 10 ns or 10% of t_{CP} whichever is less.

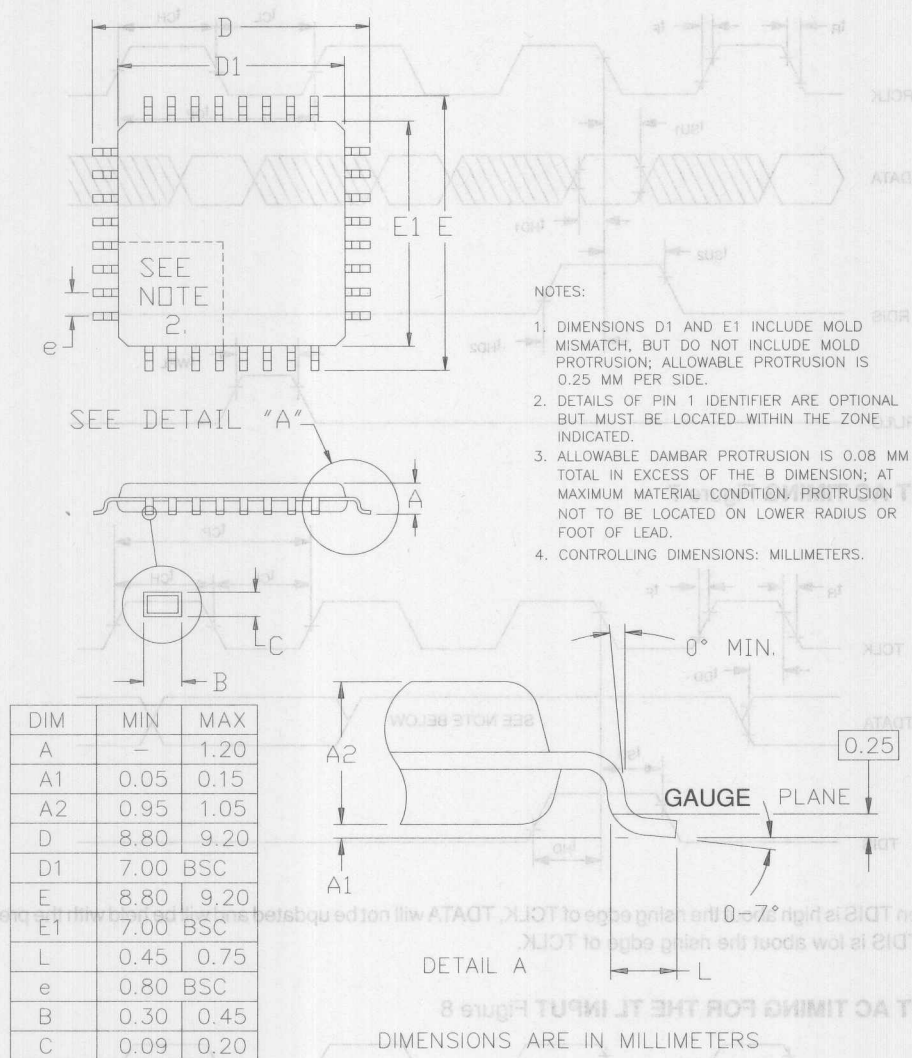
RECEIVE AC TIMING Figure 6**TRANSMIT AC TIMING Figure 7**

NOTE: When TDIS is high about the rising edge of TCLK, TDATA will not be updated and will be held with the previous value until TDIS is low about the rising edge of TCLK.

TRANSMIT AC TIMING FOR THE TL INPUT Figure 8

NOTE: The rising edge of TL causes the internal pattern generation circuitry to be reloaded; the first bit of the new pattern (the shaded one) will appear after two TCLK periods.

DS2172 32-PIN TQFP

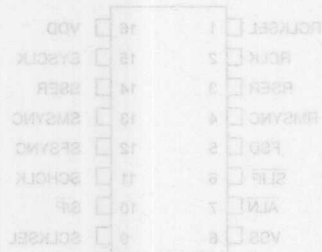


T1/CEPT (E1) ELASTIC STORES

DS2175

T1/CEPT Elastic Store

PIN ASSIGNMENT



16-PIN DIP (300 MIL)
16-PIN SOIC (300 MIL)

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on-chip "slip" control logic
 - Slips occur only on frame boundaries
 - Outputs report slip occurrences and direction
 - Align feature allows buffer to be reentered at any time
 - Buffer depth easily monitored
- Compatible with DS2180A T1 and DS2181A CEPT Transceivers
- Industrial temperature range of -40°C to +85°C available, designated DS2175N

DESCRIPTION

The DS2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1-1.544 MHz) and European (CEPT-2.048 MHz) rate networks. The chip has several flexible operating

modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunk, drop and insert equipment, digital cross-connects (DACS), private network equipment and PAXX-to-computer interfaces such as DMI and CFI.

DALLAS

SEMICONDUCTOR

DS2175

T1/CEPT Elastic Store

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 - Slips occur only on frame boundaries
 - Outputs report slip occurrences and direction
 - Align feature allows buffer to be recentered at any time
 - Buffer depth easily monitored
- Compatible with DS2180A T1 and DS2181A CEPT Transceivers
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$ available, designated DS2175N

PIN ASSIGNMENT

RCLKSEL	1	16	VDD
RCLK	2	15	SYCLK
RSER	3	14	SSER
RMSYNC	4	13	SMSYNC
FSD	5	12	SFSYNC
SLIP	6	11	SCHCLK
ALN	7	10	S/P
VSS	8	9	SCLKSEL

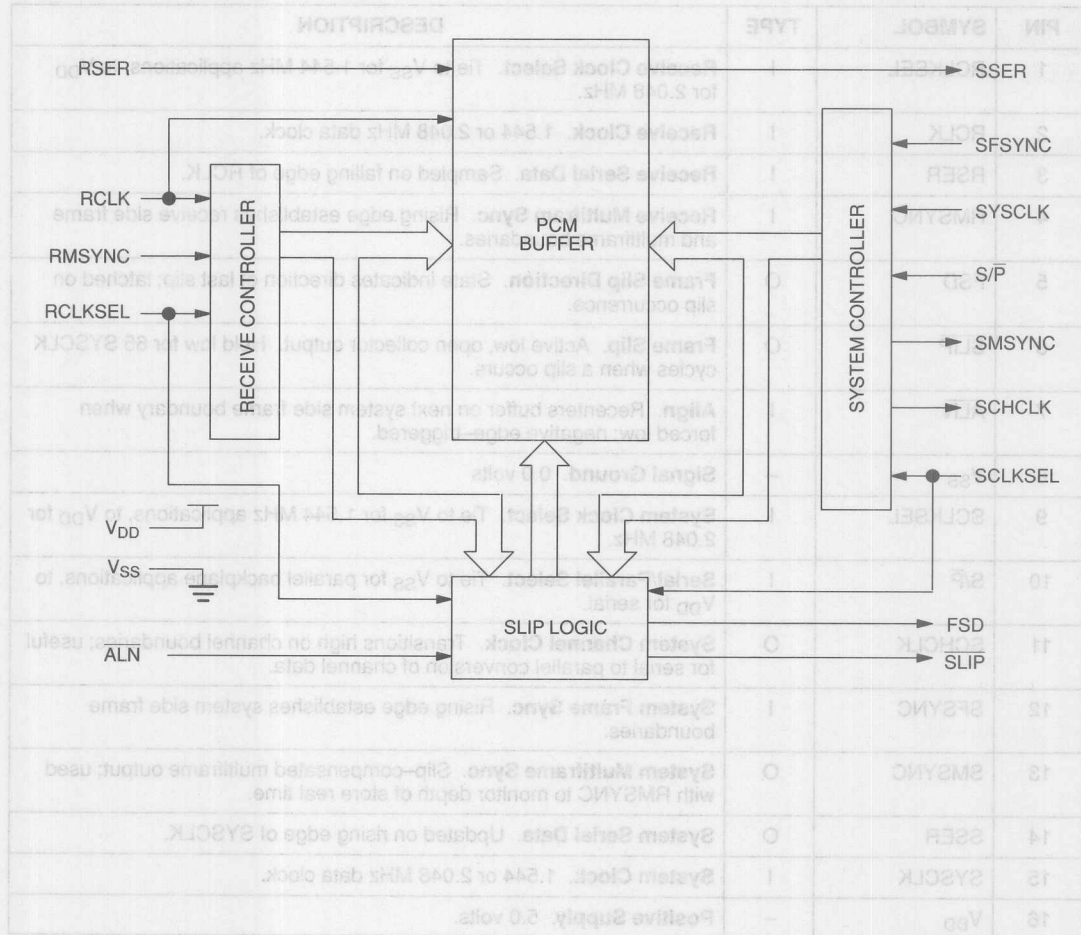
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modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross-connects (DACs), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2175 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	RCLKSEL	I	Receive Clock Select. Tie to V_{SS} for 1.544 MHz applications, to V_{DD} for 2.048 MHz.
2	RCLK	I	Receive Clock. 1.544 or 2.048 MHz data clock.
3	RSER	I	Receive Serial Data. Sampled on falling edge of RCLK.
4	RMSYNC	I	Receive Multiframe Sync. Rising edge establishes receive side frame and multiframe boundaries.
5	FSD	O	Frame Slip Direction. State indicates direction of last slip; latched on slip occurrence.
6	SLIP	O	Frame Slip. Active low, open collector output. Held low for 65 SYSCLK cycles when a slip occurs.
7	ALN	I	Align. Recenters buffer on next system side frame boundary when forced low; negative edge-triggered.
8	V_{SS}	—	Signal Ground. 0.0 volts
9	SCLKSEL	I	System Clock Select. Tie to V_{SS} for 1.544 MHz applications, to V_{DD} for 2.048 MHz.
10	S/P	I	Serial/Parallel Select. Tie to V_{SS} for parallel backplane applications, to V_{DD} for serial.
11	SCHCLK	O	System Channel Clock. Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
12	SFSYNC	I	System Frame Sync. Rising edge establishes system side frame boundaries.
13	SMSYNC	O	System Multiframe Sync. Slip-compensated multiframe output; used with RMSYNC to monitor depth of store real time.
14	SSER	O	System Serial Data. Updated on rising edge of SYSCLK.
15	SYSCLK	I	System Clock. 1.544 or 2.048 MHz data clock.
16	V_{DD}	—	Positive Supply. 5.0 volts.

PCM BUFFER

The DS2175 utilizes a 2-frame buffer to synchronize incoming PCM data to the system backplane clock. Buffer depth is mode-dependent; 2.048 MHz to 2.048 MHz applications utilize 64 bytes of buffer memory, while all other modes are supported by 48 bytes. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. The buffer depth is constantly monitored by onboard contention logic; a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

DATA FORMAT

Data is presented to, and output from, the elastic store in a "framed" format. A rising edge at RMSYNC and SFSYNC establishes frame boundaries for the receive and system sides. North American (T1) frames contain 24 data channels of 8 bits each and an F-bit (193 bits total). European (CEPT) frames contain 32 data channels (256 bits). The frame rate of both systems is 8 KHz. RMSYNC and SFSYNC do not require a pulse at every frame boundary; if desired, they may be pulsed once to establish frame alignment. Internal counters will then maintain the frame alignment and may be reinforced by the next rising edge at RMSYNC and/or SFSYNC.

SLIP CORRECTION CAPABILITY

The 2-frame buffer depth is adequate for T-carrier and CEPT applications where short term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2175 provides an ideal balance between total delay (less than 250 microseconds at its full depth) and slip correction capability.

BUFFER RECENTERING

Many applications require that the buffer be recentered during system power-up and/or initialization. Forcing ALN low recenters the buffer on the occurrence of the next frame sync boundary. A slip will occur during this

recentering if the buffer depth is adjusted. If the depth is presently optimum, no adjustment (slip) occurs.

SLIP REPORTING

SLIP is held low for 65 SYSCLK cycles when a slip occurs. SLIP is an active-low, open collector output. FSD indicates slip direction. When low (buffer empty) a frame of data was "repeated" at SSER during the previous slip. When high (buffer full), a frame of data was "deleted". FSD is updated at every slip occurrence.

BUFFER DEPTH MONITORING

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges of RMSYNC and SMSYNC indicates the current buffer depth. Impending slip conditions may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK periods.

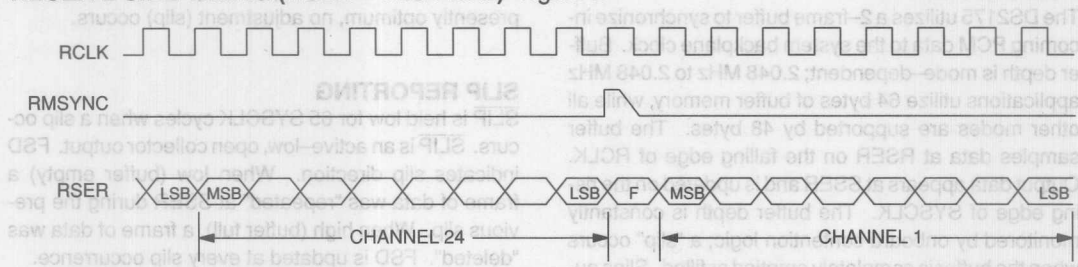
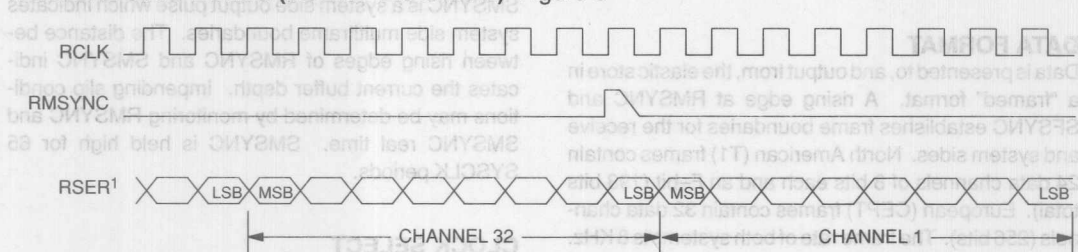
CLOCK SELECT

Receive and system side clock frequencies are independently selectable by inputs RCLKSEL and SCLKSEL. 1.544 MHz is selected when RCLKSEL (SCLKSEL) = 0; 2.048 MHz is selected when RCLKSEL (SCLKSEL) = 1. In 1.544 MHz (receive) to 1.544 MHz (system) applications, the F-bit position is passed through the receive buffer and presented at SSER immediately after the rising edge of the system side frame sync. The F-bit position is forced to 1 in 2.048 MHz to 1.544 MHz applications. No F-bit position exists in 2.048 MHz system side applications.

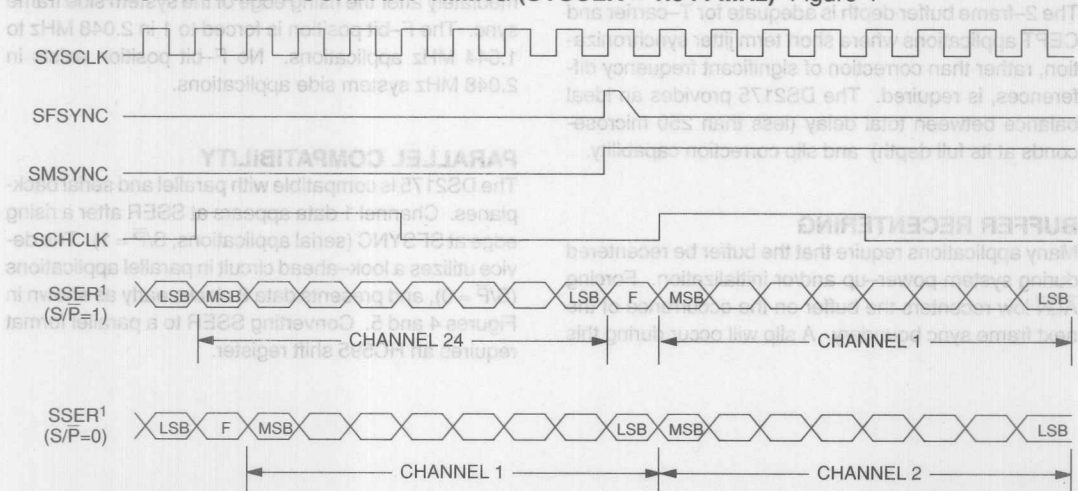
PARALLEL COMPATIBILITY

The DS2175 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC (serial applications, S/P = 1). The device utilizes a look-ahead circuit in parallel applications (S/P = 0), and presents data 8 clocks early as shown in Figures 4 and 5. Converting SSER to a parallel format requires an HC595 shift register.



RECEIVE SIDE TIMING (RCLK = 1.544 MHz) Figure 2**RECEIVE SIDE TIMING (RCLK = 2.048 MHz) Figure 3****NOTES:**

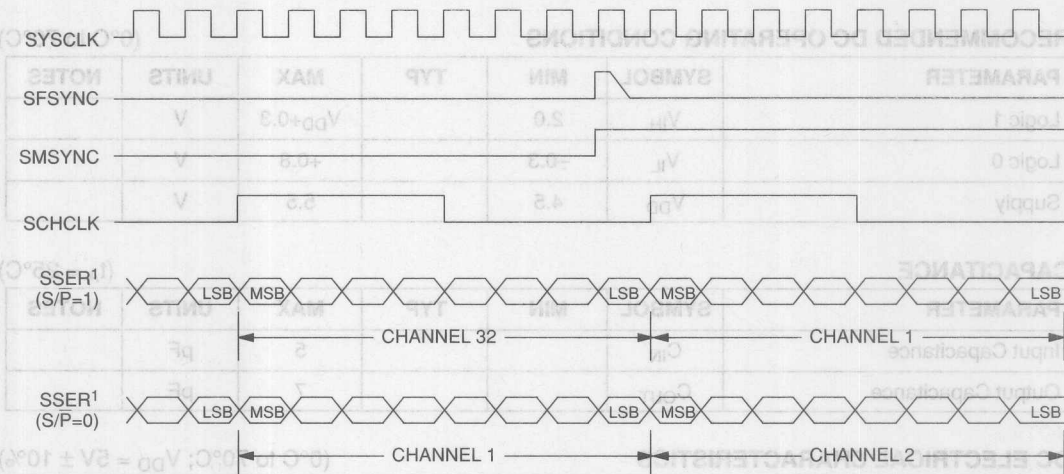
1. All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1);
2. Data in channels >24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHz) Figure 4

NOTES:

- 1. In 1.544 MHz receive side applications (RCLKSEL=0), the F-bit position contains F-bit data extracted from the data stream at RSER. The F-bit position is forced to "1" in 2.048 MHz receive side applications (RCLKSEL=1).
- 2. In 2.048 MHz receive side applications (RCLKSEL=1), the E-bit position is forced to "1" and data in channels >24 is ignored.

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHz) Figure 5



NOTES:

- 1. In 2.048 MHz receive side applications (RCLKSEL=1), all channel data is passed through the elastic store.
- 2. In 1.544 MHz receive side applications (RCLKSEL=0), all channel data is passed through the elastic store, except the F-bit position which is ignored. Data in channels >24 on the system side is forced to all ones.

Storage temperature
Soldering Temperature

–55°C to 125°C
260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

($t_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		9	16	mA	1, 2
Input Leakage	I_{IL}	–1.0		+1.0	μA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	3
Output Current @ 0.4V	I_{OL}	+4.0			mA	4

NOTES:

1. $\text{SYSCLK} = \text{RCLK} = 2.048 \text{ MHz}$
2. Outputs open
3. All outputs except $\overline{\text{SLIP}}$, which is open collector
4. All outputs

AC ELECTRICAL CHARACTERISTICS

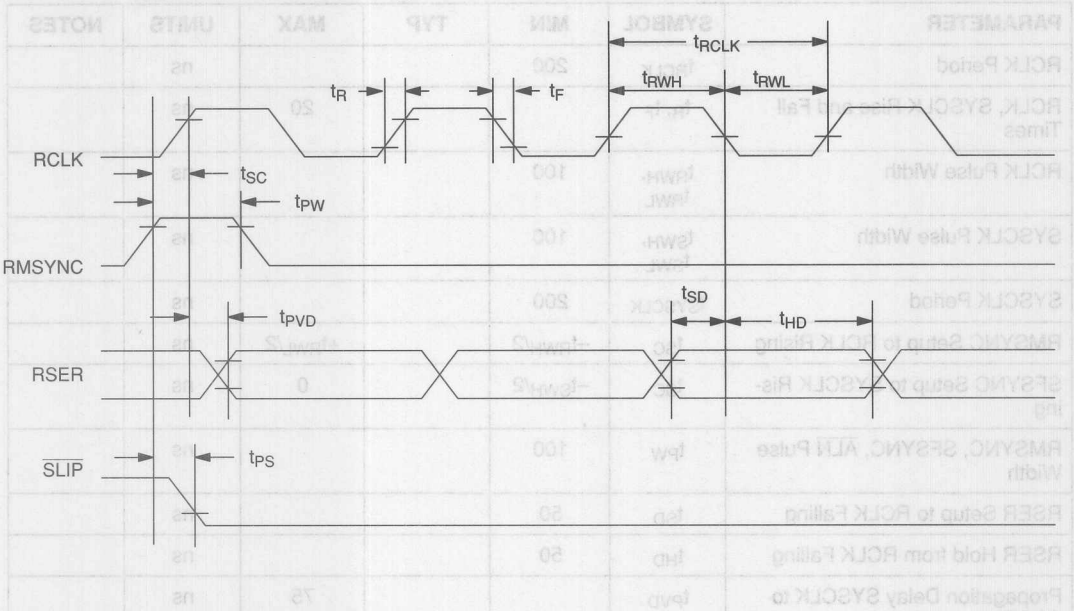
(0°C to 70°C; $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	200			ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH}, t_{RWL}	100			ns	
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100			ns	
SYSCLK Period	t_{SYSCLK}	200			ns	
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns	
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		0	ns	
RMSYNC, SFSYNC, ALN Pulse Width	t_{PW}	100			ns	
RSER Setup to RCLK Falling	t_{SD}	50			ns	
RSER Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to SSER	t_{PVD}			75	ns	
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to SLIP Low, FSD Low/High	t_{PS}			100	ns	
ALN Setup to SFSYNC Rising	t_{SR}	500			ns	

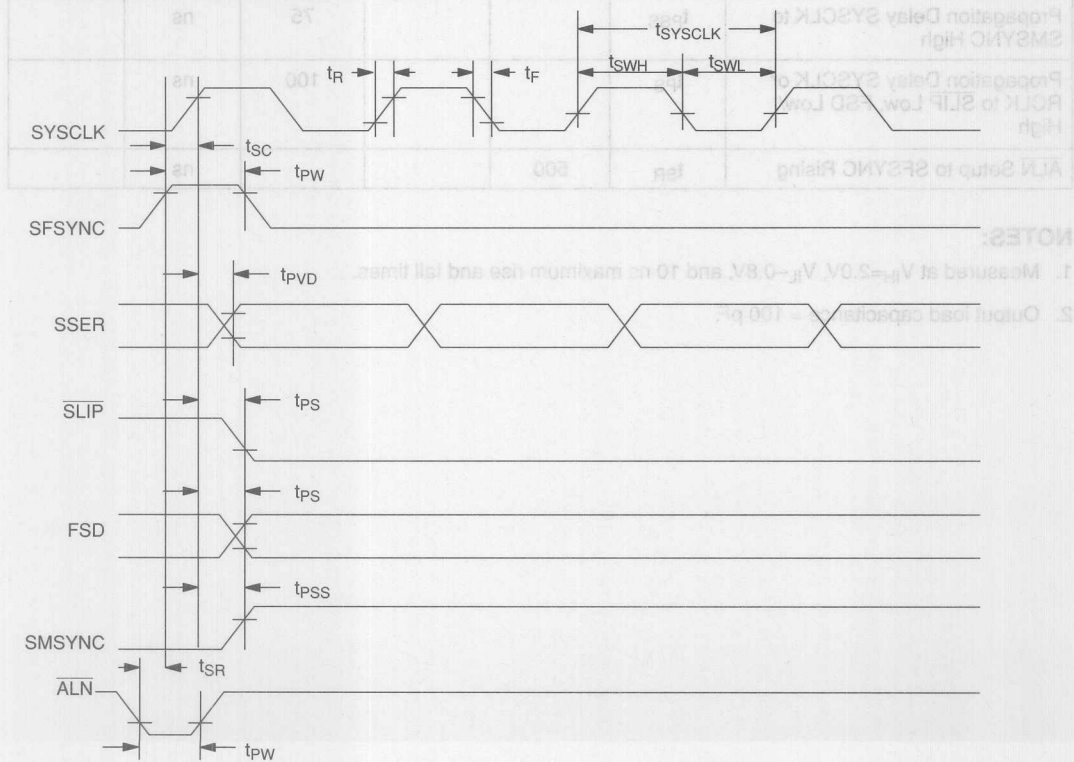
NOTES:

1. Measured at $V_{IH}=2.0V$, $V_{IL}=0.8V$, and 10 ns maximum rise and fall times.
2. Output load capacitance = 100 pF.

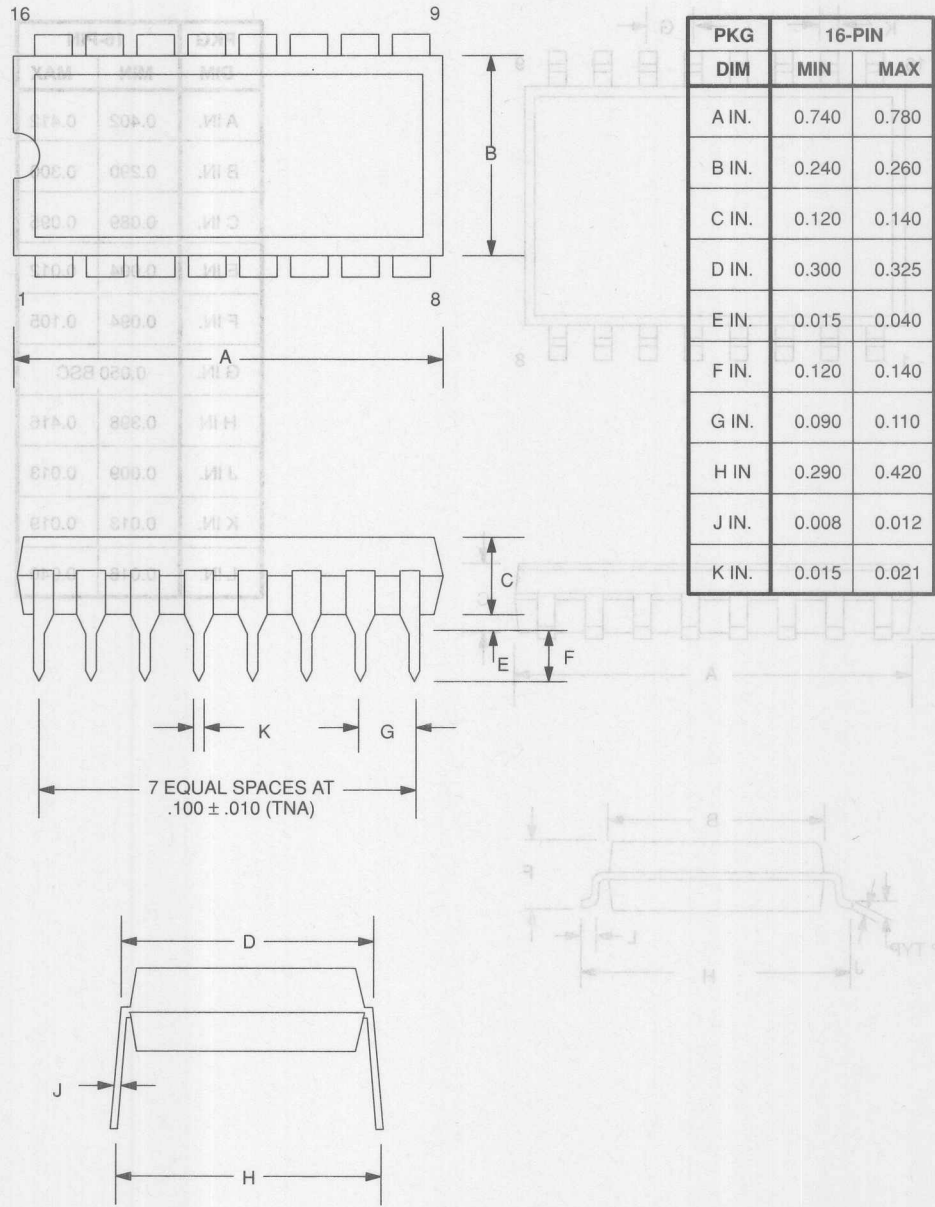
RECEIVE AC TIMING DIAGRAM Figure 6



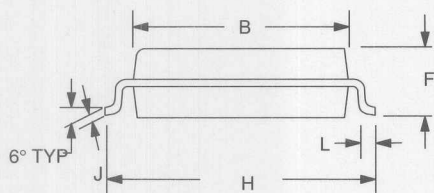
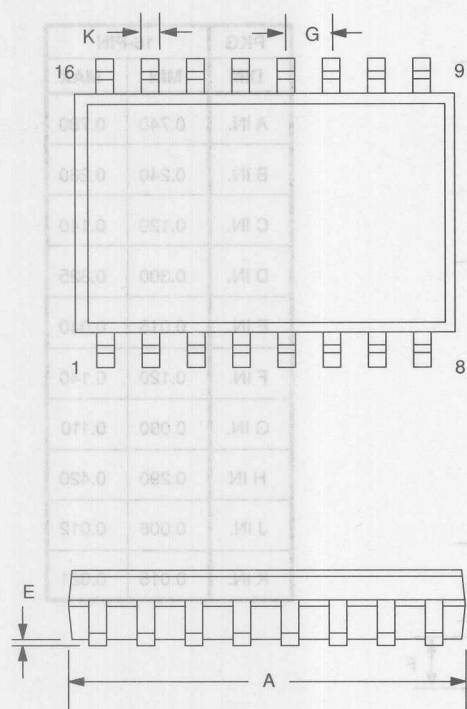
SYSTEM AC TIMING DIAGRAM Figure 7



DS2175 T1/CEPT ELASTIC STORE



DS2175S T1/CEPT ELASTIC STORE



PKG	16-PIN	
DIM	MIN	MAX
A IN.	0.402	0.412
B IN.	0.290	0.300
C IN.	0.089	0.095
E IN.	0.004	0.012
F IN.	0.094	0.105
G IN.	0.050 BSC	
H IN	0.398	0.416
J IN.	0.009	0.013
K IN.	0.013	0.019
L IN.	0.016	0.040

DALLAS

SEMICONDUCTOR

DS2176

T1 Receive Buffer

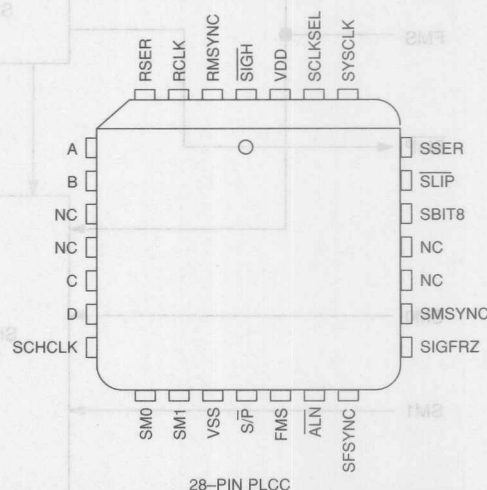
FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$ available, designated DS2176N

PIN ASSIGNMENT

SIGH	1	24	VDD
RMSYNC	2	23	SCLKSEL
RCLK	3	22	SYSCLK
RSER	4	21	SSER
A	5	20	SLIP
B	6	19	SBIT8
C	7	18	SMSYNC
D	8	17	SIGFRZ
SCHCLK	9	16	SFSYNC
SM0	10	15	ALN
SM1	11	14	FMS
VSS	12	13	S/P

24-PIN 300 MIL DIP



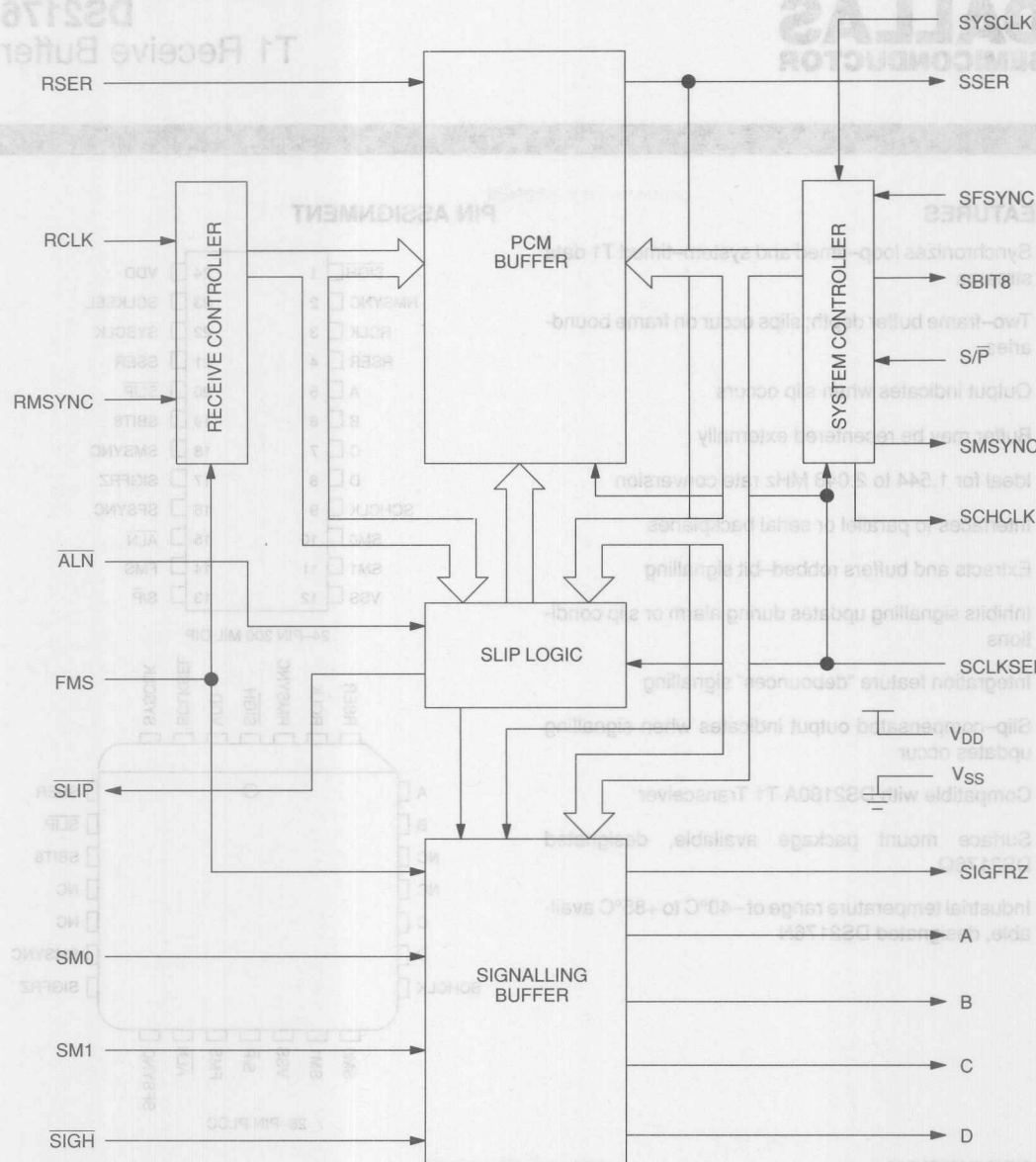
28-PIN PLCC

DESCRIPTION

The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during

alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACs), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2176 BLOCK DIAGRAM Figure 1



ing alarm or slip conditions. The buffer replaces exten-
sive hardware in existing applications with one "skinny"
24-lead package. Application areas include digital
trunk, drop and insert equipment, transcoders, digital
cross-connects (DACS), private network equipment,
and PBX-to-computer interfaces such as DMI and
CPI.

The DS2176 is a low-power CMOS device specifically
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PIN DESCRIPTION Table 1

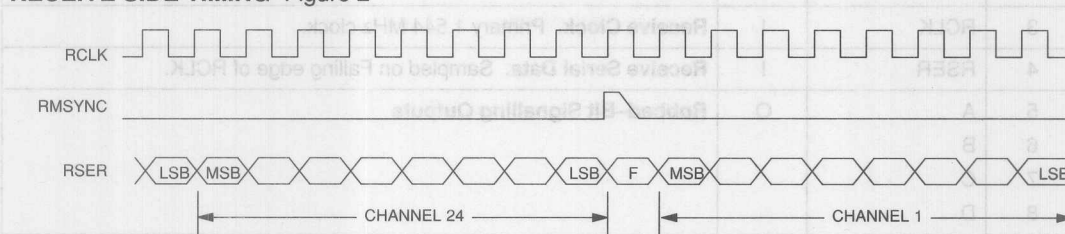
PIN	SYMBOL	TYPE	DESCRIPTION
1	SIGH	I	Signalling Inhibit. When low, ABCD signalling updates are disabled for a period determined by SM0 and SM1, or until returned high.
2	RMSYNC	I	Receive Multiframe Sync. Must be pulsed high at multiframe boundaries to establish frame and multiframe alignment.
3	RCLK	I	Receive Clock. Primary 1.544 MHz clock.
4	RSER	I	Receive Serial Data. Sampled on Falling edge of RCLK.
5	A	O	Robbed-Bit Signalling Outputs
6	B		
7	C		
8	D		
9	SCHCLK	O	System Channel Clock. Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
10	SM0	I	Signalling Modes 0 and 1. Select signalling supervision technique.
11	SM1	I	
12	V _{SS}	—	Signal Ground. 0.0 volts.
13	S/P	I	Serial/Parallel Select. Tie to V _{SS} for parallel backplane applications, to V _{DD} for serial.
14	FMS	I	Frame Mode Select. Tie to V _{SS} to select 193S (D4) framing to V _{DD} for 193E (extended).
15	ALN	I	Align. Recenters buffer on next system side frame boundary when forced low.
16	SFSYNC	I	System Frame Sync. Rising edge establishes start of frame.
17	SIGFRZ	O	Signalling Freeze. When high, indicates signalling updates have been disabled internally via a slip or externally by forcing SIGH low.
18	SMSYNC	O	System Multiframe Sync. Slip-compensated multiframe output; indicates when signalling updates are made.
19	SBIT8	O	System Bit 8. High during the LSB time of each channel. Used to reinsert extracted signalling into outgoing data stream.
20	SLIP	O	Frame Slip. Active low, open collector output. Held low for 65 SYSCLK cycles when a slip occurs.
21	SSER	O	System Serial Out. Updated on rising edge of SYSCLK.
22	SYSCLK	I	System Clock. 1.544 or 2.048 MHz data clock.
23	SCLKSEL	I	System Clock Select. Tie to V _{SS} for 1.544 MHz applications, to V _{DD} for 2.048 MHz.
24	V _{DD}	—	Positive Supply. 5.0 volts.

OVERVIEW

The DS2176 performs two primary functions: 1) *synchronization* of received T1 PCM data (looped timed) to host backplane frequencies; 2) *supervision* of robbed-bit signalling data embedded in the data stream. The

buffer, while optimized for use with the DS2180A T1 Transceiver, is also compatible with other transceiver devices. The DS2180A data sheet should serve as a valuable reference when designing with the DS2176.

RECEIVE SIDE TIMING Figure 2



DATA SYNCHRONIZATION

PCM BUFFER

The DS2176 utilizes a 2-frame buffer (386 bits) to synchronize incoming PCM data to the system backplane clock. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. A rising edge at RMSYNC establishes receive side frame and multi-frame alignment. A rising edge at SFSYNC establishes system side frame alignment. The buffer depth is constantly monitored by onboard contention logic; a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

SLIP CORRECTION CAPABILITY

The 2-frame buffer depth is adequate for most T-carrier applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2176 provides an ideal balance between total delay and slip correction capability.

BUFFER RECENTERING

Many applications require that the buffer be recentered during system power-up and/or initialization. Forcing ALN low recenters the buffer on the occurrence of the next frame sync boundary. A slip will occur during this recentering if the buffer depth is adjusted. If the depth is presently optimum, no adjustment (slip) occurs. SLIP is held low for 65 SYSCLK cycles when a slip occurs. SLIP is an active-low, open collector output.

BUFFER DEPTH MONITORING

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK cycles.

CLOCK SELECT

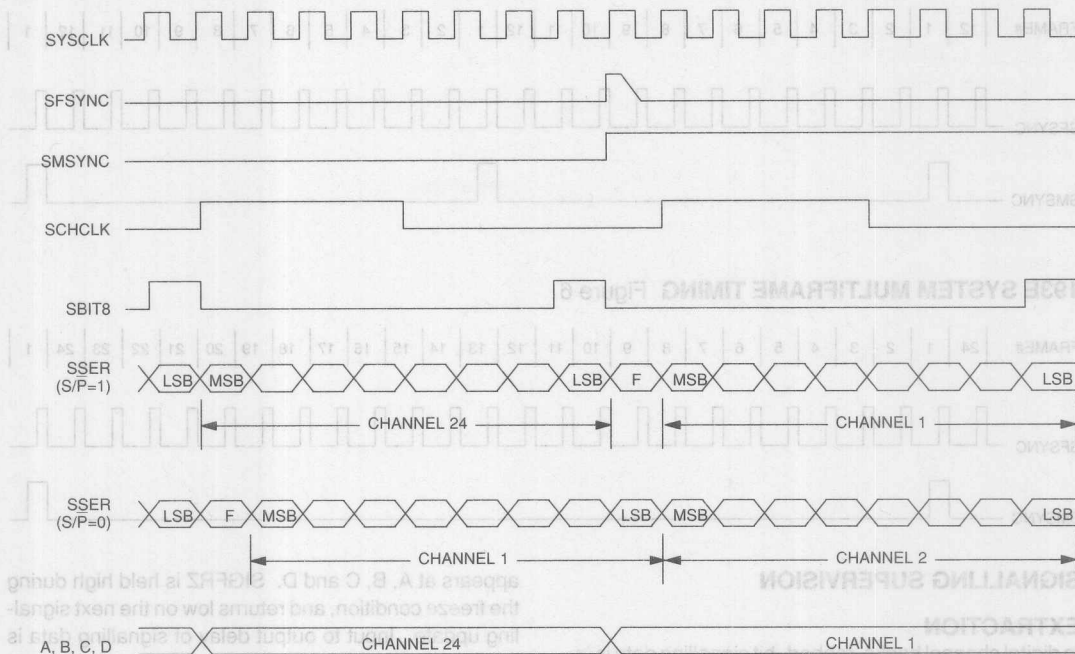
The device is compatible with two common backplane frequencies: 1.544 MHz, selected when SCLKSEL=0; and 2.048 MHz, selected when SCLKSEL=1. In 1.544 MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after the rising edge of the system side frame sync. The F-bit is dropped in 2.048 MHz applications and the MSB of channel 1 appears at SSER one bit period after a rising edge at SFSYNC. SSER is forced to 1 in all channels greater than 24. See Figures 3 and 4.

In 2.048 MHz applications (SCLKSEL=1), the PCM buffer control logic establishes slip criteria different from that used in 1.544 MHz applications to compensate for the faster system-side read frequency.

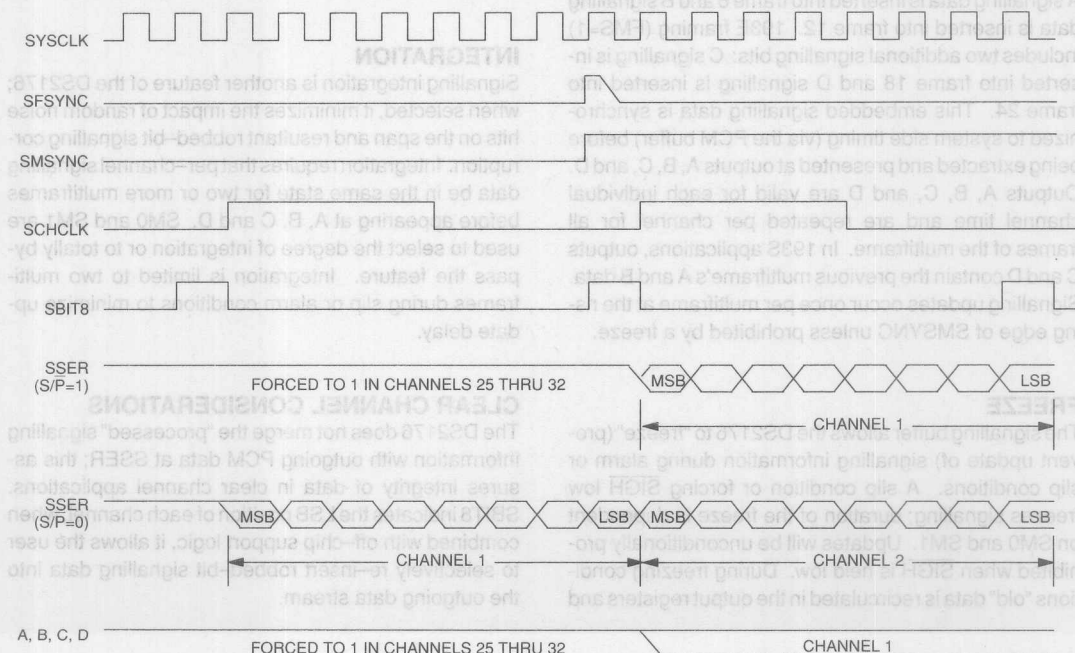
PARALLEL COMPATIBILITY

The DS2176 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC as shown in Figures 3 and 4 (serial applications, S/P=1). The device utilizes a look-ahead circuit in parallel applications (S/P=0). Data is output 8 clocks earlier, allowing the user to convert parallel data externally.

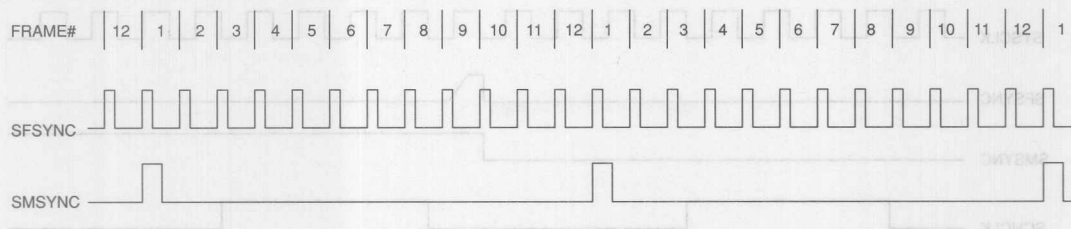
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHz) Figure 3



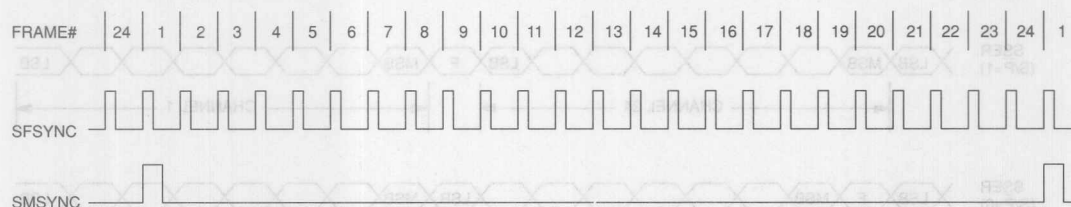
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHz) Figure 4



193S SYSTEM MULTIFRAME TIMING Figure 5



193E SYSTEM MULTIFRAME TIMING Figure 6



SIGNALLING SUPERVISION

EXTRACTION

In digital channel banks, robbed-bit signalling data is inserted into the LSB position of each channel during signalling frames. In 193S framing (FMS=0) applications, A signalling data is inserted into frame 6 and B signalling data is inserted into frame 12. 193E framing (FMS=1) includes two additional signalling bits: C signalling is inserted into frame 18 and D signalling is inserted into frame 24. This embedded signalling data is synchronized to system side timing (via the PCM buffer) before being extracted and presented at outputs A, B, C, and D. Outputs A, B, C, and D are valid for each individual channel time and are repeated per channel for all frames of the multiframe. In 193S applications, outputs C and D contain the previous multiframe's A and B data. Signalling updates occur once per multiframe at the rising edge of SMSYNC unless prohibited by a freeze.

FREEZE

The signalling buffer allows the DS2176 to "freeze" (prevent update of) signalling information during alarm or slip conditions. A slip condition or forcing SIGH low freezes signalling; duration of the freeze is dependent on SM0 and SM1. Updates will be unconditionally prohibited when SIGH is held low. During freezing conditions "old" data is recirculated in the output registers and

appears at A, B, C and D. SIGFRZ is held high during the freeze condition, and returns low on the next signalling update. Input to output delay of signalling data is equal to 1 multiframe (the depth of the signalling buffer) + the current depth of the PCM buffer (1 frame \pm approximately 1 frame).

INTEGRATION

Signalling integration is another feature of the DS2176; when selected, it minimizes the impact of random noise hits on the span and resultant robbed-bit signalling corruption. Integration requires that per-channel signalling data be in the same state for two or more multiframes before appearing at A, B, C and D. SM0 and SM1 are used to select the degree of integration or to totally bypass the feature. Integration is limited to two multiframes during slip or alarm conditions to minimize update delay.

CLEAR CHANNEL CONSIDERATIONS

The DS2176 does not merge the "processed" signalling information with outgoing PCM data at SSER; this assures integrity of data in clear channel applications. SBIT8 indicates the LSB position of each channel; when combined with off-chip support logic, it allows the user to selectively re-insert robbed-bit signalling data into the outgoing data stream.

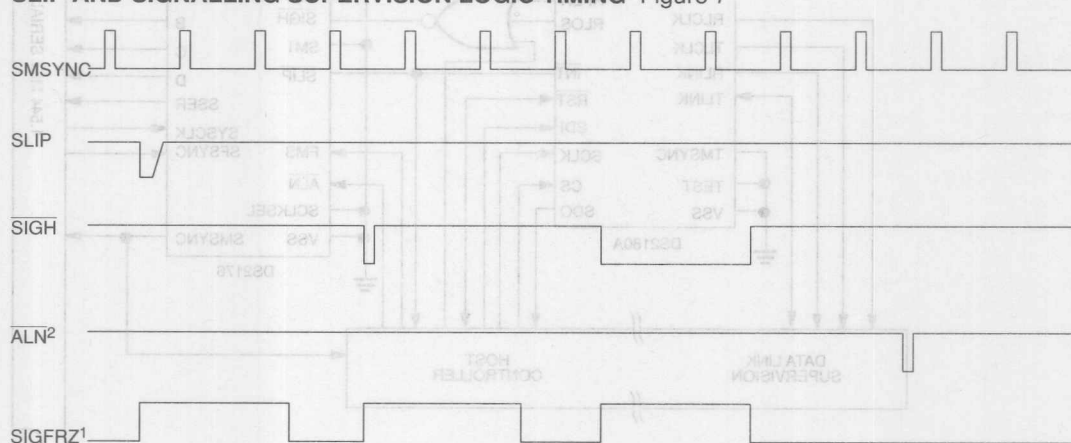
SIGNALLING SUPERVISION MODES Table 2

SM0	SM1	FMS	SELECTED MODE
0	0	0	193S framing, no integration, 1 multiframe freeze.
0	0	1	193E framing, no integration, 1 multiframe freeze.
0	1	0	193S framing, 2 multiframe integration and freeze.
0	1	1	193E framing, 2 multiframe integration and freeze.
1	0	0 ¹	193S framing, 5 multiframe integration, 2 multiframe freeze.
1	0	1 ¹	193E framing, 3 multiframe integration, 2 multiframe freeze.
1	1	0	193S framing, no integration, 1 multiframe freeze, replace robbed bit signaling bits at SSER with ones.
1	1	1	193E framing, no integration, 1 multiframe freeze, replace robbed bit signalling bits at SSER with ones.

NOTE:

1. During slip or alarm conditions, integration is limited to two multiframe to minimize signalling delay.

SLIP AND SIGNALLING SUPERVISION LOGIC TIMING Figure 7

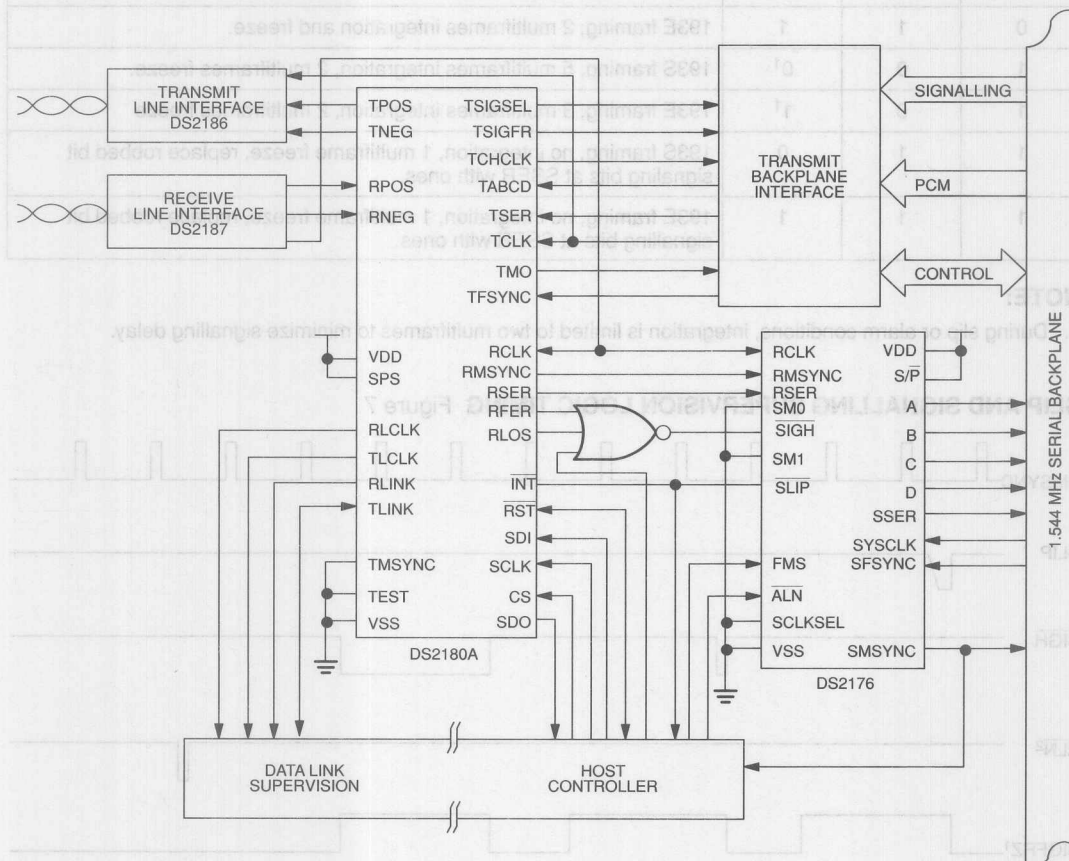
**NOTES:**

1. Integration feature disabled (SM0=SM1=0) in timing set shown.
2. Depending on present buffer depth, forcing ALN low may or may not cause a slip condition.

DS2176/DS2180A SYSTEM APPLICATION

Figure 8 shows how the DS2180A T1 Transceiver and DS2176 Receive Buffer interconnect in a typical application.

SERIAL 1.544 MHz BACKPLANE INTERFACE Figure 8



Storage temperature -55°C to 125°C
 Soldering Temperature 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		5	10	mA	1, 2
Input Leakage	I_{IL}	-1.0		+1.0	μA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	3
Output Current @ 0.4V	I_{OL}	+4.0			mA	4
Output Leakage	I_{LO}	-1.0		+1.0	μA	5

NOTES:

1. $TCLK=RCLK=1.544$ MHz.
2. Outputs open.
3. All outputs except \overline{SLIP} , which is open collector.
4. All outputs.
5. Applies to \overline{SLIP} when tri-stated.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD}=5V ± 10%)

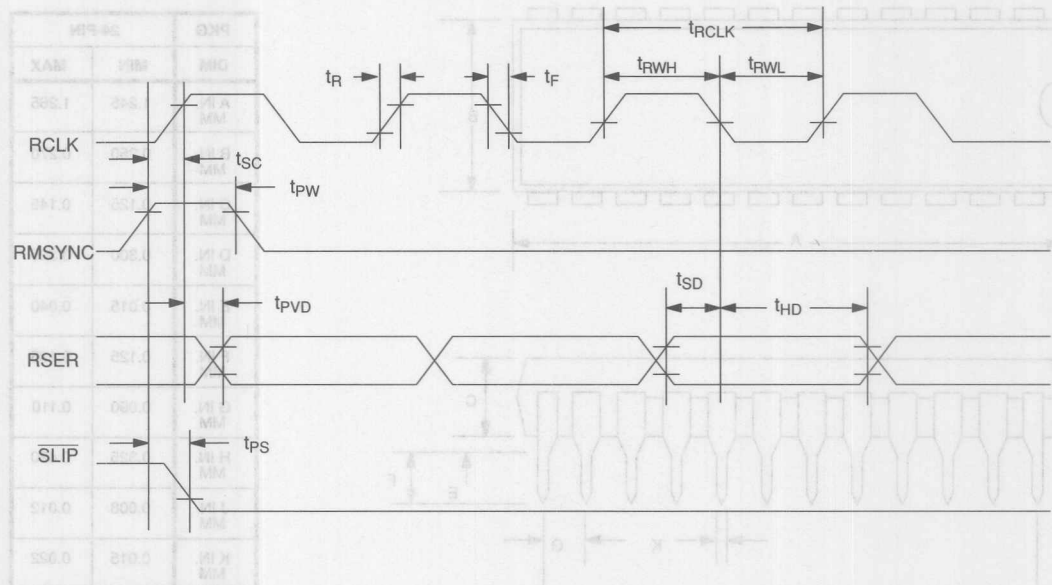
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t _{RCLK}	250	648		ns	
RCLK, SYSCLK Rise and Fall Times	t _R , t _F			20	ns	
RCLK Pulse Width	t _{RWH} , t _{RWL}	125	324		ns	
SYSCLK Pulse Width	t _{SWH} , t _{SWL}	100	244		ns	
SYSCLK Period	t _{SYSCLK}	200	488		ns	
RMSYNC Setup to RCLK Rising	t _{SC}	-t _{RWH} /2		+t _{RWL} /2	ns	
SFSYNC Setup to SYSCLK Rising	t _{SC}	-t _{SWH} /2		+t _{SWL} /2	ns	
RMSYNC, SFSYNC, SIGH, ALN Pulse Width	t _{PW}	100		ns		
RSER Setup to RCLK Falling	t _{SD}	50			ns	
RSER Hold from RCLK Falling	t _{HD}	50			ns	
Propagation Delay SYSCLK to SSER, A, B, C, D	t _{PVD}			100	ns	
Propagation Delay SYSCLK to SMSYNC High	t _{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to SLIP Low	t _{PS}			100	ns	
Propagation Delay SYSCLK to SIGFRZ Low/High	t _{PSF}			75	ns	
ALN, SIGH Setup to SFSYNC Rising	t _{SR}	500			ns	

NOTES:

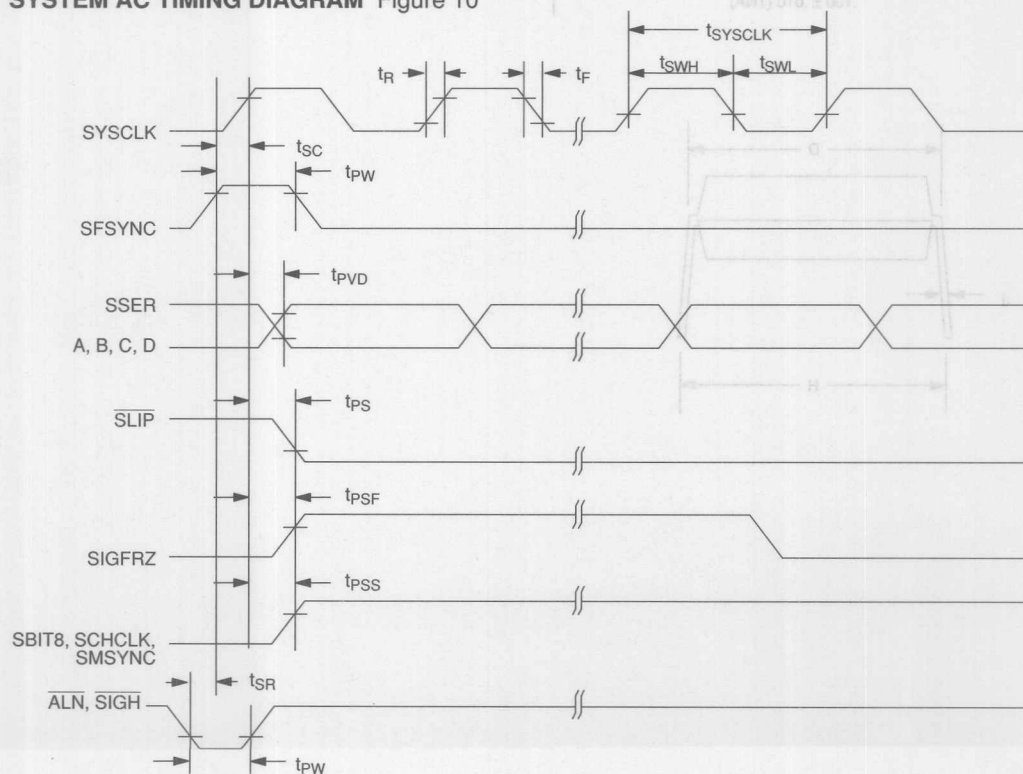
- 1. Measured at V_{IH}=2.0V, V_{IL}=0.8V, and 10 ns maximum rise and fall times.
- 2. Output load capacitance = 100 pF.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C _{IN}			5	pF	
Output Capacitance	C _{OUT}			7	pF	

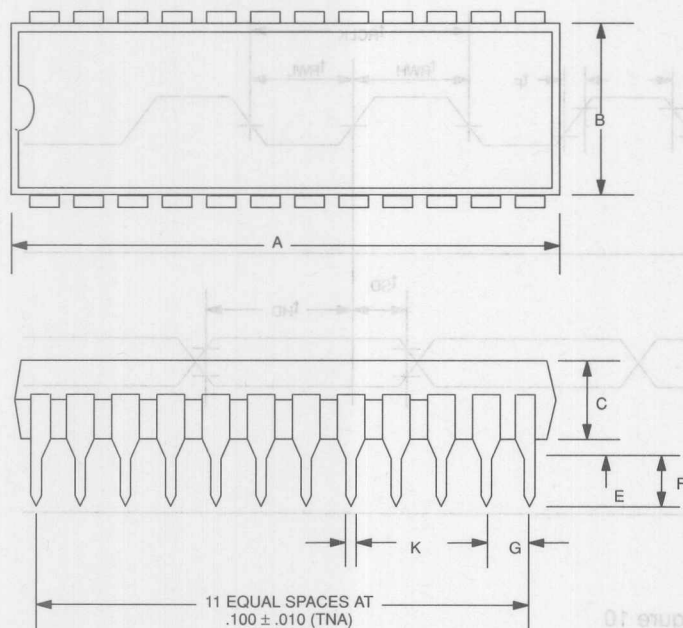
RECEIVE AC DIAGRAM Figure 9



SYSTEM AC TIMING DIAGRAM Figure 10

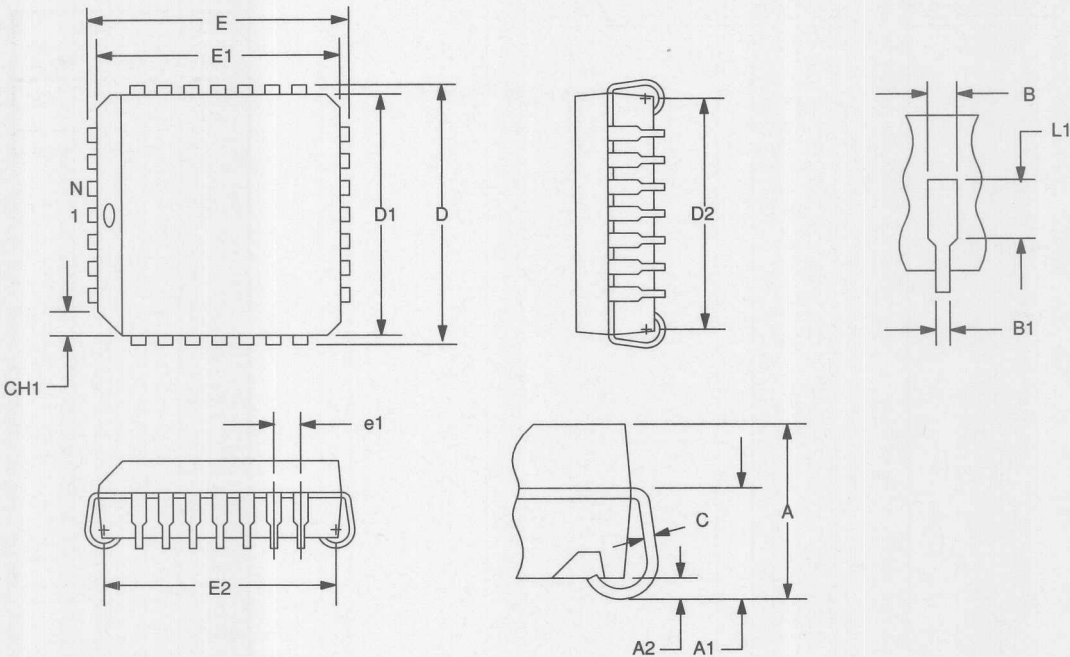


DS2176 T1 RECEIVE BUFFER

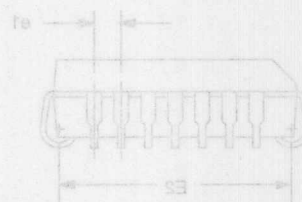
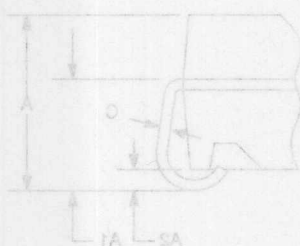
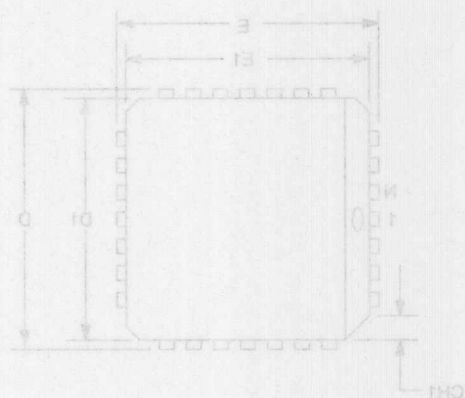
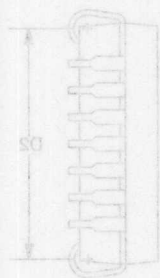
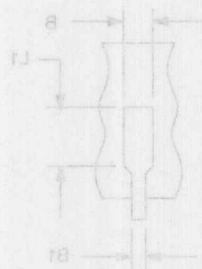


PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.245	1.265
B IN. MM	0.250	0.270
C IN. MM	0.125	0.145
D IN. MM	0.300	0.325
E IN. MM	0.015	0.040
F IN. MM	0.125	0.135
G IN. MM	0.090	0.110
H IN. MM	0.325	0.420
J IN. MM	0.008	0.012
K IN. MM	0.015	0.022

DS2176Q



DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	—
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	—
N	28	—
e1	0.050 BSC	
CH1	0.042	0.048



DIM	INCHES	
	MIN	MAX
A	0.182	0.187
A1	0.000	0.120
A2	0.020	—
B	0.020	0.030
B1	0.013	0.021
C	0.008	0.015
D	0.482	0.485
D1	0.420	0.422
D5	0.380	0.430
E	0.482	0.485
E1	0.420	0.422
E2	0.380	0.430
L1	0.020	—
N	1/8	—
e1	0.020 BSC	
CH1	0.042	0.049

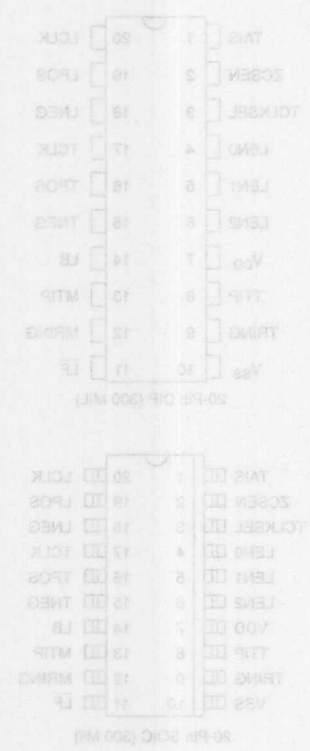
Key on-chip components include: programmable wave-
shaping circuitry, line drivers, remote feedback, and
zero suppression logic. A line-coupling transformer is
the only external component required.

DESCRIPTION
The DS2188 T1/CEPT Transceiver Line Interface Chip in-
tegrates user equipment to North American (T1-1.544
MHz) and European (CEPT-2.048 MHz) primary rate
communications networks. The device is compatible
with all types of twisted pair and coax cable found in
such networks.

- Single 5V supply; low-power CMOS technology
- Companion to the DS2187 Receive Line Interface
and DS2188 T1/CEPT Jitter Attenuator
- Compatible with DS2180A T1 and DS2181A CEPT
Transceivers DS2141A T1 and DS2143 E1 Control
Interface
- Transceiver B8ZS and HDB3 zero code suppression
modes
- Supports bipolar and unipolar input data formats
and long-loop applications
- Programmable output pulse shape supports short-
eliminate external components
- On-chip transmit LBO (line build out) and line drivers
eliminate external components
- Line interface for T1 (1.544 MHz) and CEPT (2.048
MHz) primary rate networks

FEATURES

PIN ASSIGNMENT



Application areas include: DACS, CPU, CPU channel
panels, and PABX-to-computer interfaces such as DMI
and CPT. The DS2188 supports ISDN-PRI (Primary
Rate Interface) specifications.

Short loop (DSX-1, 0 to 855 feet) and long loop (CEU-0
dB, -7.5 dB and -15 dB) pulse templates found in T1
applications are supported. Appropriate CCITT recom-
mendations are met in the CEPT mode.

DALLAS

SEMICONDUCTOR

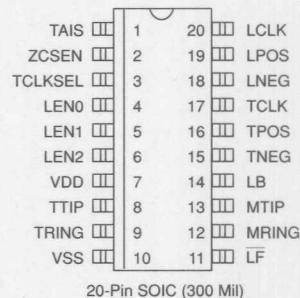
DS2186

Transmit Line Interface

FEATURES

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- On-chip transmit LBO (line build out) and line drivers eliminate external components
- Programmable output pulse shape supports short- and long-loop applications
- Supports bipolar and unipolar input data formats
- Transparent B8ZS and HDB3 zero code suppression modes
- Compatible with DS2180A T1 and DS2181A CEPT Transceivers DS2141A T1 and DS2143 E1 Controllers
- Companion to the DS2187 Receive Line Interface and DS2188 T1/CEPT Jitter Attenuator
- Single 5V supply; low-power CMOS technology

PIN ASSIGNMENT



DESCRIPTION

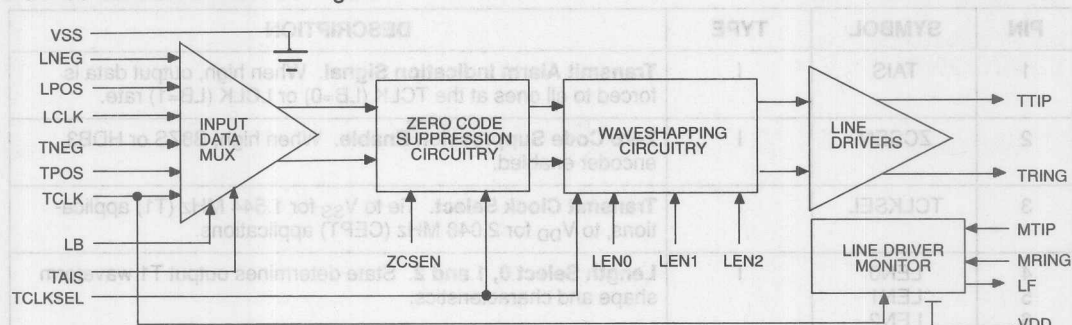
The DS2186 T1/CEPT Transmit Line Interface Chip interfaces user equipment to North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks.

Key on-chip components include: programmable wave shaping circuitry, line drivers, remote loopback, and zero suppression logic. A line-coupling transformer is the only external component required.

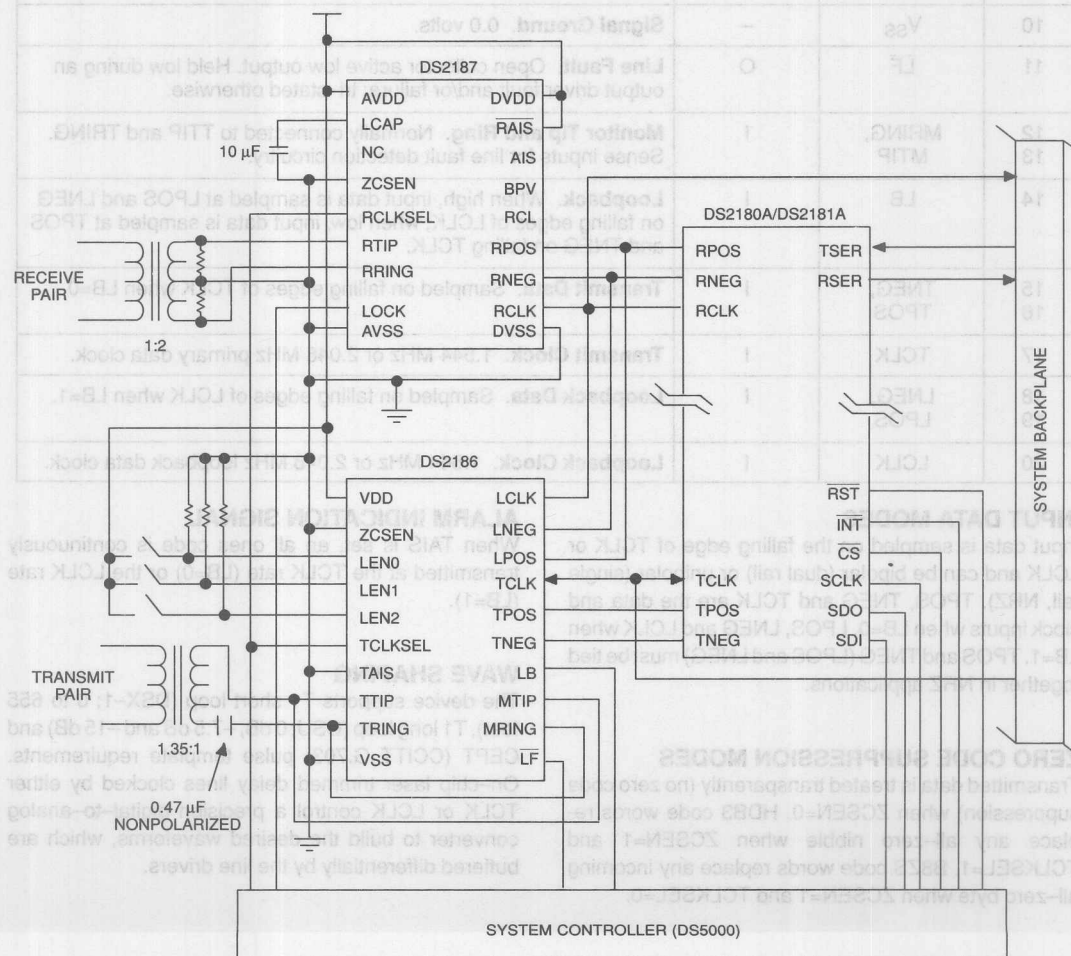
Short loop (DSX-1, 0 to 655 feet) and long loop (CSU; 0 dB, -7.5 dB and -15 dB) pulse templates found in T1 applications are supported. Appropriate CCITT recommendations are met in the CEPT mode.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI. The DS2186 supports ISDN-PRI (Primary Rate Interface) specifications.

DS2186 BLOCK DIAGRAM Figure 1



SYSTEM LEVEL INTERCONNECT Figure 2



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TAIS	I	Transmit Alarm Indication Signal. When high, output data is forced to all ones at the TCLK (LB=0) or LCLK (LB=1) rate.
2	ZCSEN	I	Zero Code Suppression Enable. When high, B8ZS or HDB3 encoder enabled.
3	TCLKSEL	I	Transmit Clock Select. Tie to V _{SS} for 1.544 MHz (T1) applications, to V _{DD} for 2.048 MHz (CEPT) applications.
4 5 6	LEN0 LEN1 LEN2	I	Length Select 0, 1 and 2. State determines output T1 waveform shape and characteristics.
7	V _{DD}	–	Positive Supply. 5.0 volts.
8 9	TTIP, TRING	O	Transmit Tip and Ring. Line driver outputs; connect to transmit line transformer.
10	V _{SS}	–	Signal Ground. 0.0 volts.
11	LF	O	Line Fault. Open collector active low output. Held low during an output driver fault and/or failure; tri-stated otherwise.
12 13	MRING, MTIP	I	Monitor Tip and Ring. Normally connected to TTIP and TRING. Sense inputs for line fault detection circuitry.
14	LB	I	Loopback. When high, input data is sampled at LPOS and LNEG on falling edges of LCLK; when low, input data is sampled at TPOS and TNEG on falling TCLK.
15 16	TNEG, TPOS	I	Transmit Data. Sampled on falling edges of TCLK when LB=0.
17	TCLK	I	Transmit Clock. 1.544 MHz or 2.048 MHz primary data clock.
18 19	LNEG, LPOS	I	Loopback Data. Sampled on falling edges of LCLK when LB=1.
20	LCLK	I	Loopback Clock. 1.544 MHz or 2.048 MHz loopback data clock.

INPUT DATA MODES

Input data is sampled on the falling edge of TCLK or LCLK and can be bipolar (dual rail) or unipolar (single rail, NRZ). TPOS, TNEG and TCLK are the data and clock inputs when LB=0, LPOS, LNEG and LCLK when LB=1. TPOS and TNEG (LPOS and LNEG) must be tied together in NRZ applications.

ZERO CODE SUPPRESSION MODES

Transmitted data is treated transparently (no zero code suppression) when ZCSEN=0. HDB3 code words replace any all-zero nibble when ZCSEN=1 and TCLKSEL=1. B8ZS code words replace any incoming all-zero byte when ZCSEN=1 and TCLKSEL=0.

ALARM INDICATION SIGNAL

When TAIS is set, an all ones code is continuously transmitted at the TCLK rate (LB=0) or the LCLK rate (LB=1).

WAVE SHAPING

The device supports T1 short loop (DSX-1; 0 to 655 feet), T1 long loop (CSU; 0 dB, –7.5 dB and –15 dB) and CEPT (CCITT G.703) pulse template requirements. On-chip laser trimmed delay lines clocked by either TCLK or LCLK control a precision digital-to-analog converter to build the desired waveforms, which are buffered differentially by the line drivers.

The shape of the "pre-emphasized" T1 waveform is controlled by inputs LEN0, LEN1, and LEN2 (TCLKSEL=0). These control inputs allow the user to select the appropriate output pulse shape to meet DSX-1 or CSU templates over a wide variety of cable types and lengths. Those cable types include ABAM, PIC, and PULP.

The CEPT mode is enabled when TCLKSEL=1. Only one output pulse shape is available in the CEPT mode; inputs LEN0, LEN1 and LEN2 can be any state except all zeros.

The line coupling transformer also contributes to the pulse shape seen at the cross-connect point. Transformers for both T1 and CEPT applications must be 1:1.35.

The wave shaping circuitry does not contribute significantly to output jitter (less than 0.01 Upp broadband). Output jitter will be dominated by the jitter on TCLK or LCLK. TCLK and LCLK need only be accurate in frequency, not duty cycle.

LINE DRIVERS

The on-chip differential line drivers interface directly to the output transformer. To optimize device performance, length of the TTIP and TRING traces should be minimized and isolated from neighboring interconnect.

FAULT PROTECTION

The line drivers are fault-protected and will withstand a shorted transformer secondary (or primary) without damage. Inputs MTIP and MRING are normally tied to TTIP and TRING to provide fault monitoring capability. Output LF will transition low if 192 TCLK cycles occur without a one occurring at MTIP or MRING. LF will tri-state on the next one occurrence or two TCLK periods later, whichever is greater.

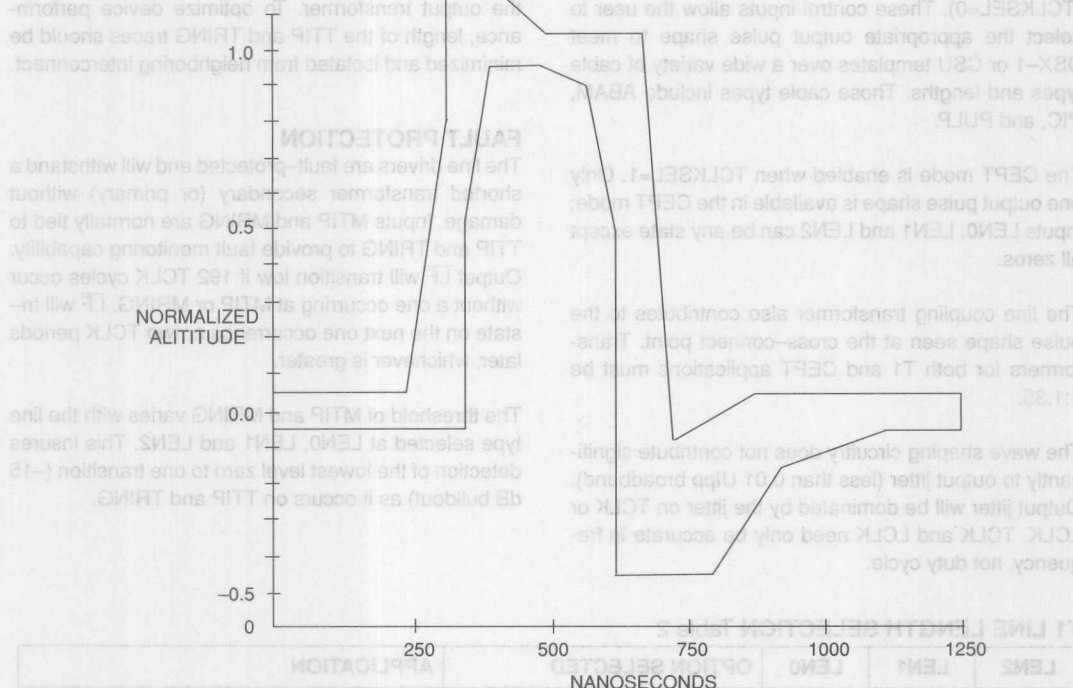
The threshold of MTIP and MRING varies with the line type selected at LEN0, LEN1 and LEN2. This insures detection of the lowest level zero to one transition (–15 dB buildout) as it occurs on TTIP and TRING.

T1 LINE LENGTH SELECTION Table 2

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	0	0	Test mode	Do not use
0	0	1	–7.5 dB buildout	T1 CSU
0	1	0	–15 dB buildout	T1 CSU
0	1	1	0 dB buildout, 0 – 133 feet	T1 CSU, DSX-1 Cross connect
1	0	0	133 – 266 feet	DSX-1 Cross connect
1	0	1	266 – 399 feet	DSX-1 Cross connect
1	1	0	399 – 533 feet	DSX-1 Cross connect
1	1	1	533 – 655 feet	DSX-1 Cross connect

NOTE:

1. The LEN0, LEN1 and LEN2 inputs control T1 output waveshapes when TCLKSEL=0. The G.703 (CEPT) template is selected when TCLKSEL=1 and LEN0, LEN1, and LEN2 are at any state except all zeros.

DSX-1 ISOLATED PULSE TEMPLATE Figure 3**NOTES:**

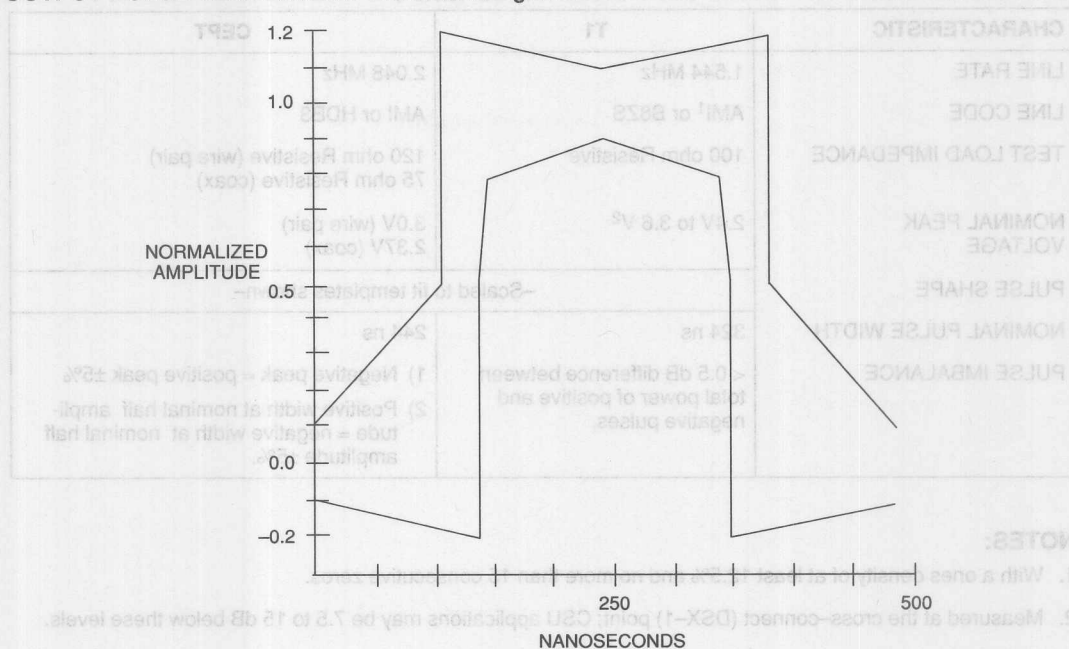
1. Template shown is measured at the cross-connect point.
2. Amplitude shown is normalized; the actual midpoint voltage measured may be between 2.4 and 3.6 volts.
3. The corner points shown below are joined by straight lines to form the template.

MAXIMUM CURVE

(0, 0.05)
 (250, 0.05)
 (325, 0.80)
 (325, 1.15)
 (425, 1.15)
 (500, 1.05)
 (675, 1.05)
 (725, -0.07)
 (875, 0.05)
 (1250, 0.05)

MINIMUM CURVE

(0, -0.05)
 (350, -0.05)
 (350, 0.5)
 (400, 0.95)
 (500, 0.95)
 (600, 0.9)
 (650, 0.5)
 (650, -0.45)
 (800, -0.45)
 (925, -0.2)
 (1100, -0.05)
 (1250, -0.05)

OUTPUT PULSE TEMPLATE AT 2.048 MHz Figure 4**NOTES:**

1. Unlike the DSX-1 template, which is specified at the cross-connect point, the CEPT (2.048 MHz) template is specified at the transmit line output.
2. The template shown above is normalized. The actual pulse height is cable dependent and is specified in Table 3.
3. The corner points shown below are joined by straight lines to form the template.

MAXIMUM CURVE

(0, 0.1)
 (109.5, 0.5)
 (109.5, 1.2)
 (244, 1.1)
 (378.5, 1.2)
 (378.5, 0.5)
 (488, 0.1)

MINIMUM CURVE

(0, -0.1)
 (134.5, -0.2)
 (134.5, 0.5)
 (147, 0.8)
 (244, 0.9)
 (341, 0.8)
 (353.5, 0.5)
 (353.5, -0.2)
 (488, -0.1)

CHARACTERISTICS OF T1 AND CEPT INTERFACES Table 3

CHARACTERISTIC	T1	CEPT
LINE RATE	1.544 MHz	2.048 MHz
LINE CODE	AMI ¹ or B8ZS	AMI or HDB3
TEST LOAD IMPEDANCE	100 ohm Resistive	120 ohm Resistive (wire pair) 75 ohm Resistive (coax)
NOMINAL PEAK VOLTAGE	2.4V to 3.6 V ²	3.0V (wire pair) 2.37V (coax)
PULSE SHAPE	—Scaled to fit templates shown—	
NOMINAL PULSE WIDTH	324 ns	244 ns
PULSE IMBALANCE	< 0.5 dB difference between total power of positive and negative pulses.	1) Negative peak = positive peak $\pm 5\%$ 2) Positive width at nominal half amplitude = negative width at nominal half amplitude $\pm 5\%$.

NOTES:

1. With a ones density of at least 12.5% and no more than 15 consecutive zeros.
2. Measured at the cross-connect (DSX-1) point; CSU applications may be 7.5 to 15 dB below these levels.

NOTES:

1. Unlike the DSX-1 template, which is specified at the cross-connect point, the CEPT (2.048 MHz) template is specified at the transmit line output.

2. The template shown above is normalized. The actual pulse height is cable dependent and is specified in Table 3.

3. The corner points shown below are joined by straight lines to form the template.

MINIMUM CURVE	MAXIMUM CURVE
(0, -0.1)	(0, 0)
(134.5, -0.5)	(108.5, 0.5)
(184.5, 0.5)	(108.5, 1.5)
(147, 0.8)	(544, 1.1)
(244, 0.8)	(378.5, 1.5)
(341, 0.5)	(378.5, 0.5)
(323.5, 0.5)	(488, 0.1)
(383.5, -0.5)	
(488, -0.1)	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground
 Operating Temperature
 Storage Temperature
 Soldering Temperature

1.0V to +7V
 0°C to 70°C
 -55°C to +125°C
 260°C for 10°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+3$	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{DD}	4.75		5.25	V	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		50		mA	2,3
Supply Current	I_{DD}		35		mA	2,4
Supply Current	I_{DD}		20		mA	2,5
Input Leakage	I_{IL}	-1.0		+1.0	μA	6
Output Current @ 0.4V	I_{OL}	+4.0			mA	7

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All inputs except MTIP and MRING.
2. $V_{DD}=5.25V$; TCLK = LCLK = 1.544 MHz; output line transformer and load as shown in Figure 2.
3. TAIS = 1
4. 50% ones density.
5. All zeros at data inputs.
6. $0.0V < V_{IN} < 5.0V$.
7. Output LF (open collector).

AC ELECTRICAL CHARACTERISTICS

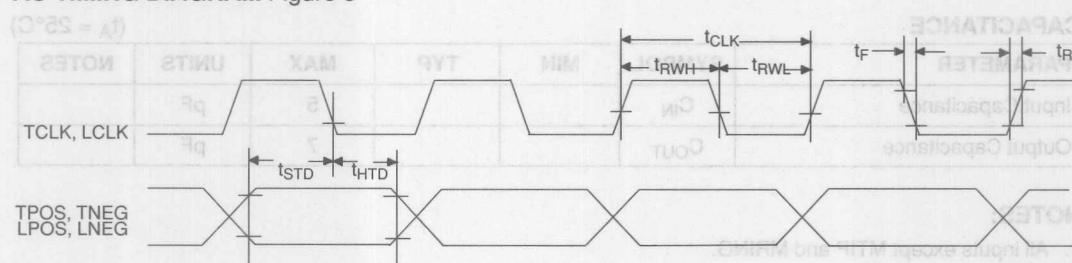
(0°C to 70°C; $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK, LCLK Period	t_{CLK}		648		ns	1
TCLK, LCLK Period	t_{CLK}		488		ns	2
TCLK, LCLK Pulse Width	t_{RWH}, t_{RWL}	70	324		ns	1
TCLK, LCLK Pulse Width	t_{RWH}, t_{RWL}	70	244		ns	2
TCLK, LCLK Rise and Fall Times	t_R, t_F			20	ns	
TPOS, TNEG Setup to TCLK Falling	t_{STD}	50			ns	
LPOS, LNEG Setup to LCLK Falling	t_{STD}	50			ns	
TPOS, TNEG Hold from TCLK Falling	t_{HTD}	50			ns	
LPOS, LNEG Hold from LCLK Falling	t_{HTD}	50			ns	

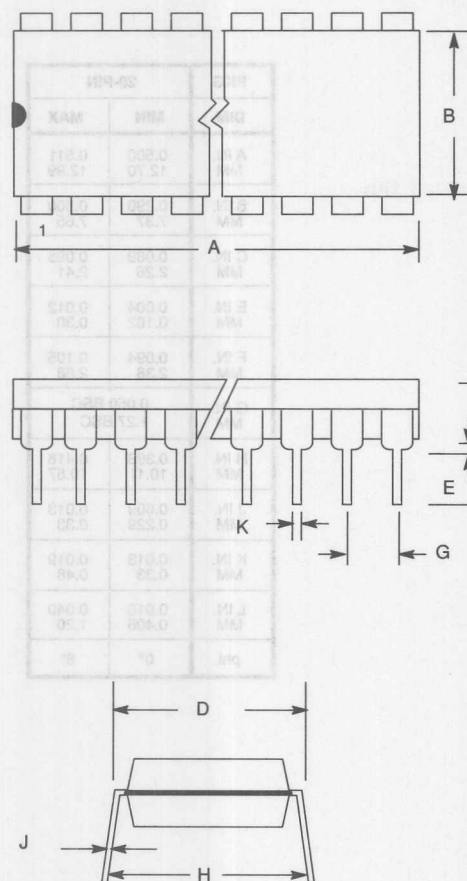
NOTES:

1. T1 applications.
2. CEPT applications.

AC TIMING DIAGRAM Figure 5

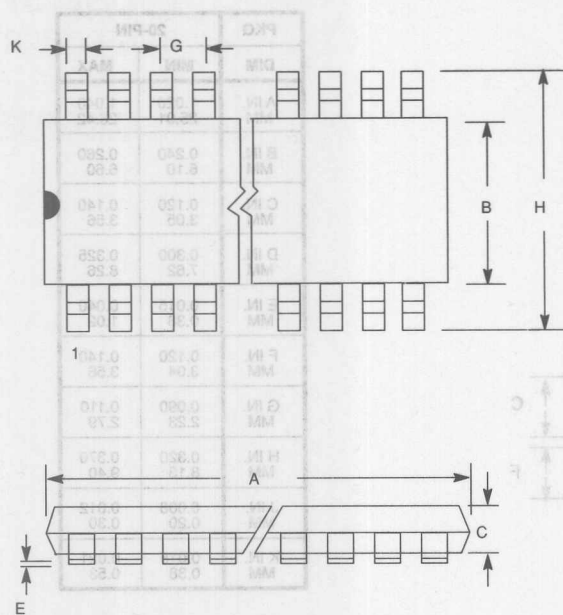


DS2186 TRANSMIT LINE INTERFACE 20-PIN DIP

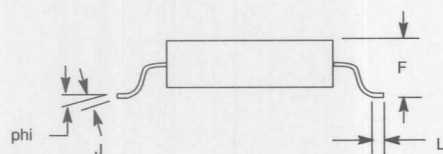


PKG	20-PIN	
	DIM	
	MIN	MAX
A IN.	1.020	1.040
MM	25.91	26.42
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.23	2.79
H IN.	0.320	0.370
MM	8.13	9.40
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS2186 TRANSMIT LINE INTERFACE 20-PIN SOIC



PKG	20-PIN	
DIM	MIN	MAX
A IN. MM	0.500 12.70	0.511 12.99
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.406	0.040 1.20
phi	0°	8°



DALLAS

SEMICONDUCTOR

DS2187

Receive Line Interface

FEATURES

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801, TR 62411, and applicable CCITT G.823
- Precision on-chip PLL eliminates external crystal or LC tank - no tuning required
- Decodes AMI, B8ZS, and HDB3 coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180A T1/ISDN Primary Rate and DS2181A CEPT Transceivers, as well as DS2141A T1 and DS2143 E1 Controllers
- Companion to the DS2186 T1/CEPT Transmit Line Interface and DS2188 T1/CEPT Jitter Attenuator
- Single 5V supply; low-power CMOS technology

DESCRIPTION

The DS2187 T1/CEPT Receive Line Interface Chip interfaces user equipment to North American (T1 1.544 MHz) and European (CEPT 2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and eliminates expensive discrete components and/or

PIN ASSIGNMENT

AVDD	1	20	DVDD
RAIS	2	19	RCL
ZCSEN	3	18	AIS
NC	4	17	BPV
LCAP	5	16	NC
RCLKSEL	6	15	NC
RTIP	7	14	RPOS
RRING	8	13	RNEG
LOCK	9	12	RCLK
AVSS	10	11	DVSS

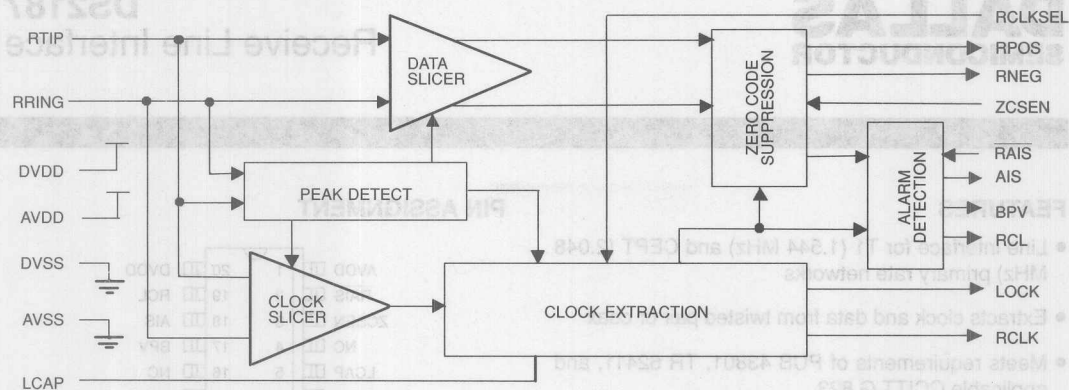
20-Pin SOIC (300 Mil)

AVDD	1	18	DVDD
RAIS	2	17	RCL
ZCSEN	3	16	AIS
LCAP	4	15	BPV
RCLKSEL	5	14	NC
RTIP	6	13	RPOS
RRING	7	12	RNEG
LOCK	8	11	RCLK
AVSS	9	10	DVSS

18-Pin DIP (300 Mil)

manual tuning required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI.

DS2187 BLOCK DIAGRAM Figure 1

LINE INPUT

Input signals are coupled to the DS2187 via a 1:2 center-tapped transformer as shown in Figure 2. For T1 applications, R1 and R2 must be 200 ohms in order to properly terminate the line at 100 ohms. R1 and R2 are set at 150 or 240 ohms for CEPT applications. Special internal circuitry of the RTIP and RRING inputs permits negative signal excursions below V_{SS} , which will occur in the circuit in Figure 2.

PEAK DETECTOR AND SLICERS

Signal pulses present at RTIP and RRING are sampled by an internal peak detect circuit. The clock and data slicer threshold are set for 50% of the sampled peak voltage.

Peak input levels at RRIP and RRING must exceed 0.6 volts to establish minimum slicer thresholds. Signals below this level will cause RCL to transition high after 192 bit times.

CLOCK EXTRACTION

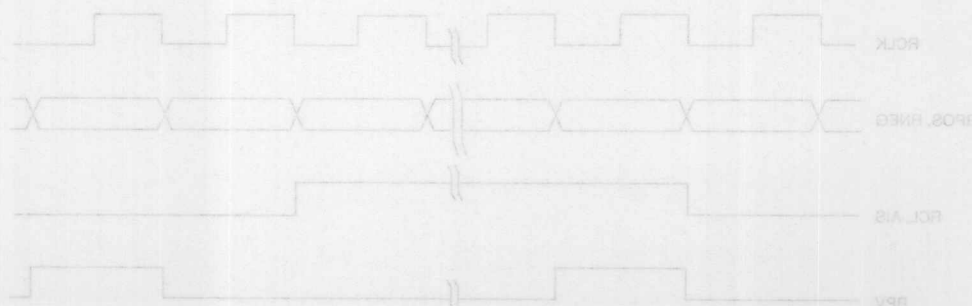
The DS2187 utilizes both frequency locked (FLL) and digital phase locked (DPLL) loops to recover data and

clock from the incoming AMI signal. T1 applications utilize a 18.528 MHz clock divided by either 11, 12, or 13 to match the phase of the incoming jittered line signal. This technique affords exceptional jitter tracking which enables the DS2187 to meet the latest AT&T TR 62411 and ECSA jitter specifications. A 24.576 MHz clock divided by 11, 12, or 13 provides jitter tracking in the CEPT mode. The DPLL output is buffered and presented at RCLK. An on-chip, laser-trimmed voltage controlled oscillator (V_{CO}) provides the precision 18.528 MHz and 24.576 MHz frequency sources utilized in the FLL. The FLL is a high-Q circuit which tracks the average frequency of the incoming signal, minimizing the effect of the DPLL on output jitter.

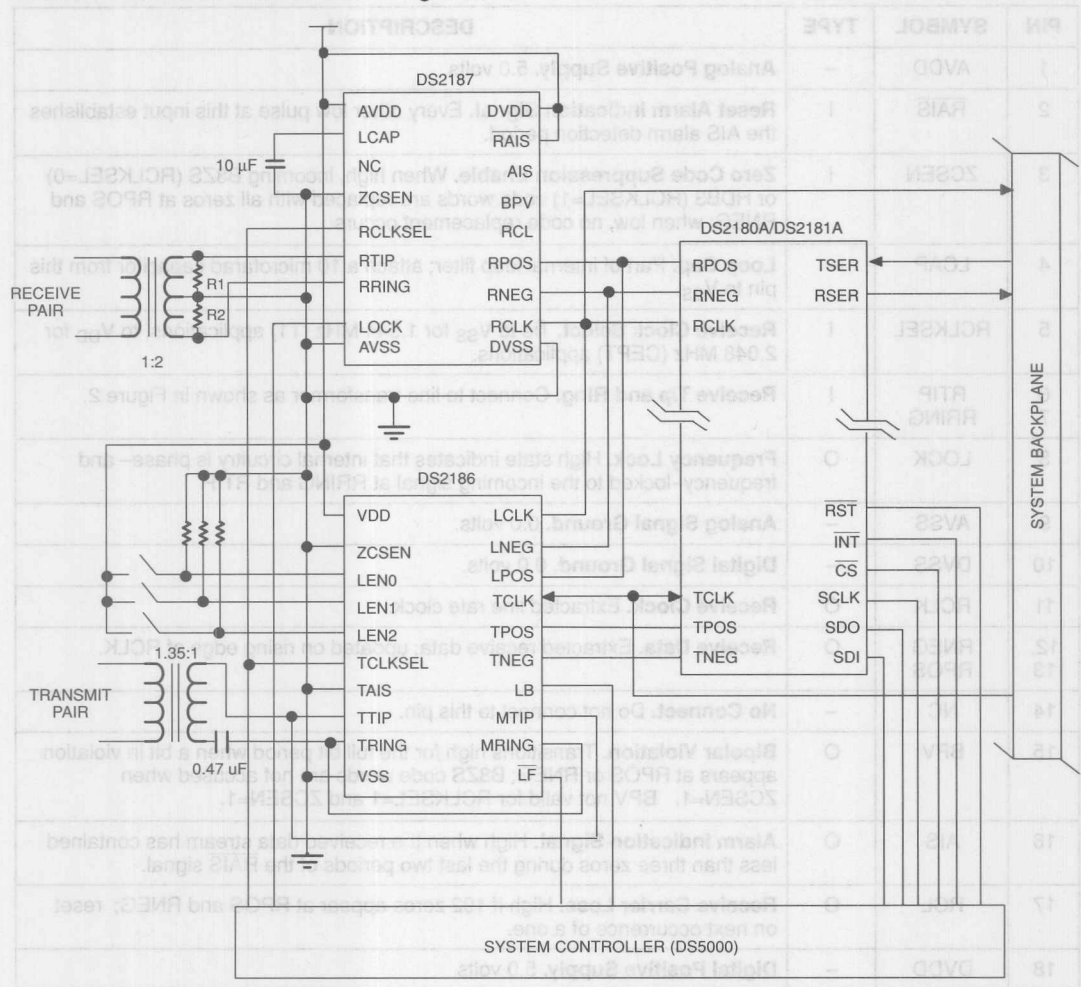
During the acquisition time or if RCL goes high, the LOCK pin will go low to indicate a loss of synchronization to the line signal. Once this pin goes high, the FLL has achieved frequency lock and valid data is present at the RPOS and RNEG outputs.

PIN DESCRIPTION Table 1

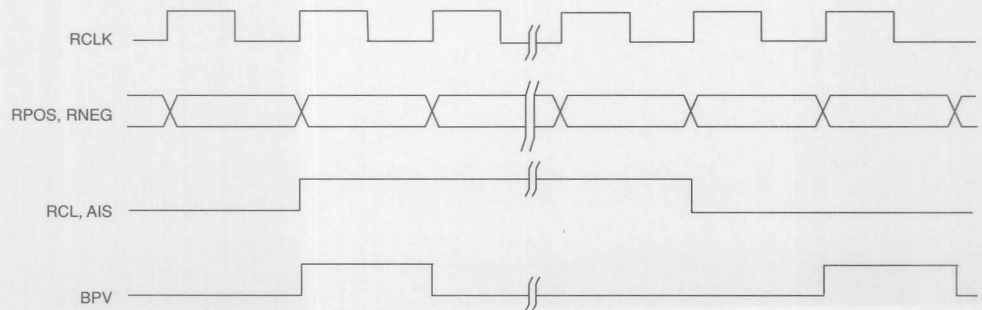
PIN	SYMBOL	TYPE	DESCRIPTION
1	AVDD	—	Analog Positive Supply. 5.0 volts.
2	RAIS	I	Reset Alarm Indication Signal. Every other low pulse at this input establishes the AIS alarm detection period.
3	ZCSEN	I	Zero Code Suppression Enable. When high, incoming B8ZS (RCLKSEL=0) or HDB3 (RCLKSEL=1) code words are replaced with all zeros at RPOS and RNEG; when low, no code replacement occurs.
4	LCAP	—	Loop Cap. Part of internal loop filter; attach a 10 microfarad capacitor from this pin to V _{SS} .
5	RCLKSEL	I	Receive Clock Select. Tie to V _{SS} for 1.544 MHz (T1) applications, to V _{DD} for 2.048 MHz (CEPT) applications.
6 7	RTIP RRING	I	Receive Tip and Ring. Connect to line transformer as shown in Figure 2.
8	LOCK	O	Frequency Lock. High state indicates that internal circuitry is phase- and frequency-locked to the incoming signal at RRING and RTIP.
9	AVSS	—	Analog Signal Ground. 0.0 volts.
10	DVSS	—	Digital Signal Ground. 0.0 volts.
11	RCLK	O	Receive Clock. Extracted line rate clock.
12, 13	RNEG RPOS	O	Receive Data. Extracted receive data; updated on rising edge of RCLK.
14	NC	—	No Connect. Do not connect to this pin.
15	BPV	O	Bipolar Violation. Transitions high for the full bit period when a bit in violation appears at RPOS or RNEG; B8ZS code words are not accused when ZCSEN=1. BPV not valid for RCLKSEL=1 and ZCSEN=1.
16	AIS	O	Alarm Indication Signal. High when the received data stream has contained less than three zeros during the last two periods of the RAIS signal.
17	RCL	O	Receive Carrier Loss. High if 192 zeros appear at RPOS and RNEG; reset on next occurrence of a one.
18	DVDD	—	Digital Positive Supply. 5.0 volts



SYSTEM LEVEL INTERCONNECT Figure 2



OUTPUT TIMING Figure 3



ZERO CODE SUPPRESSION

The device will decode incoming B8ZS (RCLKSEL=0) or HDB3 (RCLKSEL=1) code words and replace them with an all zero code when ZCSEN=1. When ZCSEN=0, code words will pass through the device without being altered. This feature can be disabled when the DS2187 is used with transceiver devices such as the DS2180A, DS2181A, DS2141A, or DS2143.

ALARM DETECTION

The extracted data is monitored for network alarm and error conditions. RCL is set when 192 consecutive zeros occur; it is cleared on the next one occurrence. AIS is set when less than three zeros have appeared at RPOS and RNEG during the last two periods of the RAIS signal; once set, AIS will remain high for the next two periods of RAIS. AIS will return low when more than two zeros appear. BPV reports bipolar violations as

they occur at RPOS and RNEG; B8ZS code words will not be flagged by BPV when ZCSEN=1.

BYPASSING AND LAYOUT CONSIDERATIONS

The DS2187 contains both precision analog and high-speed digital circuitry on the same chip. The power supplies of these circuits (AVDD, AVSS, DVDD and DVSS) should be connected to system analog and digital supplies. If separate system supplies do not exist, the appropriate supply pins can be tied together. Tying the analog and digital supplies together on the DS2187 will not degrade its performance, provided the power supply is sufficiently decoupled.

To assure optimum performance, the length of LCAP, RTIP and RRING printed circuit board traces should be minimized and isolated from neighboring interconnect.

	V	12.0		-7.0	V _{IN}	Input Voltage Swing RTIP, RRING
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DC ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I _{DD}		18	25	mA	2
Input Leakage	I _I	-1.0		+1.0	μA	1,3
Output Current @ 2.4V	I _{OH}	-1.0			mA	4
Output Current @ 0.4V	I _{OL}	+4.0			mA	4

- NOTES:
- 1. All inputs except RTIP and RRING.
 - 2. Outputs open.
 - 3. 0.0V < V_{IN} < V_{DD}.
 - 4. All outputs.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground**	-1.0V to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**Inputs other than RTIP and RRING.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V _{IH}	2.0		V _{DD} +3	V	1
Logic 0	V _{IL}	-0.3		+0.8	V	1
Supply	V _{DD}	4.75		5.25	V	
Input Voltage Swing RTIP, RRING	V _{IN}	-7.0		12.0	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I _{DD}		18	25	mA	2
Input Leakage	I _{IL}	-1.0		+10	μA	1,3
Output Current @ 2.4V	I _{OH}	-1.0			mA	4
Output Current @ 0.4V	I _{OL}	+4.0			mA	4

NOTES:

1. All inputs except RTIP and RRING.
2. Outputs open.
3. 0.0V < V_{IN} < V_{DD}.
4. All outputs.

ANALOG ELECTRICAL CHARACTERISTICS(0°C to 70°C, $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Acquisition	t_{LOCK}		50		ms	1
RTIP, RRING Minimum Sensitivity	V_{THRES}		.4	.6	V_{pk}	2
FLL Loop Bandwidth	f_{BW}		50		Hz	3
Capture Range	f_{CAP}		± 6		%	4
Input Jitter Tolerance	J_{IN}	200			UI	5

NOTES:

1. Time from reappearance of a valid signal at RPOS and RNEG to a LOCK=1.
2. Minimum peak voltage necessary for proper processing of signal.
3. Loop bandwidth when in lock (LOCK=1).
4. When out-of-lock (LOCK=0); measured as a percent of incoming clock frequency.
5. Maximum input jitter in unit intervals at 10 Hz.

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

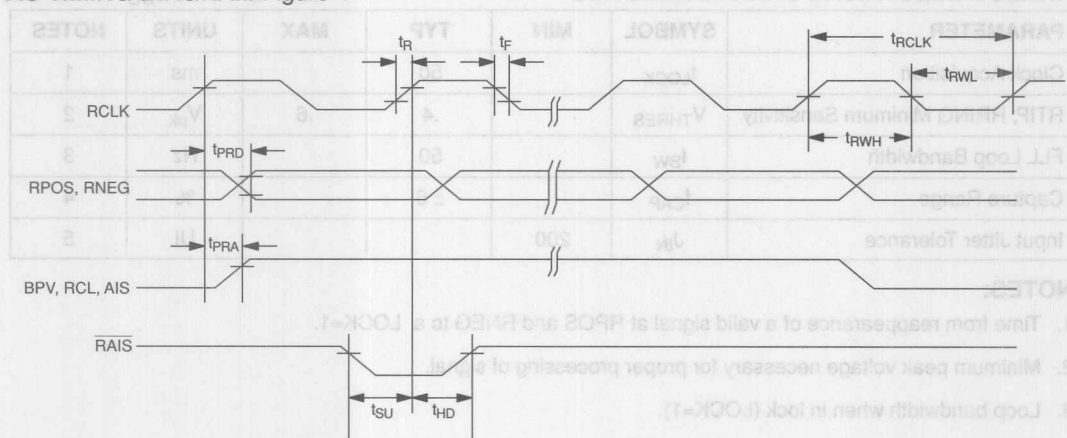
AC ELECTRICAL CHARACTERISTICS(0° to 70°C, $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	594	648	702	ns	1,3
RCLK Period	t_{RCLK}	445	488	530	ns	2,3
RCLK Pulse Width	t_{RWH}, t_{RWL}		324		ns	1
RCLK Pulse Width	t_{RWH}, t_{RWL}		244		ns	2
RCLK Rise and Fall Time	t_R, t_F			20	ns	
Propagation Delay RCLK to RPOS, RNEG	t_{PRD}			75	ns	
Propagation Delay RCLK to BPV, RCL, AIS	t_{PRA}			75	ns	
RAIS Setup	t_{SU}, t_{HD}	50			ns	

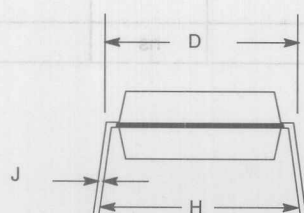
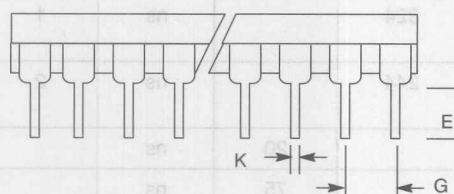
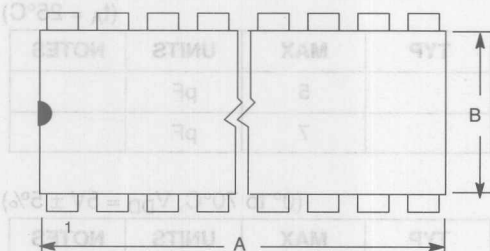
NOTES:

1. T1 applications (RCLKSEL=0).
2. CEPT applications (RCLKSEL=1).
3. Minimum and maximum limits shown reflect changes in DPLL divide ratio as required to track jitter.

AC TIMING DIAGRAM Figure 4

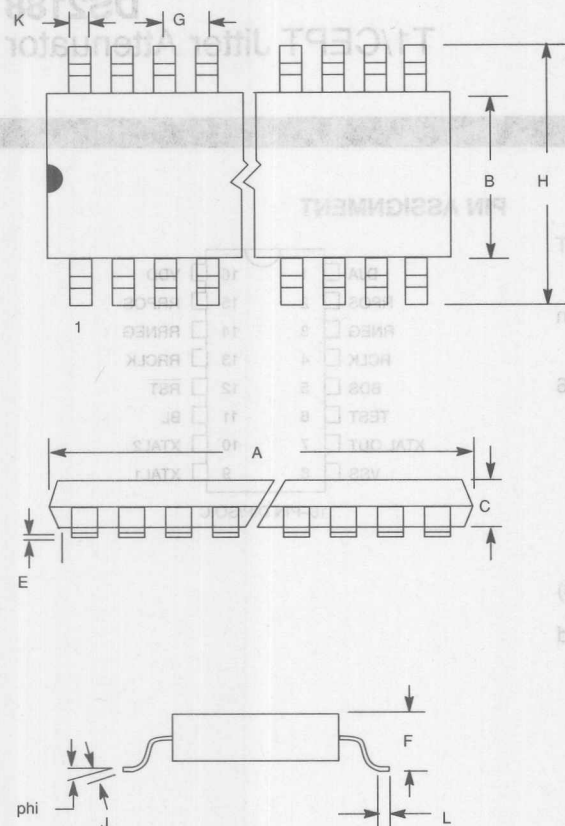


DS2187 RECEIVE LINE INTERFACE 18-PIN DIP



PKG	18-PIN	
DIM	MIN	MAX
A IN. MM	0.890	0.920
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.23	0.110 2.79
H IN. MM	0.320 8.13	0.370 9.40
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS2187S RECEIVE LINE INTERFACE 20-PIN SOIC



PKG	20-PIN	
DIM	MIN	MAX
A IN. MM	0.500 12.70	0.511 12.99
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.406	0.040 1.20
phi	0°	8°

DALLAS

SEMICONDUCTOR

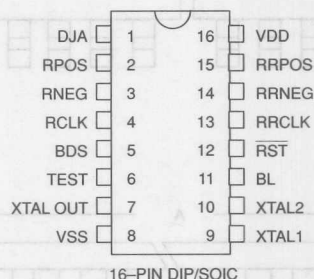
DS2188

T1/CEPT Jitter Attenuator

FEATURES

- Attenuates clock and data jitter present in T1 or CEPT lines
- Meets the jitter attenuation templates outlined in TR62411, TR-TSY-000170, G.735, and G.742
- Only one external component required; either a 6.176 MHz (T1) or 8.192 MHz (CEPT) crystal
- Selectable buffer size of 128 or 32 bits
- Jitter attenuation is easily disabled
- Single +5V supply; low-power CMOS technology
- Available in 16-pin DIP and 16-pin SOIC (DS2188S)
- Companion to the DS2186 Transmit Line and DS2187 Receive Line Interfaces

PIN ASSIGNMENT



DESCRIPTION

The DS2188 T1/CEPT Jitter Attenuator Chip contains a 128 X 2-bit buffer which, in conjunction with an external 4X crystal, is used to attenuate the incoming jitter present in clock and data. The device meets all of the latest applicable specifications including those outlined in TR 62411 (Accunet* T1.5 Service Description and Interface Specifications, December 1990), TR-TSY-000170 (Digital Cross-Connect System Requirements and Ob-

jectives, November 1985), and the CCITT Recommendations G.735 and G.742. The DS2188 is compatible with the DS2180A T1/ISDN Primary Rate Transceiver and DS2181A CEPT Transceiver and it is the companion to the DS2187 T1/CEPT Receive Line Interface and DS2186 T1/CEPT Transmit Line Interface. It can also be used in conjunction with the DS2190 T1 Network Interface Unit.

* Service mark of AT&T Communications

OVERVIEW

The RCLK input is fed to a 128 x 2 bit FIFO where it drives the write pointer for the positive (RPOS) and negative (RNEG) data. The read pointer of the FIFO and RRCLK is generated by dividing the frequency of the crystal connected to XTAL1 and XTAL2 by four. The frequency of the crystal is adjusted by a DPLL to the long-term average frequency of RCLK. As long as the jitter present at RCLK is less than 120 unit intervals peak-to-peak (UIpp), then the FIFO buffer will be able to absorb the incoming jitter and it will be attenuated in accordance with TR 62411 (December 1990). In this situation, the BL (Buffer Limit) pin will remain low. Figures 1 and 2 illustrate the DS2188 Jitter Attenuator performance.

If the incoming jitter has excursions greater than 120 UIpp, then the crystal is adjusted to track the short-term frequency variations of the incoming signal so that there is no loss of data. This adjustment is accomplished by dividing the 4X crystal by either 3 1/2 or 4 1/2 instead of 4. When the incoming jitter is greater than 120 UIpp, the BL pin will transition high. When the incoming jitter returns to less than 120 UIpp, the BL pin will return low.

The jitter attenuator in the DS2188 can be disabled by tying the DJA pin high. When the jitter attenuator is disabled, the FIFO is bypassed and jitter received at RCLK, RPOS and RNEG is passed through the DS2188 to RRCLK, RRPOS, and RRNEG. In this situation, the BL pin has no significance and XTAL OUT will not be coherent with RRCLK.

How to use the DS2188 with Dallas Semiconductor's other T1 and CEPT line interface parts is illustrated in

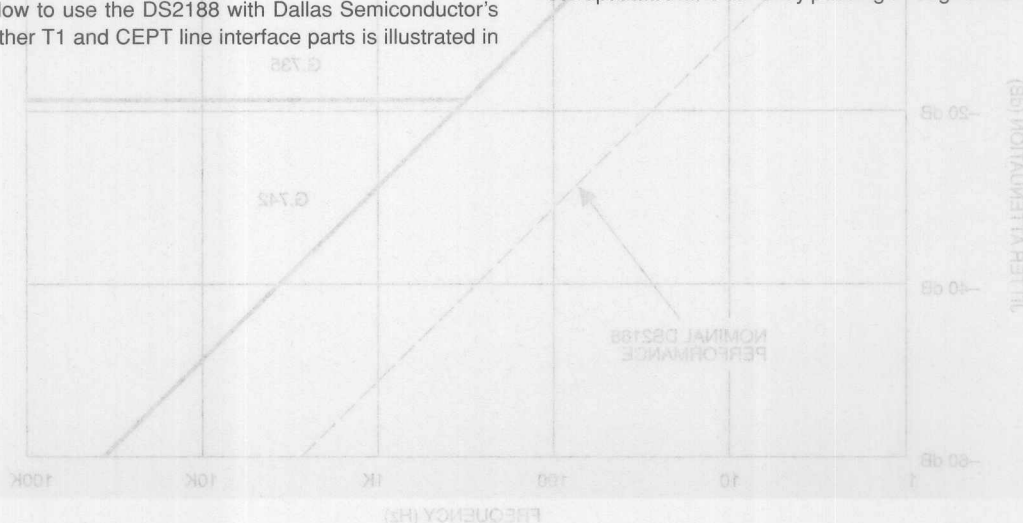
Figures 3 through 5. Figure 3 illustrates how to use the DS2188 in the receive path along with a DS2187 Receive Line Interface. Figure 4 illustrates how to use the DS2188 in the transmit path with the DS2186 Transmit Line Interface. Also, see DS2188 Application Note, "Operation at Speeds Greater than E1" for additional information.

BUFFER DEPTH SELECT

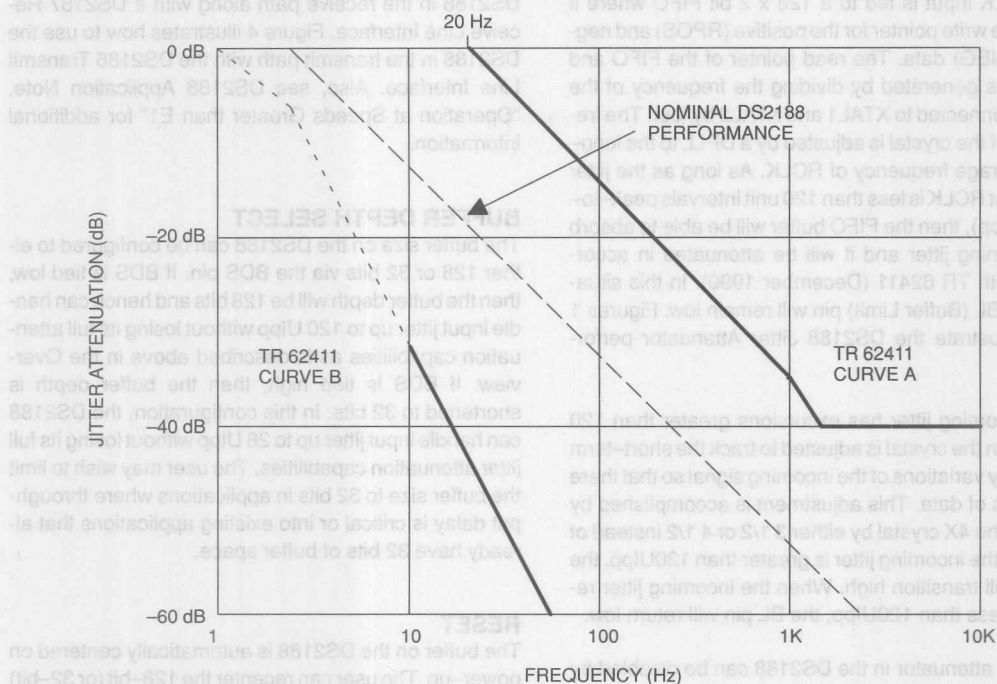
The buffer size on the DS2188 can be configured to either 128 or 32 bits via the BDS pin. If BDS is tied low, then the buffer depth will be 128 bits and hence can handle input jitter up to 120 UIpp without losing its full attenuation capabilities as is described above in the Overview. If BDS is tied high, then the buffer depth is shortened to 32 bits. In this configuration, the DS2188 can handle input jitter up to 28 UIpp without losing its full jitter attenuation capabilities. The user may wish to limit the buffer size to 32 bits in applications where throughput delay is critical or into existing applications that already have 32 bits of buffer space.

RESET

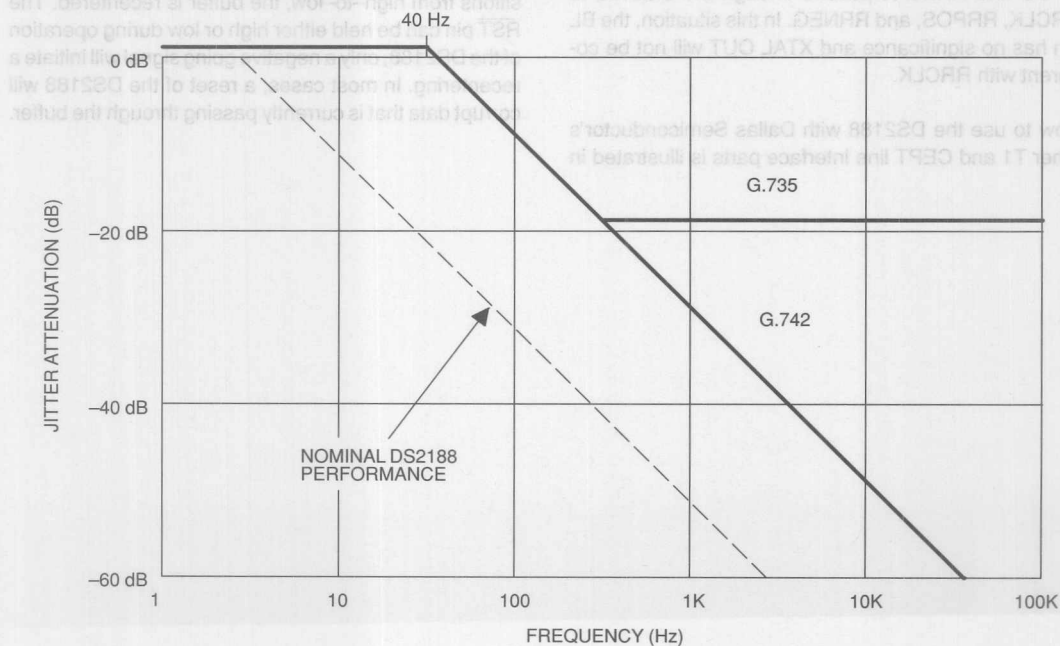
The buffer on the DS2188 is automatically centered on power-up. The user can recenter the 128-bit (or 32-bit) buffer on demand via the RST pin. The RST pin on the DS2188 is negative-edge triggered. When this pin transitions from high-to-low, the buffer is recentered. The RST pin can be held either high or low during operation of the DS2188; only a negative going signal will initiate a recentering. In most cases, a reset of the DS2188 will corrupt data that is currently passing through the buffer.



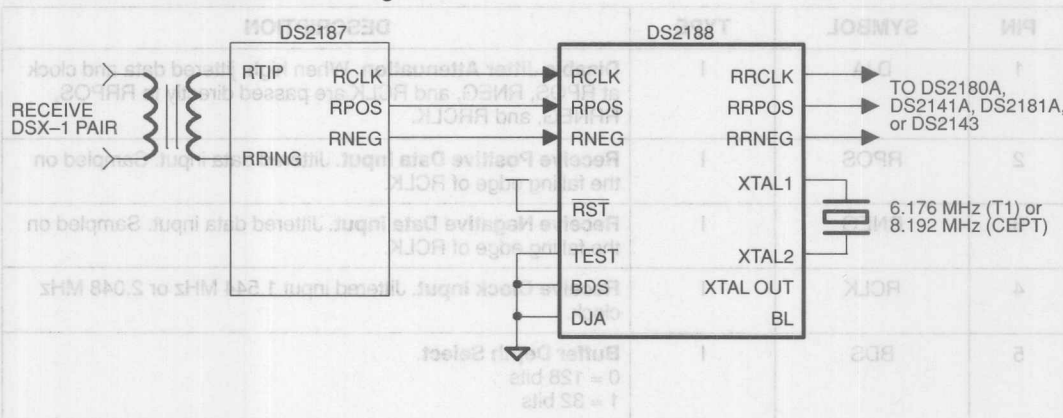
DS2188 T1 JITTER ATTENUATION PERFORMANCE Figure 1



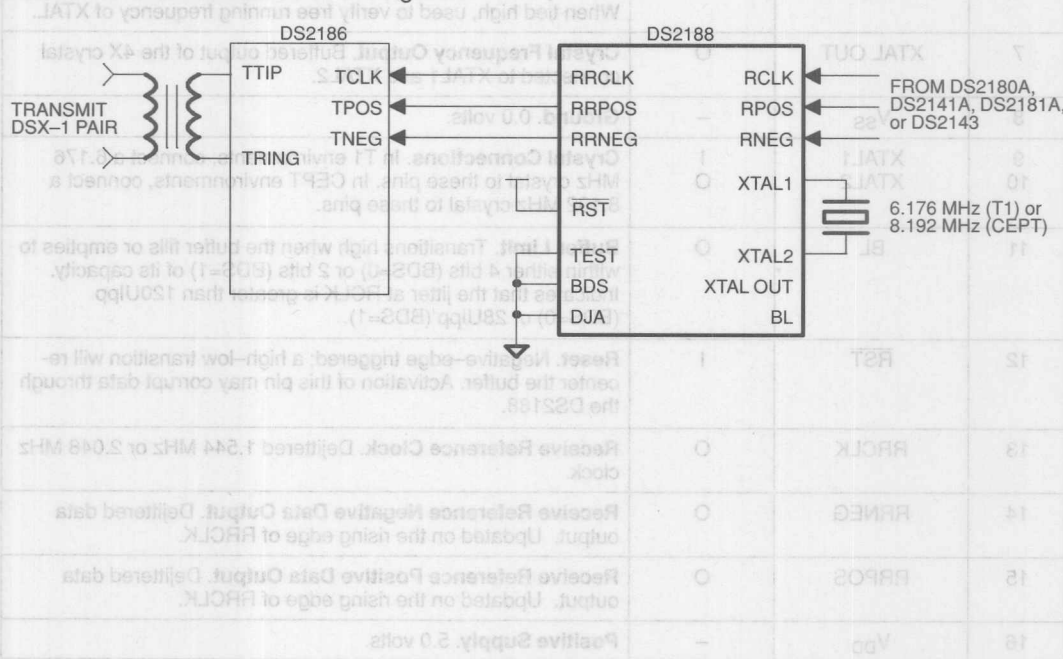
DS2188 CEPT JITTER ATTENUATION PERFORMANCE Figure 2



DS2188 IN THE RECEIVE PATH Figure 3



DS2188 IN THE TRANSMIT PATH Figure 4



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	DJA	I	Disable Jitter Attenuation. When high, jittered data and clock at RPOS, RNEG, and RCLK are passed directly to RRPOS, RRNEG, and RRCLK.
2	RPOS	I	Receive Positive Data Input. Jittered data input. Sampled on the falling edge of RCLK.
3	RNEG	I	Receive Negative Data Input. Jittered data input. Sampled on the falling edge of RCLK.
4	RCLK	I	Receive Clock Input. Jittered input 1.544 MHz or 2.048 MHz clock.
5	BDS	I	Buffer Depth Select. 0 = 128 bits 1 = 32 bits
6	TEST	I	Test Input. In normal applications, this pin should be tied low. When tied high, used to verify free running frequency of XTAL.
7	XTAL OUT	O	Crystal Frequency Output. Buffered output of the 4X crystal connected to XTAL1 and XTAL2.
8	V _{SS}	—	Ground. 0.0 volts.
9 10	XTAL1 XTAL2	I O	Crystal Connections. In T1 environments, connect a 6.176 MHz crystal to these pins. In CEPT environments, connect a 8.192 MHz crystal to these pins.
11	BL	O	
12	RST	I	Reset. Negative-edge triggered; a high-low transition will re-center the buffer. Activation of this pin may corrupt data through the DS2188.
13	RRCLK	O	Receive Reference Clock. Dejittered 1.544 MHz or 2.048 MHz clock.
14	RRNEG	O	Receive Reference Negative Data Output. Dejittered data output. Updated on the rising edge of RRCLK.
15	RRPOS	O	Receive Reference Positive Data Output. Dejittered data output. Updated on the rising edge of RRCLK.
16	V _{DD}	—	Positive Supply. 5.0 volts.

quency of this crystal should be 6.176 MHz. For CEPT environments, the frequency of this crystal should be

nominal speeds greater than 2.1 for additional information.

CRYSTAL MANUFACTURERS Table 2

MANUFACTURER	PART #	FREQUENCY
JAN Crystal	6323-00, JC6A14 6323-00, JC8A14	6.176 MHz 8.192 MHz
M-TRON	MP-1 6.176, SRMP-1 6.176, 4575-001 MP-1 8.192, SRMP-1 8.192, 4575-002	6.176 MHz 8.192 MHz

CRYSTAL SELECTION GUIDELINES FOR THE DS2188

PARAMETER	SPECIFICATION
Parallel resonant frequency	6.176 MHz (T1) or 8.192 MHz (CEPT)
Mode	Fundamental
Load capacitance	14 to 20 pF (16 pF preferred)
Tolerance	±50 ppm over 0 to 70°C
Pullability	CL = 10 pF, $\Delta f = +175$ to +250 ppm CL = 45 pF, $\Delta f = -175$ to -250 ppm
Effective series resistance	40 ohms maximum for 6.176 MHz 30 ohms maximum for 8.192 MHz
Crystal cut	AT

NOTES:

1. $R_{CLK} = 1.544 \text{ M}\Omega$; $V_{DD} = 2.50$; outputs open.
2. $V_{SS} < V_{IN} < V_{DD}$; $X_{TAL1} = X_{TAL2} = V_{DD}$.
3. Does not apply to XTAL1 or XTAL2.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground
Operating Temperature
Storage Temperature
Soldering Temperature

-1.0V to +7.0V
0°C to 70°C
-55°C to +125°C
260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic1	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{DD}	4.50		5.50	V	

NOTE:

- Does not apply to XTAL1.

CAPACITANCE

($t_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output	C_{OUT}		10		pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		7	12	mA	1
Input Leakage	I_L	-1.0		+1.0	μA	2,3
Output Current (2.4V)	I_{OH}	-1.0			mA	3
Output Current (0.4V)	I_{OL}	+4.0			mA	3

NOTES:

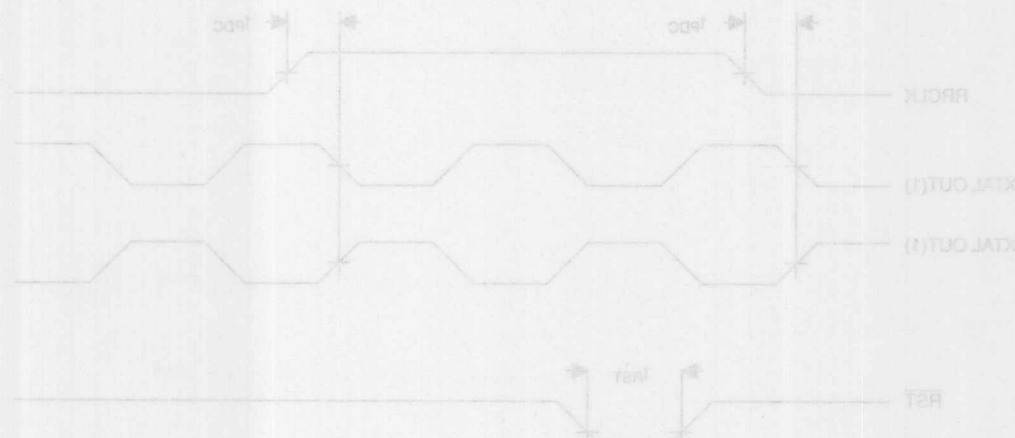
- $RCLK = 1.544 \text{ MHz}$; $V_{DD} = 5.50$; outputs open.
- $V_{SS} < V_{IN} < V_{DD}$; $XTAL1 = XTAL2 = V_{DD}$.
- Does not apply to XTAL1 or XTAL2.

AC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_p	-200		+200	ppm	1
RCLK Pulse Width	t_{WH}, t_{WL}	100			ns	
RCLK Rise and Fall Times	t_R, t_F			50	ns	
RPOS, RNEG Setup to RCLK	t_{SD}	50			ns	
RPOS, RNEG Hold from RCLK	t_{HD}	50			ns	
Propagation Delay from RRCLK to RRPOS, RRNEG Valid	t_{PD}			50	ns	
Propagation Delay from XTAL OUT to RRCLK	t_{PDC}			50	ns	2
\overline{RST} Pulse Width	t_{RST}	1			μs	

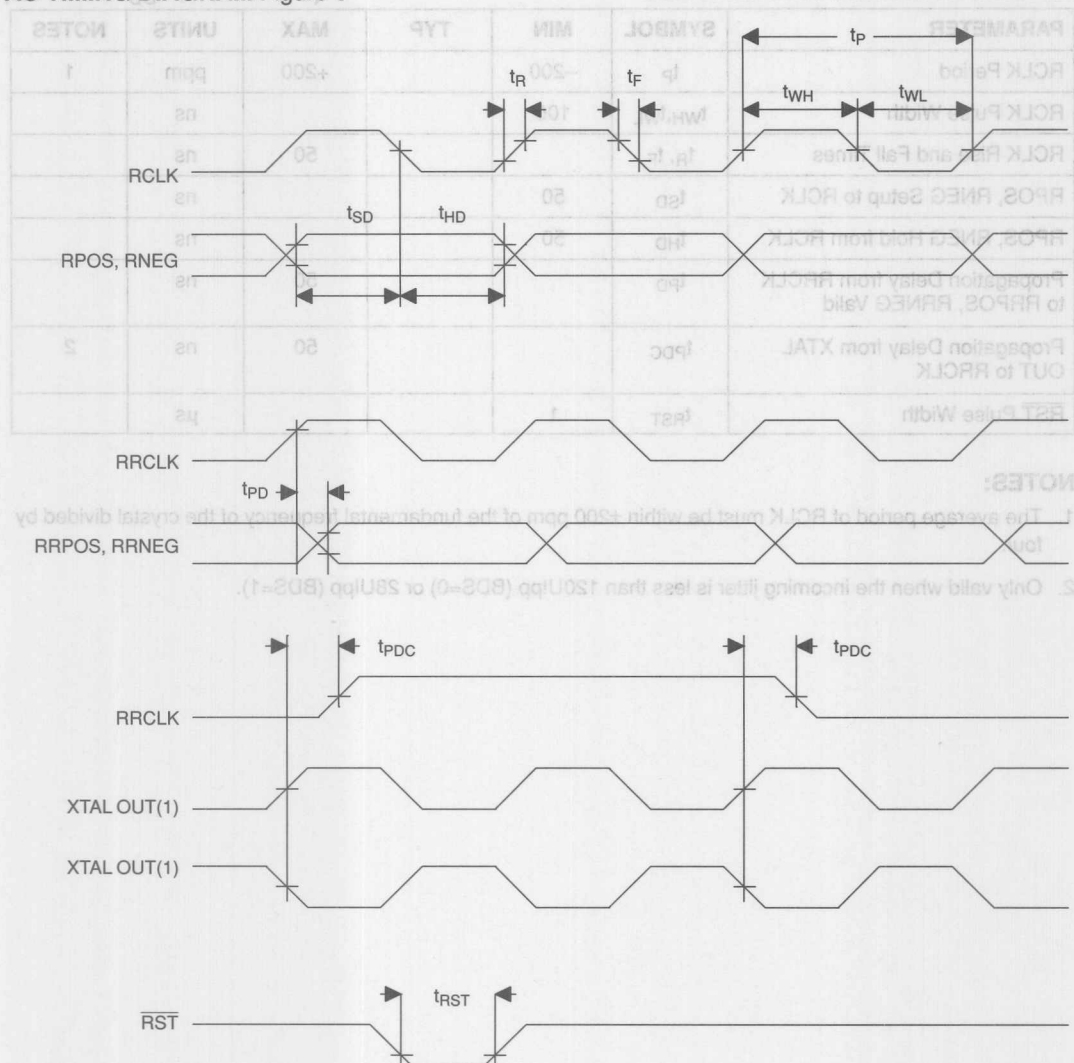
NOTES:

1. The average period of RCLK must be within ± 200 ppm of the fundamental frequency of the crystal divided by four.
2. Only valid when the incoming jitter is less than 120UIpp (BDS=0) or 28UIpp (BDS=1).

**NOTE:**

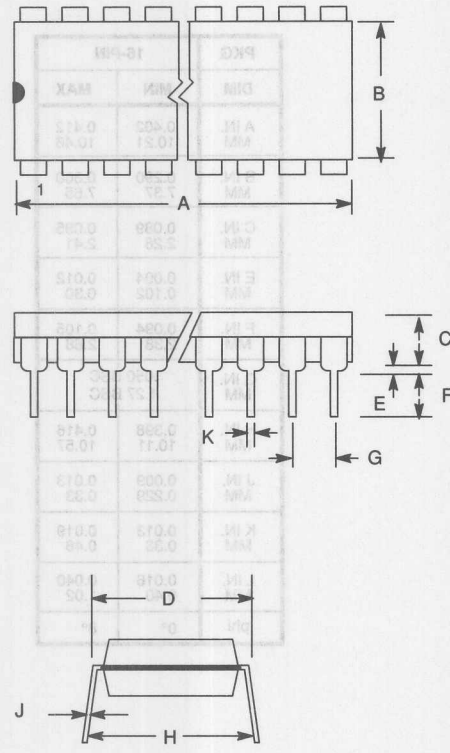
1. The phase relationship between XTAL OUT and RCLK can be either form.

AC TIMING DIAGRAM Figure 5

**NOTE:**

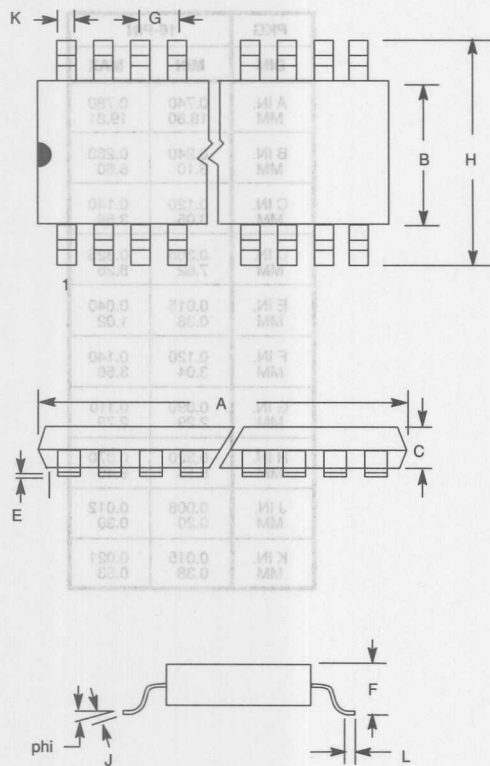
1. The phase relationship between XTAL OUT and RRCLK can be of either form.

DS2188 T1/CEPT JITTER ATTENUATOR 16-PIN DIP



PKG	16-PIN	
	DIM	
A IN.	MIN	MAX
MM		
B IN.	MIN	MAX
MM		
C IN.	MIN	MAX
MM		
D IN.	MIN	MAX
MM		
E IN.	MIN	MAX
MM		
F IN.	MIN	MAX
MM		
G IN.	MIN	MAX
MM		
H IN.	MIN	MAX
MM		
J IN.	MIN	MAX
MM		
K IN.	MIN	MAX
MM		

DS2188S T1/CEPT JITTER ATTENUATOR 16-PIN SOIC

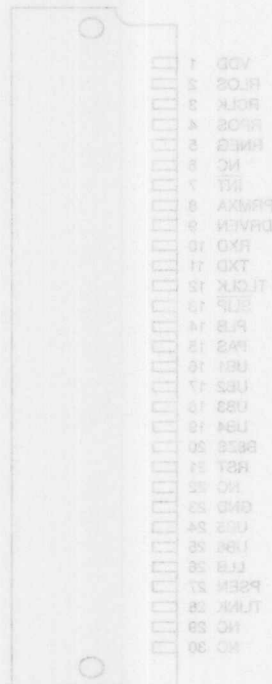


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.40	0.040 1.02
phi	0°	8°

T1 CSU PRODUCTS

D25282
T1 FDL Controller/Monitor Stik

PIN ASSIGNMENT



(actual size)

FEATURES

- Fully implements the FDL message format as described in the ANSI document T1.403-1989
- Fully implements the maintenance message protocol described in AT&T TR 54016 (1986/89)
- Provides high-level monitor counts, namely:
 - Encoded Seconds
 - Severely Encoded Seconds
 - Unavailable Seconds
- Important counts are stored in nonvolatile memory
- Works in conjunction with the D25283 Enhanced T1 Line Card Stik or D25180A T1 Transceiver
- Simple serial port used to retrieve information and control operation
- Can be used without an external controller
- Connects to a standard 30-pin Single In-Line connector
- Single +5V supply

DESCRIPTION

The D25282 completely controls the Facility Data Link (FDL) as described in the Bellcore document TR-TSY-000164 (Extended Superframe Format Interface Specification - December 1987) and the ANSI document T1.403-1989 (Carrier Center Installation - DSI Metallic Interface). It also implements the protocol that

is described in the AT&T publication TR 54016 (Requirements for Interfacing DTE to Services Employing ESF - 1986/89). In addition it provides a number of important performance parameters involved in monitoring T1 lines such as Encoded Seconds, Severely Encoded Seconds, and Unavailable Seconds.

DALLAS

SEMICONDUCTOR

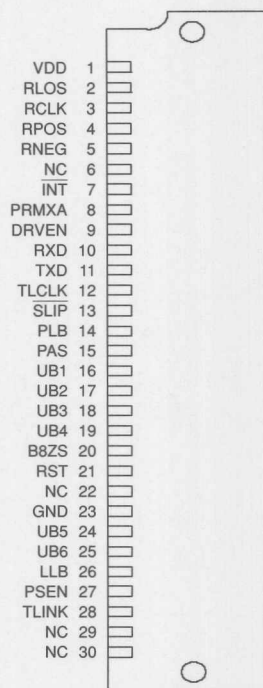
DS2282

T1 FDL Controller/Monitor Stik

FEATURES

- Fully implements the FDL message format as described in the ANSI document T1.403-1989
- Fully implements the maintenance message protocol described in AT&T TR 54016 (1986/89)
- Provides high-level monitor counts, namely:
 - Errored Seconds
 - Severely Errored Seconds
 - Unavailable Seconds
- Important counts are stored in nonvolatile memory
- Works in conjunction with the DS2283 Enhanced T1 Line Card Stik or DS2180A T1 Transceiver
- Simple serial port used to retrieve information and control operation
- Can be used without an external controller
- Connects to a standard 30-pin Single In-Line connector
- Single +5V supply

PIN ASSIGNMENT



(actual size)

DESCRIPTION

The DS2282 completely controls the Facility Data Link (FDL) as described in the Bellcore document TR-TSY-000194 (Extended Superframe Format Interface Specification – December 1987) and the ANSI document T1.403-1989 (Carrier to Carrier Installation – DS1 Metallic Interface). It also implements the protocol that

is described in the AT&T publication TR 54016 (Requirements for Interfacing DTE to Services Employing ESF – 1986/89). In addition it provides a number of important performance parameters involved in monitoring T1 lines such as Errored Seconds, Severely Errored Seconds, and Unavailable Seconds.

OVERVIEW

The DS2282 completely controls the Facility Data Link (FDL) in T1 environments. It can handle the FDL requirements outlined in American National Standards Institute (ANSI) document T1.403-1989 or those outlined in the AT&T publication TR 54016 (1986/89). Recovered data from a T1 line is clocked into the DS2282 via the RPOS and RNEG pins with the RCLK signal. See Figure 1. The DS2282 synchronizes to the incoming data stream and extracts the FDL. Then, it will decode the incoming messages on the FDL and properly create the FDL messages that must be transmitted.

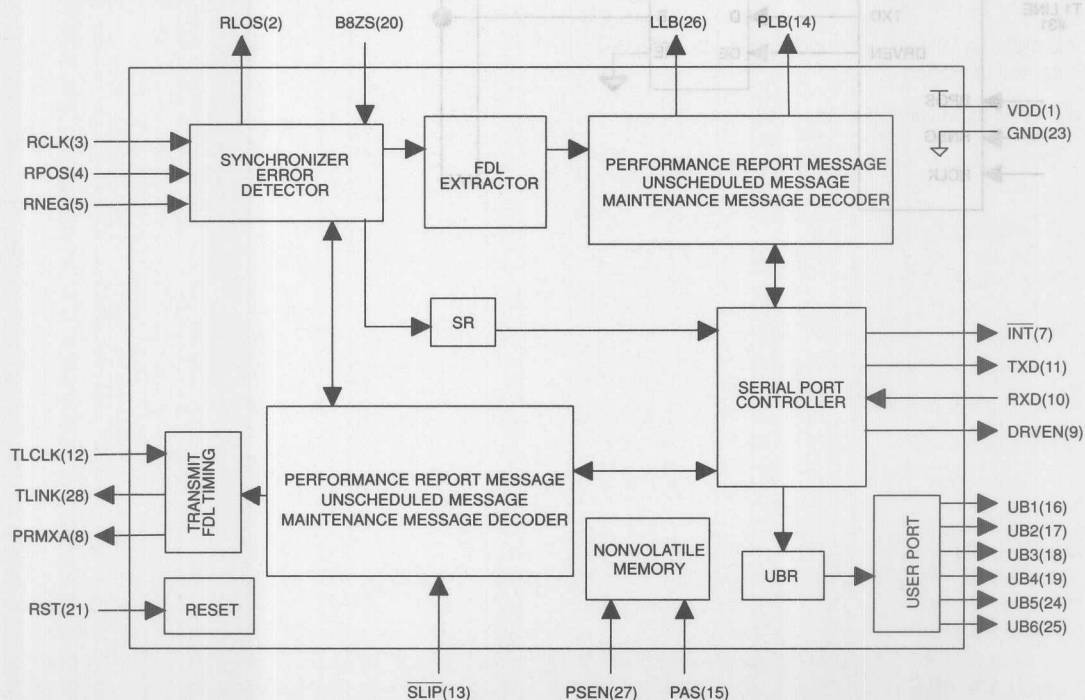
An asynchronous serial port is used to control the DS2282 and to retrieve data from it. The port is operated at 19.2 Kbps. Access to the onboard registers is achieved through the serial port via the TXD and RXD pins. An address can be assigned to this serial port. This allows a single external controller to communicate over a single bus to as many as 31 separate DS2282's.

See Figure 2. Each DS2282 will listen for its address and only respond when it is asked to do so.

Most of the clearable registers in the DS2282 that either count error events or errored time intervals are recorded in onboard, nonvolatile memory. Hence, in case of a local loss of power, these registers will maintain their counts.

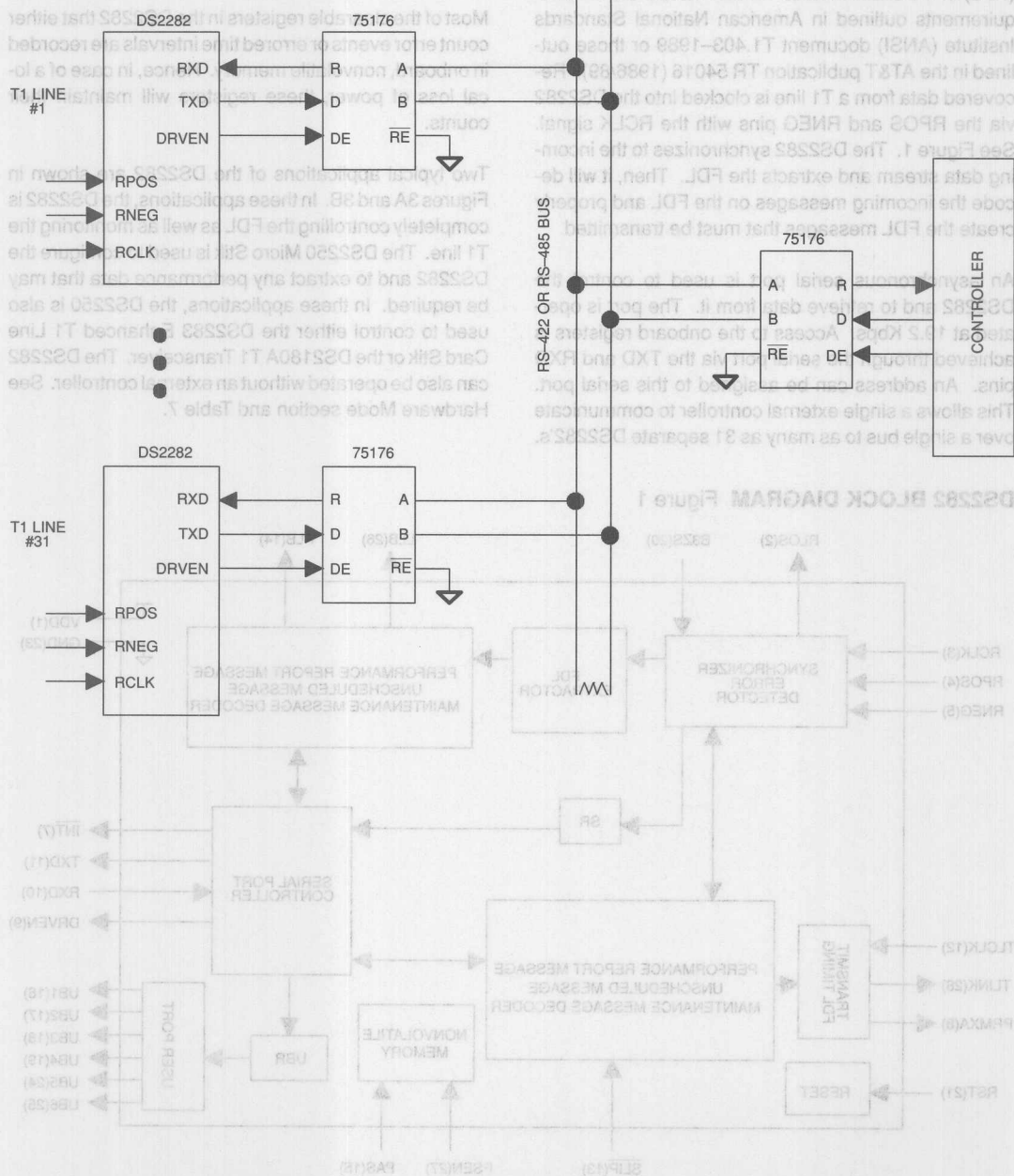
Two typical applications of the DS2282 are shown in Figures 3A and 3B. In these applications, the DS2282 is completely controlling the FDL as well as monitoring the T1 line. The DS2250 Micro Stik is used to configure the DS2282 and to extract any performance data that may be required. In these applications, the DS2250 is also used to control either the DS2283 Enhanced T1 Line Card Stik or the DS2180A T1 Transceiver. The DS2282 can also be operated without an external controller. See Hardware Mode section and Table 7.

DS2282 BLOCK DIAGRAM Figure 1



MULTIPLE DS2282 CONNECTION SCHEME

Figure 2



OVERVIEW

The DS2282 completely controls the Facility Data Link (FDL) in T1 environments. It can handle the FDL re-quirements outlined in American National Standards Institute (ANSI) document T1.403-1988 or those out-lined in the AT&T publication TR 54016 (1988). The DS2282 covers data from a T1 line is clocked into the DS2282 via the RPOS and RNEG pins with the RCLK signal. See Figure 1. The DS2282 synchronizes to the incoming data stream and extracts the FDL. Then, it will de-code the incoming messages on the FDL and pro-cess the FDL messages that must be transmitted over a single due to as many as 31 separate DS2282s. An asynchronous signal is used to control the DS2282 and to receive data from it. The pin is op-erated at 16.5 KHz. Access to the on-board registers is achieved through the TXD and RXD pins. An address can be assigned to this serial port. This allows a single external controller to communicate over a single due to as many as 31 separate DS2282s.

DS2282 BLOCK DIAGRAM Figure 1

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	VDD	—	Positive Supply. 5.0 volts.
2	RLOS	O	Receive Loss Of Sync. Indicates sync status; high when internal resync is in progress, low otherwise.
3	RCLK	I	Receive Clock. 1.544 MHz clock input. All internal time intervals are derived from this clock. A clock must be applied to this pin or the DS2282 will not operate properly.
4 5	RPOS RNEG	I	Receive Bipolar Data. Sampled on falling edge of RCLK. Can be tied together to receive NRZ data and disable BPV and B8ZS detection circuitry.
6	NC	—	No Connect. Do not connect any signal to this pin.
7	INT	O	Interrupt. Transitions low when bits in the Status Register (SR) change state or when an unscheduled message (T1.403) or request message (54016) is received.
8	PRMXA	O	PRM Transmit Active. Transitions high when a Performance Report Message (T1.403) or response message (54016) is being sent via TLINK. DS2282 will transmit 27 flags before each messages. The PRMXA pin will be high for the message and flags.
9	DRVEN	O	Serial Port Drive Enable. Driven high when the DS2282 is transmitting data via TXD. Can be used to enable an external line driver. Tie this pin low to invoke 8-bit communications via the serial port.
10	RXD	I	Serial Port Receive. Serial data input; data is input asynchronously at 19.2Kbps.
11	TXD	O	Serial Port Transmit. Serial data output; data is output asynchronously at 19.2Kbps.
12	TLCLK	I	Transmit Link Clock. 4 KHz demand clock for the FDL data.
13	SLIP	I	Slip Occurrence Event. This edge-triggered pin should be held low for at least 10 μ s when a slip occurs locally. If local slip indications are not available, this pin should be tied low to allow model #3 to be sent in 54016 mode.
14	PLB	O	Payload Loopback. Transitions high when the code word or message for payload loopback activate has been received; transitions low when the code word or message for payload loopback deactivate has been received.
15	PAS	I	Program Address Select. Used to program the serial port address; active high.
16 17 18 19	UB1 UB2 UB3 UB4	O	User Bits 1 to 4. Each user bit can be independently configured either high or low via the UBR register. In hardware mode, tied high or low externally to configure DS2282.
20	B8ZS	I	B8ZS Enable. Tie low to disable B8ZS; tie high to enable B8ZS. Logically OR'ed with the B8ZS bit in the UBR register; tie low if the B8ZS bit is to be used to select B8ZS mode.
21	RST	I	Reset. Active high level will initiate a reset. Contains an internal pull-down resistor.

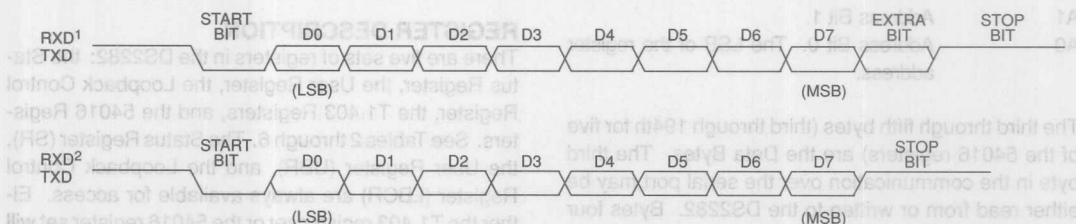
PIN	SYMBOL	TYPE	DESCRIPTION
22	NC	—	No Connect. Do not connect any signal to this pin.
23	GND	—	Ground. 0.0 volts.
24 25	UB5 UB6	O	User Bits 5 to 6. Each user bit can be independently configured either high or low via the UBR register. In hardware mode, tied high or low externally to configure DS2282.
26	LLB	O	Line Loopback. Transitions high when the code word for line loopback activate has been received; transitions low when the code word for line loopback deactivate has been received. This pin does not go active in a 54016 environment.
27	PSEN	—	Program Store Enable. Used in conjunction with the RST pin to program the onboard nonvolatile memory. In normal applications, do not connect any signal to this pin.
28	TLINK	O	Transmit Link Data. FDL data to be transmitted; updated on the falling edge of TLCLK.
29	NC	—	No Connect. Do not connect any signal to this pin.
30	NC	—	No Connect. Do not connect any signal to this pin.

SERIAL PORT OPERATION

The registers in the DS2282 are controlled via a two-wire, asynchronous serial port. All but four of the registers are read-only; UBR, PAR, LBCR, and TUMR are write only. See Tables 2 through 5. Registers on the DS2282 are read from or written to one at a time. Communication over the serial port to one of the registers normally consists of either three, four, or five bytes. (Note: reads from the ESICR, UASICR, BESICR, SESICR, or CSLFICR consists of 194 bytes: two written to the DS2282 and 192 read from the Stik.) The first byte is always written to the DS2282 and is called the Address Byte. Normally, all communications via the asynchronous serial port on the DS2282 are performed in 11-bit

bursts. See Figure 4. There is a Start Bit which is always a zero, followed by eight data bits (LSB first), followed by an Extra Bit which is a one in the Address Byte and a zero in the Register and Data Bytes, followed finally by a Stop Bit which is always a one. If the user wishes to eliminate the need for the Extra Bit in the serial port communications of the DS2282, then either the serial port address on the Stik must be set to decimal 31 (how to set the serial port address on the DS2282 is described in "Initializing the Address of the Serial Port") or the DRVEN pin (pin 9) must be tied permanently low. If the user ties DRVEN low, then the address defaults to zero.

DS2282 SERIAL PORT COMMUNICATIONS Figure 4



NOTES:

1. If the serial port is programmed for addresses between 0 and 30 decimal (inclusive)
2. If the serial port is programmed for address 31 decimal or if DRVEN tied low

(MSB)									(LSB)
EB	0	0	0	A4	A3	A2	A1	A0	

EB	Extra Bit. Should always be set to one.
A4	Address Bit 4. The MSB of the serial port address.
A3	Address Bit 3.
A2	Address Bit 2.
A1	Address Bit 1.
A0	Address Bit 0. The LSB of the serial port address.

The second byte is also always written to the DS2282 and is called the Register Byte. The Register Byte contains the address of the register that is to be either read from or written to. The MSB in the Register Byte is the Clear Bit. The Clear Bit is used to clear a register after it has been read; hence, it can only be used in association with read registers. Furthermore, only certain read registers are clearable. See Tables 1 and 2. Typically, the only registers that can be cleared after reading are registers that count events and/or errors.

Register Byte

(MSB)									(LSB)
CB	0	A5	A4	A3	A2	A1	A0		

CB	Clear Bit. Set to a one if register is to be cleared after reading.
A5	Address Bit 5. The MSB of the register address.
A4	Address Bit 4.
A3	Address Bit 3.
A2	Address Bit 2.
A1	Address Bit 1.
A0	Address Bit 0. The LSB of the register address.

The third through fifth bytes (third through 194th for five of the 54016 registers) are the Data Bytes. The third byte in the communication over the serial port may be either read from or written to the DS2282. Bytes four and five are always read from the DS2282 since there are no write registers longer than one byte. When writing Data Bytes to the DS2282, the Extra Bit must be set to zero and the Extra Bit will be set to zero by the DS2282 for transfers at TXD.

least significant byte is read first and the most significant byte is read last.

As an example, if a DS2282 had been programmed for a serial port address of five (decimal) and the user wished to retrieve and clear the count in the BPV Count Register (BPVCR=09h), then the following transactions would occur:

1. The Address Byte with the Extra Bit set to one and the proper serial port address <100000101> would be written to the DS2282, least significant bit first.
2. The Register Byte with the Clear Bit set to one and the proper register address for the BPVCR selected <100001001> would be written to the DS2282, least significant bit first.
3. The current value in the 24-bit (3-byte) BPVCR is read from the DS2282; the least significant bit in the least significant byte is read first and the most significant bit in the most significant byte is read last.
4. The BPVCR will automatically be reset to zero after the read is completed.

The serial port communication on the DS2282 is handled by the onboard DS5000 Soft Microcontroller. The DS5000 is based on an 8051-type architecture. The DS2282 utilizes the asynchronous Mode 2 operation of an 8051-like microcontroller. Hence, each byte written to the DS2282 must be preceded by a start bit (0) and followed with a stop bit (1). See Figure 4. The DS2282 will append start and stop bits to the bytes that it transmits back to an external controller via the TXD pin. More information on Mode 2 operation can be found in the DS5000 Soft Microcontroller User's Guide.

REGISTER DESCRIPTION

There are five sets of registers in the DS2282: the Status Register, the User Register, the Loopback Control Register, the T1.403 Registers, and the 54016 Registers. See Tables 2 through 6. The Status Register (SR), the User Register (UBR), and the Loopback Control Register (LBCR) are always available for access. Either the T1.403 register set or the 54016 register set will be available depending on whether the DS2282 is programmed via the UBR to operate in either T1.403 or 54016 environments, respectively.

STATUS REGISTER SUMMARY Table 2

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
SR	04	R	Yes	Status Register. An 8-bit register that reports alarm conditions. See "Status Register."

USER REGISTER SUMMARY Table 3

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
UBR ¹	14	W	No	User Bit Register. An 8-bit register that sets the position of the six available user bits. See "User Register."

LOOPBACK CONTROL REGISTER SUMMARY Table 4

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
LBCR	35	W	No	Loopback Control Register. An 8-bit register that determines the actions of the PLB and LLB pins. See "Loopback Control."

SOFTWARE VERSION AND LEVEL REGISTER SUMMARY Table 4A

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
SWVR ¹	3F	R	No	Software Version Register. An 8-bit register that reports the DS2282 software version.
SWLR ¹	3E	R	No	Software Version Level Register. An 8-bit register that reports the DS2282 software version level in two's complement format.

T1.403 REGISTER SET SUMMARY Table 5

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
CRCCR ¹	08	R	Yes	CRC Count Register. A 16-bit register that counts CRC-6 error events.
BPVCR ¹	09	R	Yes	BPV Count Register. A 24-bit register that counts bipolar violations.
OOF CR ¹	0A	R	Yes	OOF Count Register. A 16-bit register that counts OOF error events.
FE CR ¹	0B	R	Yes	Frame Error Count Register. A 16-bit register that counts errors in the FPS framing pattern.
ESR ¹	0C	R	Yes	Errored Second Register. A 16-bit register that counts ES.
SESR ¹	0D	R	Yes	Severely Errored Second Register. A 16-bit register that counts SES.
UASR ¹	0E	R	Yes	Unavailable Seconds Register. A 16-bit register that counts UAS.
PRMR0	10	R	No	Performance Report Message Registers. Four 8-bit registers that contain the PRMs that were received in the FDL in the last four seconds.
PRMR1	11	R	No	
PRMR2	12	R	No	
PRMR3	13	R	No	
RUMR	18	R	Yes	Receive Unscheduled Message Register. An 8-bit register that reports unscheduled messages as they are received.

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
TUMR	19	W	No	Transmit Unscheduled Message Register. An 8-bit register that is used to send unscheduled messages.
PRMESR ¹	1C	R	Yes	PRM Errored Second Register. A 16-bit register that counts ES as reported in the PRM.
PRMSESR ¹	1D	R	Yes	PRM Severely Errored Second Register. A 16-bit register that counts SES as reported in the PRM.
PRMER ¹	1E	R	Yes	PRM Error Register. An 8-bit register that counts PRMs that are received in error.
PAR ¹	1F	W	No	PRM Address Register. An 8-bit register determines the action of the PRM opening address.

NOTES:

1. Register is nonvolatile.
2. Values indicated in hexadecimal format.
3. All registers read/written LSB first.

STATUS REGISTER (04)

The Status Register (SR) reports alarms and events. The SR is always cleared when it is read by an external controller, hence the Clear Bit in the Register Byte does not need to be set. All of the bits in the SR operate in a “latched” fashion. That is, once an event or alarm has occurred, the appropriate bit in the SR will remain set until the SR is read. All of the bits in the SR will be cleared when read unless the alarm condition still exists. Also, except for the B8ZSD bit, the INT pin will be asserted (transitions low), indicating to an external controller that a bit in the SR has changed status. The INT pin will return high as soon as the status register is accessed.

SR: Status Register (04)

(MSB)							(LSB)
PLB	LLB	16ZD	RCL	RYEL	RLOS	B8ZSD	AIS

- PLB Payload Loopback. Set when payload loopback is active.
- LLB Line Loopback. Set when line loopback is active. Will not go active in 54016 environments.
- 16ZD Sixteen Zero Detect. Set when 16 consecutive zeros are received. An indication of a pulse density violation.
- RCL Receive Carrier Loss. Set when 192 consecutive zeros have been received.

- RYEL Receive Yellow Alarm. Set when 16 consecutive 00FF Hex codes have been received in the FDL.
- RLOS Receive Loss of Sync. Set when the DS2282 loses synchronization.
- B8ZSD B8ZS Detect. Set when a B8ZS code word is received; operates whether the DS2282 is set up for B8ZS or not. Does not affect INT.
- AIS Alarm Indication Signal. Set when an unframed all one's signal is received.

SOFTWARE VERSION REGISTER

The software version register (SWVR) (3F) allows the user to display software version information. When accessed, the DS2282 software revision will be returned by the serial port. For example, the serial port will return 0Bh for software version V11.

SOFTWARE LEVEL REGISTER

The software level register (SWLR) (3E) allows the user to display software version level information. When accessed, the two's complement of the DS2282 software revision level will be returned by the serial port. If the returned value is negative, the software revision level is in “beta” or prototype state. If positive, the software revision level is the production release. For example, the serial port will return 05h for production software version level V11.5 (FBh for “beta” release).

USER REGISTER (14)

The DS2282 contains a 6-bit user port (pins UB1 to UB6). An external controller can independently set or clear these user bits via the User Bit Register (UBR). The UBR is also used to select whether the DS2282 is to operate in a T1.403 or a 54016 environment. If the 54016 bit is set to a one, then the DS2282 will operate in a 54016 fashion and the 54016 register set will be selected. If the 54016 bit is cleared (set to zero), then the DS2282 will operate in a T1.403 fashion and the T1.403 register set will be selected. Operation in both modes simultaneously is not allowed. If the user accesses the opposite mode's register set, a value of 00h is returned. For example, 00h will be returned if the DS2282 is programmed for TR54016 mode and the user reads address location 08h (CRCCR). The B8ZS bit should be set to a one when the DS2282 is connected to T1 streams that include B8ZS code words. The default for the UBR is 00 hex.

UBR: User Bit Register (14)

(MSB)								(LSB)
B8ZS	54016	UB6	UB5	UB4	UB3	UB2	UB1	
B8ZS		B8ZS Select. Logically OR'ed with the B8ZS pin.						
54016		54016 Select. Set to a one in a 54016 environment.						
UB6		User Bit 6. Sets or clears the UB6 pin.						
UB5		User Bit 5. Sets or clears the UB5 pin.						
UB4		User Bit 4. Sets or clears the UB4 pin.						
UB3		User Bit 3. Sets or clears the UB3 pin.						
UB2		User Bit 2. Sets or clears the UB2 pin.						
UB1		User Bit 1. Sets or clears the UB1 pin.						

54016 REGISTER SET SUMMARY Table 6

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
CSR	20	R	No	Current Status Register. An 8-bit register that indicates unavailable signal state and PLB status.
ESFEER	21	R	No	ESF Error Event Register. A 16-bit register that accumulates ESF error events.
CIT	22	R	No	Current Interval Timer. A 16-bit register that counts the number of seconds in the current 15-minute interval.
CIESR	23	R	No	Current Interval ES Register. A 16-bit register that indicates the number of Errored Seconds in current 15-minute interval.
CIUASR	24	R	No	Current Interval UAS Register. A 16-bit register that indicates the number of Unavailable Seconds in current 15-minute interval.
CIBESR	25	R	No	Current Interval BES Register. A 16-bit register that indicates the number of Bursty Errored Seconds in current 15-minute interval.
CISESR	26	R	No	Current Interval SES Register. A 16-bit register that indicates the number of Severely Errored Seconds in current 15-minute interval.
CICSLFR	27	R	No	Current Interval CSS & LOFC Register. A 16-bit register that counts Controlled Slip Seconds and Loss of Frame in current 15-minute interval. The 8-bit CSS count is in the LSB and the 8-bit LOFC count is in the MSB.
ESICR	28	R	No	ES Interval Count Registers. A set of 96 16-bit registers that contain the Errored Second counts for the previous 96 individual 15-minute periods. Most recent interval is read first.

NAME	ADDR ^{2,3}	R/W	CLEARABLE	DESCRIPTION
UASICR	29	R	No	UAS Interval Count Registers. A set of 96 16-bit registers that contain the Unavailable Second counts for the previous 96 individual 15-minute periods. Most recent interval is read first.
BESICR	2A	R	No	BES Interval Count Registers. A set of 96 16-bit registers that contain the Bursty Errored Second counts for the previous 96 individual 15-minute periods. Most recent interval is read first.
SESI CR	2B	R	No	SES Interval Count Registers. A set of 96 16-bit registers that contain the Severely Errored Second counts for the previous 96 individual 15-minute periods. Most recent interval is read first.
CSLFICR	2C	R	No	CSS & LOFC Interval Count Registers. A set of 96 16-bit registers that contain the Controlled Slip and Loss Of Frame counts for the previous 96 individual 15-minute periods. The 8-bit CSS count is the LSB and the 8-bit LOFC count is in the MSB. Most recent interval is read first.
ESDCR	2D	R	No	ES Day Count Registers. A 16-bit register that counts the number of Errored Seconds in the previous 24-hour period.
UEEER	36	R	Yes	User ESF Error Event Register. 16-bit register that mimics the ESFEER for user access.
UASDCR	2E	R	No	UAS Day Count Registers. A 16-bit register that counts the number of Unavailable Seconds in the previous 24-hour period.
BESDCR	2F	R	No	BES Day Count Registers. A 16-bit register that counts the number of Bursty Errored Seconds in the previous 24-hour period.
SESDCR	30	R	No	SES Day Count Registers. A 16-bit register that counts the number of Severely Errored Seconds in the previous 24-hour period.
CSLFDCR	31	R	No	CSS & LOFC Day Count Registers. A 16-bit register that counts the number of Controlled Slip Seconds and Loss Of Frames in the previous 24-hour period. The 8-bit CSS count is in the LSB and the 8-bit LOFC count is in the MSB.
VITR	32	R	No	Valid Interval Total Register. An 8-bit register that indicates the number of valid 15-minute intervals in the previous 24-hour period.
RMSR	33	R	Yes	Request Message Status Register. An 8-bit register that indicates which (if any) request message is being received.
CR	34	W	No	Control Register. An 8-bit register that selects which address the DS2282 will respond to.

NOTES:

1. All of the registers in the DS2282 that count events will saturate at their maximum possible count; they do not roll over. For example, all the 16-bit registers stop at a count of 65,535. They do not roll over to zero and continue counting.
2. Values indicated in hexadecimal format.
3. All register read/written LSB first.

T1.403 OPERATION

In order to properly operate on T1 lines running the FDL under the definition spelled out in the ANSI document T1.403, the DS2282 must have the 54016 bit in the UBR set to zero (see "User Register"). The DS2282 will decode both the incoming Performance Report Messages (PRM) and unscheduled messages and provide them for the user. The DS2282 also collects data on bipolar violations (BPV), frame errors, CRC-6 errors, and Out-of-Frame errors (OOF). The DS2282 combines the information in these registers along with the indication of local slips via the SLIP signal to create PRMs that are transmitted once a second via the TLINK signal. Also, the user can instruct the DS2282 to transmit unscheduled messages. For more information on the T1.403 definition, refer to the application note "T1.403 FDL Message Overview."

Monitor Registers

There are two sets of monitor registers. The first set helps support some of the monitoring requirements on T1 lines as spelled out in documents such as TA-TSY-000147 (DS1 Rate Digital Service Monitoring Unit Functional Specifications - October 1987), TR 62411 (Accunet* T1.5 Service Description and Interface Specifications - December 1988), and the CCITT recommendation G.821. This set consists of three registers, the Errored Seconds Register (ESR), the Severely Errored Seconds Register (SES), and the Unavailable Seconds Register (UAS). Unlike the first set of monitor registers which provides a count of conditioned data, the second set of monitor registers just provides raw data counts of events such as CRC-6 errors, bipolar violations, frame errors, and out of frame errors. The second set of monitor registers consists of four registers: the CRC Count Register (CRCCR), the Bipolar Violation Count Register (BPVCR), the Frame Error Count Register (FEER), and the Out Of Frame Count Register (OOFER). All of the monitor registers are described below.

ESR: Errored Seconds Register (0C). A 16-bit register that counts Errored Seconds (ES). An ES is any one-second time interval with either a frame bit error, CRC-6 error, OOF event, or controlled slip event.

SES: Severely Errored Seconds Register (0D). A 16-bit register that counts Severely Errored

Seconds (SES). A SES is any one-second time interval with an OOF error event and/or more than 320 CRC-6 errors in it.

UASR: Unavailable Seconds Register (0E). A 16-bit register that counts Unavailable Seconds (UAS). A UAS is the number of seconds between 10 consecutive SES events (inclusive) and 10 consecutive non-SES events (exclusive). The DS2282 starts counting SES events when it receives the first one. If it counts ten SESs in a row, then it increments the UASR by ten and decrements the ES and SES by ten. Counts in the ESR and SESR are inhibited during unavailable seconds. Once the DS2282 has begun counting unavailable seconds, it begins counting non-SES events. At the first non-SES event, it begins counting Errored Seconds in a separate register that is not available to the user. If the DS2282 fails to count ten non-SES events in a row, it clears both the non-SES count and the register counting Errored Seconds during unavailable seconds. If it counts ten non-SES events in a row, it will decrement the UASR by ten and will increment the ESR by the count in the register counting Errored Seconds during unavailable seconds. Also, when the DS2282 detects either an incoming Alarm Indication Signal (AIS) or Receive Carrier Loss (RCL), it will increment the UASR for each second either of these conditions exists.

CRCCR: CRC-6 Error Count Register (80). A 16-bit register that records CRC-6 error events. The DS2282 calculates CRC-6 on the incoming data. Each time the calculation does not match the CRC-6 code word in the incoming ESF data stream, then the CRCCR is incremented by one.

BPVCR: Bipolar Violation Count Register (81). A 24-bit register that records bipolar violations (line code violations). Bipolar violations are counted whether the synchronizer in the DS2282 is in sync (the RLOS signal is low) or not. If the DS2282 is set up to receive B8ZS code words, then B8ZS code words are not counted as bipolar violations.

FEER: Frame Error Count Register (83). A 16-bit register that records errors in the Framing Pattern Sequence (FPS). All individual bit errors in the FPS pattern (001011) are recorded in the FEER.

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OOFCR: Out Of Frame Count Register (82). A 16-bit register that records Out Of Frame (OOF) error events. An OOF error event occurs whenever 2 or more framing bits out of 6 in the FPS are incorrect. An OOF error event will cause the DS2282 to resynchronize to the incoming data stream.

Receive PRM Operation

The DS2282 decodes the incoming FDL for scheduled Performance Report Messages (PRM). It automatically detects opening flags, deletes any stuffed zero bits that may be present, and it calculates CRC-16 on all the data between the opening and closing flags. The DS2282 normally only decodes the current second's data (octets 5 and 6). Data from the previous three seconds is "bumped" from PRMR0 to PRMR1 to PRMR2 to PRMR3 and finally out of available recall range. If the PRM is received in error (CRC check sum is incorrect), the message will be ignored. The DS2282 will keep track of errored PRMs and properly place the unerrored message when it is received. For example, if a PRM is received that does not correspond to its CRC check sum, then PRMR0 will be set to all zeros indicating that an invalid message was received. If the next scheduled message is received correctly, then the data missed in the last scheduled message will be updated to PRMR1.

NOTE: PRMR0 to PRMR3 are only updated if PRMs are received; if no valid or invalid PRMs are received, then both the SE and FE bits in PRMR0 to PRMR3 will be set to one.

- PRMR0: PRM Register 0 (10)**
- PRMR1: PRM Register 1 (11)**
- PRMR2: PRM Register 2 (12)**
- PRMR3: PRM Register 3 (13)**

(MSB)				(LSB)			
PLB	SL	LV	SE	FE	CRC2	CRC1	CRC0

- PLB Payload Loopback Activated
- SL Controlled Slip (slip ≥ 1)
- LV Line Violation (BPV ≥ 1)
- SE Severely Errored Framing Event (2 of 6 OOF ≥ 1)
- FE Frame Sync Bit Error Event
- CRC2 See Table Below
- CRC1 See Table Below
- CRC0 See Table Below

CRC2	CRC1	CRC0	EVENT
0	0	0	Invalid
0	0	1	CRC=0
0	1	0	CRC=1 (G1)
0	1	1	1 < CRC ≤ 5 (G2)
1	0	0	5 < CRC ≤ 10 (G3)
1	0	1	10 < CRC ≤ 100 (G4)
1	1	0	100 < CRC ≤ 319 (G5)
1	1	1	CRC ≥ 320 (G6)

PRM History Registers

There are three registers that keep track of the scheduled PRM and collect data on the receive performance of the remote end. The first two of these registers (PRMESR and PRMSESR) mock the monitor registers in the type of data that they report. ES and SES are calculated off of the received PRM data. The PRM data is pulled from PRMR3 since it has the highest probability of containing valid data. If PRMR3 does not contain valid data, then ES and SES are not calculated. The third register (PRMER) keeps a count of how many PRMs have been received in error.

PRMESR: PRM Errored Seconds Register (1C). A 16-bit register that counts Errored Seconds (ES). An ES is any one second time interval with either a frame bit error (FE or SE=1) or CRC-6 error (G1 to G6=1).

PRMSESR: PRM Severely Errored Seconds Register (1D). A 16-bit register that counts Severely Errored Seconds (SES). A SES is any one second time interval with an OOF error event (SE=1) or more than 320 CRC-6 error events (G6=1).

PRMER: PRM Error Register (1E). An 8-bit register that records the number of PRMs that have been received in error. A PRM is considered to be received in error when the calculated CRC does not match the incoming CRC word.

Transmit PRM Operation

The DS2282 will automatically generate PRMs once a second to be included into the FDL for transmission to the remote end. It automatically pulls together all the

necessary data to create a PRM from both the monitor registers and from the SLIP signal. It creates the opening and closing flags as well as the address and control bytes. Once the PRM packet has been assembled, the DS2282 will generate CRC-16 and include it at the end of the PRM. And finally, before the PRM is sent, zeros are inserted to insure that none of the PRM data appears as a flag.

Receive Unscheduled Message Operation

The DS2282 decodes incoming unscheduled messages as they are received. The DS2282 will report the received unscheduled message via the RUMR when the message has been received for three consecutive times. This integration allows the DS2282 to operate properly even on high bit error rate lines. The RUMR is cleared when read via the serial port. The INT pin will be asserted (transitions low), indicating to an external controller that an unscheduled message has been received three consecutive times. The user may count incoming unscheduled messages by monitoring the INT pin. The INT pin will return high as soon as the RUMR is accessed.

Two output signals on the DS2282 will respond to certain unscheduled messages. The PLB (Payload Loopback) signal will transition high if the code word for payload loopback activate (001010) is received three times. It will remain high until the DS2282 has received the payload loopback deactivate code word (011001) three times. The LLB (Line Loopback) signal operates similarly. The LLB signal will transition high when the DS2282 has received the code word for line loopback activate (000111) three times. It will remain high until the DS2282 has received the code word for line loopback deactivate (011100) three times. The user has the option to control the PLB and LLB pins via the Loopback Control Register (LBCR); see "Loopback Control Register."

RUMR: Receive Unscheduled Message Register (18)

(MSB)				(LSB)			
NA	NA	CW5	CW4	CW3	CW2	CW1	CW0

NA Not Assigned. Could be any value when read.

NA Not Assigned. Could be any value when read.

CW5 MSB of the Receive Unscheduled Message Code word.

CW0 LSB of the Receive Unscheduled Message Code word.

Transmit Unscheduled Message Operation

The DS2282 will transmit outgoing unscheduled messages. The DS2282 will continuously transmit the unscheduled message described in TUMR if enabled via the TUM bit in the TUMR. If unscheduled messages are being transmitted, all PRMs are superseded. When the TUM is cleared, the DS2282 will finish sending the unscheduled message that it is currently transmitting before switching to either the idle code or PRMs.

TUMR: Transmit Unscheduled Message Register (19)

(MSB)				(LSB)			
TUM	0	CW5	CW4	CW3	CW2	CW1	CW0

TUM Transmit Unscheduled Message Enable

CW5 MSB of the Transmit Unscheduled Message Code word.

CW0 LSB of the Transmit Unscheduled Message Code word.

PAR: PRM Address Register (1F). The DS2282 allows the user to set the PRM opening address C/R bit depending on the source of the PRM. The C/R bit is set to zero for PRMs created by user equipment such as a CPE or set to one for PRMs created by a carrier. The PAR allows the user to control the expected state of the C/R bit as well as control the state of the bit in the PRMs created by the DS2282.

(MSB)						(LSB)	
0	0	0	0	0	0	TC/R	RC/R

TC/R Transmit PRM C/R Bit Control
0=force C/R bit to zero in outgoing PRM
1=force C/R bit to one in outgoing PRM

RC/R Receive PRM C/R Bit Control
0=only respond to RPM with the C/R bit set to zero
1=only respond to PRM with the C/R bit set to one

54016 OPERATION

In order to properly operate on T1 lines running the FDL under the definition spelled out in the AT&T Publication TR 54016, the DS2282 must have the 54016 bit in the UBR set to one (see "User Register"). The DS2282 monitors the incoming FDL for maintenance messages from the network. It will decode these messages and respond accordingly. The DS2282 will automatically monitor the T1 and accumulate the statistics that might be requested from the network. All of the information that is gathered by the DS2282 is locally available to the user. The 54016 register set in the DS2282 mimics the registers defined in TR 54016. When the DS2282 is not responding to maintenance messages, it transmits FFh or 7Eh programmed by the control register (CR) of user bits (UB) in the hardware mode.

CSR: Current Status Register (20). The 8-bit Current Status Register (CSR) contains information on whether an unavailable signal state or Payload Loopback is active.

0	CWS	CWS	CWS	CWS	CWS	CWS	CWS
---	-----	-----	-----	-----	-----	-----	-----

CSR: Current Status Register (20)

(MSB)	F	U	0	0	0	0	L	0	(LSB)
-------	---	---	---	---	---	---	---	---	-------

- F F=1 if either U or L is set to a one
U U=1 if an unavailable signal state exists
L L=1 if the Payload Loopback (PLB) is active

ESFEER: ESF Error Event Register (21). A 16-bit register that counts ESF error events. Each ESF is checked for the occurrence of an error event. An error event is defined as the logical OR'ing of CRC-6 error events and Out Of Frame (OOF) events. A CRC-6 error event occurs when the locally calculated CRC-6 code does not match the incoming CRC-6 code. An OOF event occurs when 2 out of 4 consecutive framing bits are received in error.

UEEER: User ESF Error Event Register (36). A 16-bit register that mimics the ESF Error Event Register (ESFEER). Unlike the ESFEER, the UEEER is user clearable once saturated by network error events. This simplifies operations when user registers are created external from the DS2282.

CIT: Current Interval Timer (22). A 16-bit register that counts the number of seconds in the current 15 minute interval. Since there can only be 900 seconds in a 15 minute interval, this register will never saturate. Since all of the time intervals in the DS2282 are derived from the T1 source, the accuracy of this timer depends on the accuracy of the RCLK signal.

Current Interval Registers

The current interval registers count the number of events that have occurred in the current 15 minute interval. There are five separate current interval registers. They are:

- CIESR (23) counts Errored Seconds (ES)
CIUASR (24) counts Unavailable Seconds (UAS)
CIBESR (25) counts Bursty Errored Seconds (BES)
CISESR (26) counts Severely Errored Seconds (SES)
CICSLFR (27) counts Controlled Slip Seconds (CSS) and Loss Of Frame Counts (LOFC)

Each of these current interval registers is 16 bits in length. Please see "54016 Definitions" for definitions of ES, UAS, BES, SES, CSS, and LOFC.

Interval Count Registers

The interval count registers are a set of 96 separate 16-bit registers that contain the number of events that have occurred in each of the previous 96, individual 15 minute periods. Or in other words, the interval count registers contain the performance of the T1 line for the previous 24 hours broken into 15 minute periods. There are five separate interval count registers. They are:

- ESICR (28) contains Errored Seconds (ES)
UASICR (29) contains Unavailable Seconds (UAS)
BESICR (2A) contains Bursty Errored Seconds (BES)
SESICR (2B) contains Severely Errored Seconds (SES)
CSLFICR (2C) contains Controlled Slip Seconds (CSS) and Loss Of Frame Counts (LOFC)

Please see "54016 Definitions" for definitions of ES, UAS, BES, SES, CSS, and LOFC.

NA	NA	CWS	CWS	CWS	CWS	CWS	CWS
----	----	-----	-----	-----	-----	-----	-----

Day Count Registers

The day count registers count the number of events that have occurred in the previous 24 hour period. There are five separate day count registers. They are:

- ESDCR (2D) counts Errored Seconds (ES)
- UASDCR (2E) counts Unavailable Seconds (UAS)
- BESDCR (2F) counts Bursty Errored Seconds (BES)
- SESDCR (30) counts Severely Errored Seconds (SES)
- CSLFDCR (31) counts Controlled Slip Seconds (CSS) and Loss Of Frame Counts (LOFC)

Each of these current interval registers are 16 bits in length. Please see "54016 Definitions" for definitions of ES, UAS, BES, SES, CSS, and LOFC.

VITR: Valid Interval Total Register (32). An 8-bit register that counts the number of 15 minute intervals since the last reset. Hence, it has a maximum count of 96.

RMSR: Request Message Status Register

(33). An 8-bit register that indicates which (if any) request maintenance message has been received. If a request maintenance message is received, the INT pin will be asserted (transitions low). The RMSR will be cleared when read. This indicates to an external controller that a request has been received and is being processed. The INT pin will return high as soon as the RMSR is accessed. There are currently 15 request messages defined.

(MSB)				(LSB)			
RM7	RM6	RM5	RM4	RM3	RM2	RM1	RM0

RM7 MSB of the request message
RM0 LSB of the request message

CR: Control Register (34). An 8-bit register that selects whether the DS2282 will respond to address A (or Z) or address B (or Y). The default is for the DS2282 to respond only to address A (or Z). The user can set the DS2282 to respond address B (or Y) by setting the AD

bit to a one. In addition, CR allows the user to send an all one's sequence FFh or LAPD idel code 7Eh.

(MSB)						(LSB)	
0	0	0	0	0	0	ICS	AD

AD Address Select Bit: Set to a one to respond to address B (or Y)

ICS Idle Code Select

0 = FFh

1 = 7Eh

54016 DEFINITIONS

Errored Seconds (ES): A one-second period with either:

- a. one or more CRC-6 error events or
- b. one or more OOF events or
- c. one or more controlled slips.

Severely Errored Seconds (SES): A one-second period with either:

- a. 320 or more CRC-6 error events or
- b. one or more OOF events.

Unavailable Seconds (UAS): A one-second period in which an unavailable signal state is present. In counting UAS, the initial period of 10 consecutive SES's is included in the count whereas the final 10 seconds of 10 consecutive non-SES's which removes the unavailable signal state is not included in the count. During UAS's, neither ES, or SES, or BES, are counted. Refer to "Monitor Registers" for a more detailed description of UAS.

Unavailable Signal State: An unavailable signal state is declared when 10 consecutive SESs have been received. An unavailable signal state is considered cleared when 10 consecutive non-SES events have occurred.

Controlled Slip Seconds (CSS): A one-second period with one or more controlled slips. A controlled slip is the deletion or replication of a DS1 frame. Indications of controlled slips are input to the DS2282 via the SLIP pin. If indications of controlled slips are not available, the SLIP pin should be tied low.

Loss Of Frame Count (LOFC): A count of the number of times Loss Of Frame (LOF) has been declared. An LOF is declared by the following method. Each super-frame (3 ms) will be examined for a LOF event. If an event is present, then an internal counter (which is not available to the user) will be incremented by five, if no event is present, then the counter will be decremented by one. When the counter crosses a boundary of 4166 (2.5 sec x 333.3 SF/sec x 5 counts/SF) then a LOF will be declared and the LOFC will be incremented by one. At this point, the counter will be reset to zero when for at least one full second, a LOF has not occurred.

Bursty Errored Seconds (BES): A one-second period with more than one but less than 320 CRC-6 error events.

ESF Error Event: Each ESF is checked for either a CRC-6 event or an OOF event.

INITIALIZING THE ADDRESS OF THE SERIAL PORT

The serial port on the DS2282 can be assigned an address from 0 to 30 decimal. Address location 31 decimal will set the serial port into a mode where the Extra Bit is not needed in the communications over the serial port (see "Serial Port Operation"). The default address is 0 decimal. The DS2282 is shipped from the factory with the default value in place. The address can be programmed in the following manner:

1. Power down the DS2282.
2. Set the Program Address Select pin to be pulled high when power is applied.
3. Configure the User Bits 1 to 5 with the desired address; UB1 is the LSB, UB5 is the MSB.
4. Leave all other pins open.
5. Apply power to the DS2282 for at least 1 second.
6. Power down the DS2282.
7. Set the Program Address Select pin to remain low when power is reapplied.

At this point, the DS2282 will be programmed to the proper value. Assigning a new address value can be performed with the same procedure. The address value is stored in nonvolatile memory.

NONVOLATILE STORAGE

The DS2282 can retain its onboard program and the contents of the nonvolatile registers for at least ten years in the absence of power at room temperature. If power is applied to the DS2282 at least 50% of the time, the nonvolatile storage will last at least 20 years.

SINGLE IN-LINE CONNECTOR

The DS2282 is designed to connect directly into a 30-position Single In-Line connector. These connectors are available from a number of vendors.

LOOPBACK CONTROL REGISTER

The Loopback Control Register (LBCR) allows the user to determine the action of the Payload Loopback (PLB) and Line Loopback (LLB) pins. The user has the option to either allow the DS2282 to respond normally to loopbacks, as described in "Receive Unscheduled Message Operation," or to force the PLB or LLB pins high or low. The default value for the LBCR is 00 hex. In addition, the LCR allows the user to automatically interrupt the transmission of the yellow alarm to either send a PRM (T1.403) or a Response Message—RM (54016) by setting the IYA bit. The yellow alarm interrupt routine transmits 27 opening flags to insure synchronization by the far end receiver prior to transmitting a PRM or RM. Within the T1.403 mode, an Unscheduled Message enabled by the TUMR register will override the transmission of the interruptable yellow alarm. Also, the LBCR allows a software method of disabling local slip indications by setting the DS bit. This enables the Enhanced Configuration Data Response (model #3) to be sent in 54016 mode, when local slip indication is disabled.

(MSB)				(LSB)			
0	DS	IYA	0	DLLB	FLLB	DPLB	FPLB

DS

Disable Local SLIP Indications.

0 = follow the SLIP pin for SLIP indications (this includes disabling slip counts by permanently tying the SLIP pin low)

1 = force the disabling of local slip indications regardless of the SLIP pin

IYA

Interruptable Yellow Alarm Enable.

0 = do not transmit an interruptable yellow

DLLB	Disable Automatic LLB Action. 0 = allow the LLB pin to act normally 1 = force the LLB pin to the value in FLLB
FLLB	Force LLB. 0 = force the LLB pin low 1 = force the LLB pin high
DPLB	Disable Automatic PLB Action. 0 = allow the PLB pin to act normally 1 = force the PLB pin to the value in FPLB
FPLB	Force PLB. 0 = force the PLB pin low 1 = force the PLB pin high

provisioned by connecting the UB5 pin to GND. If the UB5 pin is left floating, the software mode is enabled for serial port operations. In the hardware mode, the DS2282 will continue to monitor and supply the FDL data stream messages automatically without any interaction by the user. B8ZS, T1.403, and 54016 operating modes are configured by external pin connections, along with the PRM C/R bit control, address, and idle code selects indicated by the hardware mode table. The external UB pins (1–6) are read during power up or reset events. After power up or reset occurs, the defined hardware operating mode can be changed in software via the corresponding register bits.

HARDWARE MODE

The DS2282 provides an optional hardware mode for operation without an external controller. The external

HARDWARE MODE Table 7

PIN	SYMBOL	REGISTER BIT	DESCRIPTION
24	UB5	N/A	0 (GND) = Hardware Select, N/C (Floating) = Software Select
20	B8ZS	UBR–B8ZS	B8ZS Select Pin. 1 = enabled, 0 = disabled
19	UB4	UBR–54016	Mode Select Pin. 0 (GND) = T1.403, N/C (Floating) = TR54016
16	UB1	PAR–RC/R	Receive PRM C/R Bit Control Pin for T1.403 Mode. 0 (GND) = only respond to PRM with C/R bit set to one. N/C (Floating) = only respond to PRM with C/R bit set to zero.
		CR–AD	Address Select Bit Control Pin for TR54016. 0 (GND) = respond to address B (or Y). N/C (Floating) = respond to address A (or Z).
16	UB2	PAR–TC/R	Transmit PRM C/R Bit Control Pin for T1.403 Mode. 0 (GND) = force C/R bit to one in outgoing PRM. N/C (Floating) = force C/R bit to zero in outgoing PRM.
		CR–ICS	Idle Code Select Bit Control Pin for TR54016. 0 (GND) = 7E (h) N/C (Floating) = FF (h).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

-0.3V to V_{CC}

0°C to +70°C

0°C to 70°C

260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	3
Logic 1 for RST	V_{IH}	3.5		$V_{CC}+0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.75		5.25	V	

CAPACITANCE(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		30		pF	24
Output Capacitance	C_{OUT}		50		pF	20

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		30		mA	1
Static Input Leakage	I_I	-50		+50	μA	2, 3
Output Voltage (80 μA)	V_{OH}	2.4	4.8		V	18
Output Voltage (1.6 mA)	V_{OL}		0.15	0.45	V	
RST Pull-down Resistance	R_{PD}	40		125	KΩ	

NOTES:

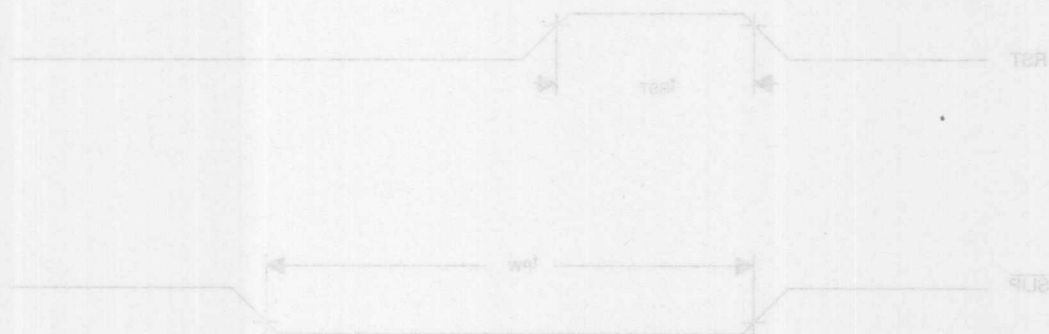
1. RCLK=1.544 MHz; $V_{DD}=5.25V$; outputs open; inputs tied low
2. $V_{IN}=4.5$ volts
3. Does not apply to RST

AC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

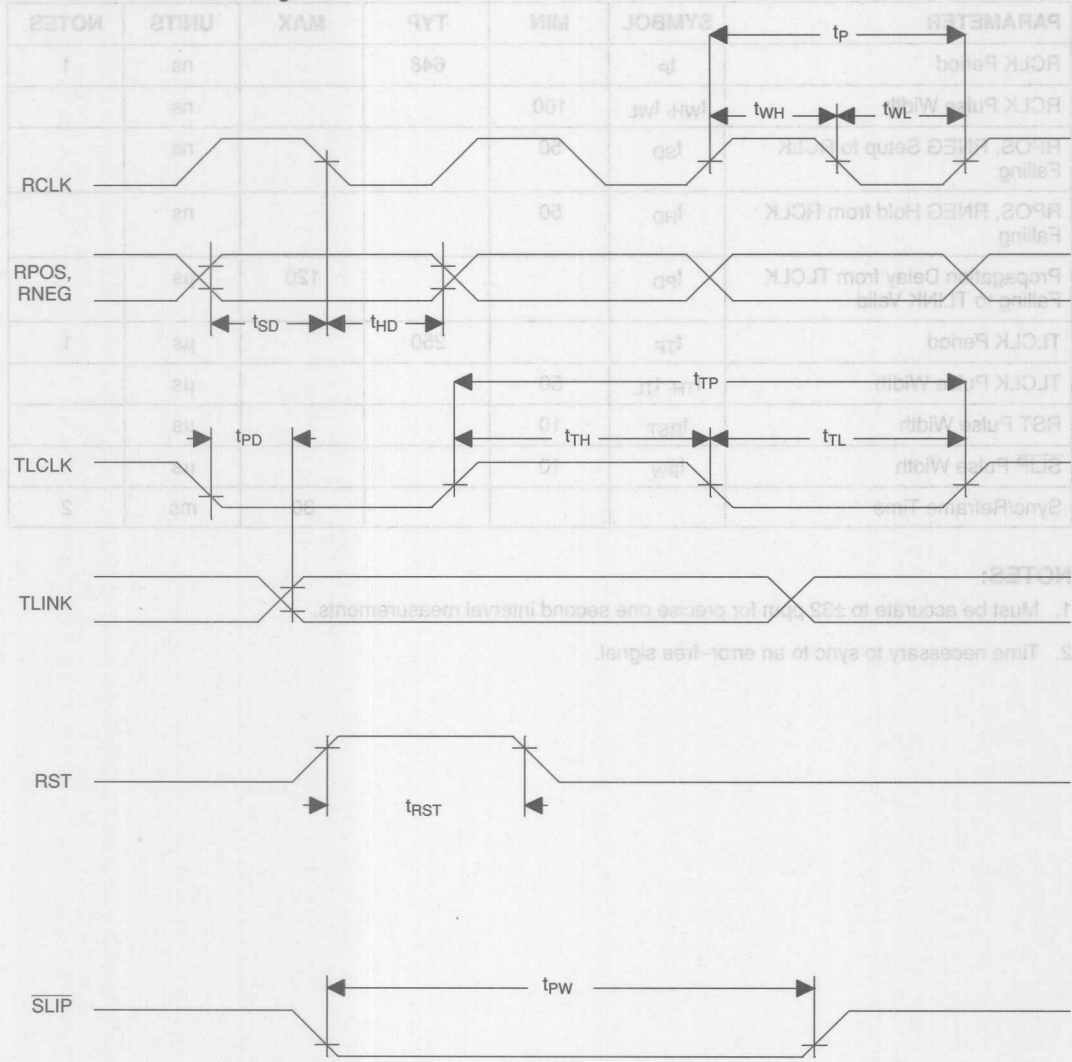
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_P		648		ns	1
RCLK Pulse Width	t_{WH}, t_{WL}	100			ns	
RPOS, RNEG Setup to RCLK Falling	t_{SD}	50			ns	
RPOS, RNEG Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay from TLCLK Falling to TLINK Valid	t_{PD}			120	μs	
TLCLK Period	t_{TP}		250		μs	1
TLCLK Pulse Width	t_{TH}, t_{TL}	50			μs	
RST Pulse Width	t_{RST}	10			μs	
SLIP Pulse Width	t_{PW}	10			μs	
Sync/Reframe Time				30	ms	2

NOTES:

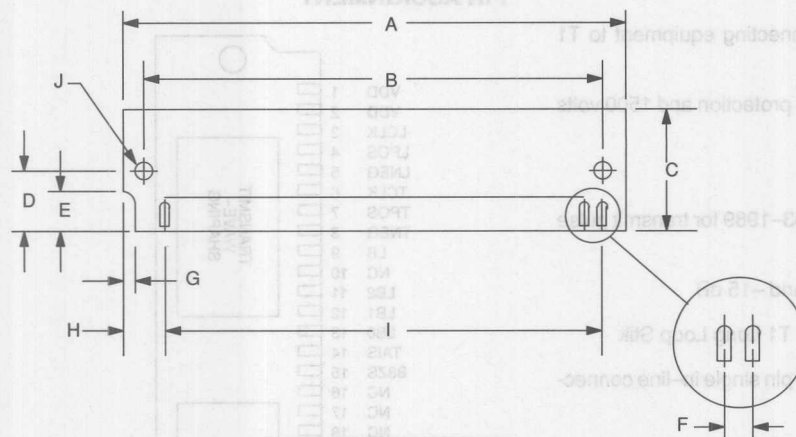
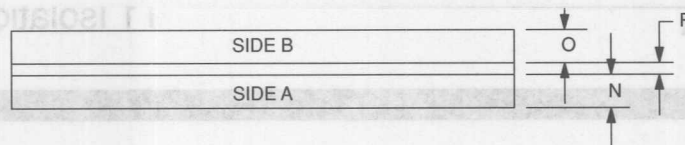
1. Must be accurate to ± 32 ppm for precise one second interval measurements.
2. Time necessary to sync to an error-free signal.



AC TIMING DIAGRAM Figure 5



T ISOLATION STIK



PKG	30-PIN	
DIM	MIN	MAX
A IN.	3.455	3.505
B IN.	3.229	3.239
C IN.	0.845	0.855
D IN.	0.395	0.405
E IN.	0.245	0.255
F IN.	0.100 BSC	
G IN.	0.075	0.085
H IN.	0.295	0.305
I IN.	2.900 BSC	
J IN.	0.120	0.130
N IN.		0.200
O IN.		0.145
P IN.		0.054

FEATURES

- Protected interface for connecting equipment to T1 lines
- Provides 800 volts of surge protection and 1000 volts of isolation
- FCC Part 68 registered
- Meets TR 82411 and T1-403-1089 for interface characteristics
- Line built out of 0.75, 1.5, 3.0, 6.0, 12.0, 24.0, 48.0, 96.0, 192.0, 384.0, 768.0, 1536.0, 3072.0, 6144.0, 12288.0, 24576.0, 49152.0, 98304.0, 196608.0, 393216.0, 786432.0, 1572864.0, 3145728.0, 6291456.0, 12582912.0, 25165824.0, 50331648.0, 100663296.0, 201326592.0, 402653184.0, 805306368.0, 1610612736.0, 3221225472.0, 6442450944.0, 12884901888.0, 25769803776.0, 51539607552.0, 103079215104.0, 206158430208.0, 412316860416.0, 824633720832.0, 1649267441664.0, 3298534883328.0, 6597069766656.0, 13194139533312.0, 26388279066624.0, 52776558133248.0, 105553116266496.0, 211106232532992.0, 422212465065984.0, 844424930131968.0, 1688849860263936.0, 3377699720527872.0, 6755399441055744.0, 13510798882111488.0, 27021597764222976.0, 54043195528445952.0, 108086391056891904.0, 216172782113783808.0, 432345564227567616.0, 864691128455135232.0, 1729382256910270464.0, 3458764513820540928.0, 6917529027641081856.0, 13835058055282163712.0, 27670116110564327424.0, 55340232221128654848.0, 110680464442257309696.0, 221360928884514619392.0, 442721857769029238784.0, 885443715538058477568.0, 1770887431076116955136.0, 3541774862152233910272.0, 7083549724304467820544.0, 14167099448608935641088.0, 28334198897217871282176.0, 56668397794435742564352.0, 113336795588871485128704.0, 226673591177742970257408.0, 453347182355485940514816.0, 906694364710971881029632.0, 1813388729421943762059264.0, 3626777458843887524118528.0, 7253554917687775048237056.0, 14507109835375550096474112.0, 29014219670751100192948224.0, 58028439341502200385896448.0, 116056878683004400771792896.0, 232113757366008801543585792.0, 464227514732017603087171584.0, 928455029464035206174343168.0, 1856910058928070412348686336.0, 3713820117856140824697372672.0, 7427640235712281649394745344.0, 14855280471424563298789490688.0, 29710560942849126597578981376.0, 59421121885698253195157962752.0, 118842243771396506390315925504.0, 237684487542793012780631851008.0, 475368975085586025561263702016.0, 950737950171172051122527404032.0, 1901475900342344102245054808064.0, 3802951800684688204490109616128.0, 7605903601369376408980219232256.0, 15211807202738752817960438464512.0, 30423614405477505635920876929024.0, 60847228810955011271841753858048.0, 121694457621910022543683507716096.0, 243388915243820045087367015432192.0, 486777830487640090174734030864384.0, 973555660975280180349468061728768.0, 1947111321950560360698936123457536.0, 3894222643901120721397872246915072.0, 7788445287802241442795744493830144.0, 15576890575604482885591488987660288.0, 31153781151208965771182977975320576.0, 62307562302417931542365955950641152.0, 124615124604835863084731911901282304.0, 249230249209671726169463823802564608.0, 498460498419343452338927647605129216.0, 996920996838686904677855295210258432.0, 1993841993677373809355710590420516864.0, 3987683987354747618711421180841033728.0, 7975367974709495237422842361682067456.0, 15950735949418990474845684723364134912.0, 31901471898837980949691369446728269824.0, 63802943797675961899382738893456539648.0, 127605887595351923798765477786913079296.0, 255211775190703847597530955573826158592.0, 510423550381407695195061911147652317184.0, 1020847100762815390390123822295304634368.0, 2041694201525630780780247644590609268736.0, 4083388403051261561560495289181218537472.0, 8166776806102523123120990578362437074944.0, 16333553612205046246241981156724874149888.0, 32667107224410092492483962313449748299776.0, 65334214448820184984967924626899496599552.0, 130668428897640369969935849253798993199104.0, 261336857795280739939871698507597986398208.0, 522673715590561479879743397015195972796416.0, 1045347431181122959759486794030391945592832.0, 2090694862362245919518973588060783891185664.0, 4181389724724491839037947176121567782371328.0, 8362779449448983678075894352243135564742656.0, 16725558898897967356151788704486271129485312.0, 33451117797795934712303577408972542258970624.0, 66902235595591869424607154817945084517941248.0, 133804471191183738849214309635890169035882496.0, 267608942382367477698428619271780338071764992.0, 535217884764734955396857238543560676143529984.0, 1070435769529469910793714477087121352287059968.0, 2140871539058939821587428954174242704574119936.0, 4281743078117879643174857908348485409148239872.0, 8563486156235759286349715816696970818296479744.0, 17126972312471518572699431633393941636592959488.0, 34253944624943037145398863266787883273185918976.0, 68507889249886074290797726533575766546371837952.0, 137015778499772148581595453067151533092743675904.0, 274031556999544297163190906134303066185487351808.0, 548063113999088594326381812268606132370974703616.0, 1096126227998177188652763624537212264741949407232.0, 2192252455996354377305527249074424529483898814464.0, 4384504911992708754611054498148849058967797628928.0, 8769009823985417509222108996297698117935595257856.0, 17538019647970835018444217992595396235871190515712.0, 35076039295941670036888435985190792471742381031424.0, 70152078591883340073776871970381584943484762062848.0, 140304157183766680147553743940763169886969524125696.0, 280608314367533360295107487881526339773939048251392.0, 561216628735066720590214975763052679547878096502784.0, 1122433257470133441180429951526105359095756193005568.0, 2244866514940266882360859903052210718191512386011136.0, 4489733029880533764721719806104421436383024772022272.0, 8979466059761067529443439612208842872766049544044544.0, 17958932119522135058886879224417685745532099088089088.0, 35917864239044270117773758448835371491064198176178176.0, 71835728478088540235547516897670742982128396352356352.0, 143671456956177080471095033795341485964256792704712704.0, 287342913912354160942190067590682971928513585409425408.0, 574685827824708321884380135181365943857027170818850816.0, 1149371655649416643768760270362731887714054341637701632.0, 2298743311298833287537520540725463775428108683275403264.0, 4597486622597666575075041081450927550856217366550806528.0, 9194973245195333150150082162901855101712434733101613056.0, 18389946490390666300300164325803710203424869466203226112.0, 36779892980781332600600328651607420406849738932406452224.0, 73559785961562665201200657303214840813699477864812904448.0, 147119571923125330402401314606429681627398955729625808896.0, 294239143846250660804802629212859363254797911459251617792.0, 588478287692501321609605258425718726509595822918503235584.0, 1176956575385002643219210516851437453019191645837006471168.0, 2353913150770005286438421033702874906038383291674012942336.0, 4707826301540010572876842067405749812076766583348025884672.0, 9415652603080021145753684134811499624153533166696051769344.0, 18831305206160042291507368269622999248307066333392103538688.0, 37662610412320084583014736539245998496614132666784207077376.0, 75325220824640169166029473078491996993228265333568414154752.0, 150650441649280338332058946156983993986456530667136828309504.0, 301300883298560676664117892313967987972913061334273656619008.0, 602601766597121353328235784627935975945826122668547313238016.0, 1205203533194242706656471569255871951891652245337094626476032.0, 2410407066388485413312943138511743903783304490674189252952064.0, 4820814132776970826625886277023487807566608981348378505904128.0, 9641628265553941653251772554046975615133217962696757011808256.0, 19283256531107883306503545108093951230266435925393514023616512.0, 38566513062215766613007090216187902460532871850787028047233024.0, 77133026124431533226014180432375804921065743701574056094466048.0, 154266052248863066452028360864751609842131487403148112188932096.0, 308532104497726132904056721729503219684262974806296224377864192.0, 617064208995452265808113443459006439368525949612592448755728384.0, 1234128417990904531616226886918012878737051899225184897511456768.0, 2468256835981809063232453773836025757474103798450369795022913536.0, 4936513671963618126464907547672051514948207596900739590045827072.0, 9873027343927236252929815095344103029896415193801479180091654144.0, 19746054687854472505859630190688206059792830387602958360183308288.0, 39492109375708945011719260381376412119585660775205916720366616576.0, 78984218751417890023438520762752824239171321550411833440733233152.0, 157968437502835780046877041525505648478342643100823666881466466304.0, 315936875005671560093754083051011296956685286201647333762932932608.0, 631873750011343120187508166102022593913370572403294667525865865216.0, 1263747500022686240375016332204045187826741144806589335051731730432.0, 2527495000045372480750032664408090375653482289613178670103463460864.0, 5054990000090744961500065328816180751306964579226357340206926921728.0, 10109980000181489923000130657632361502613929158452714680413853843456.0, 20219960000362979846000261315264723005227858316905429360827707686912.0, 40439920000725959692000522630529446010455716633810858721655415373824.0, 80879840001451919384001045261058892020911433267621717443310830747648.0, 161759680002903838768002090522117784041822866535243434886621661495296.0, 323519360005807677536004181044235568083645733070486869773243322990592.0, 647038720011615355072008362088471136167291466140973739546486645981184.0, 1294077440023230710144016724176942272334582932281947479092973291962368.0, 2588154880046461420288033448353884544669165864563894958185946583924736.0, 5176309760092922840576066896707769089338331729127789916371893167849472.0, 10352619520185845681152133793415538178676663458255579832743786335698944.0, 20705239040371691362304267586831076357353326916511159665487572671397888.0, 41410478080743382724608535173662152714706653833022319330975145342795776.0, 82820956161486765449217070347324305429413307666044638661950290685591552.0, 165641912322973530898434140694648610858826615332089277323900581371183104.0, 331283824645947061796868281389297221717653230664178554647801162742366208.0, 662567649291894123593736562778594443435306461328357109295602325484732416.0, 1325135298583788247187473125557188886870612922656714218591204650969464832.0, 2650270597167576494374946251114377773741225845313428437182409301938929664.0, 5300541194335152988749892502228755547482451690626856874364818603877859328.0, 10601082388670305977499785004457511094964903381253713748729637207755718656.0, 21202164777340611954999570008915022189929806762507427497459274415511437312.0, 42404329554681223909999140017830044379859613525014854994918548831022874624.0, 84808659109362447819998280035660088759719227050029709989837097662045749248.0, 169617318218724895639996560071320177519438454100059419979674195324091498496.0, 339234636437449791279993120142640355038876908200118839959348390648182996992.0, 678469272874899582559986240285280710077753816400237679918696781296365993984.0, 1356938545749799165119972480570561420155507632800475359837393562592731987968.0, 2713877091499598330239944961141122840311015265600950719674787125185463975936.0, 5427754182999196660479889922282245680622030531201901439349574250370927951872.0, 10855508365998393320959779844564491361244061062403802878699148500741855903744.0, 21711016731996786641919559689128982722488122124807605757398297001483711807488.0, 43422033463993573283839119378257965444976244249615211514796594002967423614976.0, 86844066927987146567678238756515930889952488499230423029593188005934847229952.0, 173688133855974293135356477513031861779904976998460846059186376011869694459904.0, 347376267711948586270712955026063723559809953996921692118372752023739388919808.0, 694752535423897172541425910052127447119619907993843384236745504047478777839616.0, 138950507084779434508285182010425

DALLAS

SEMICONDUCTOR

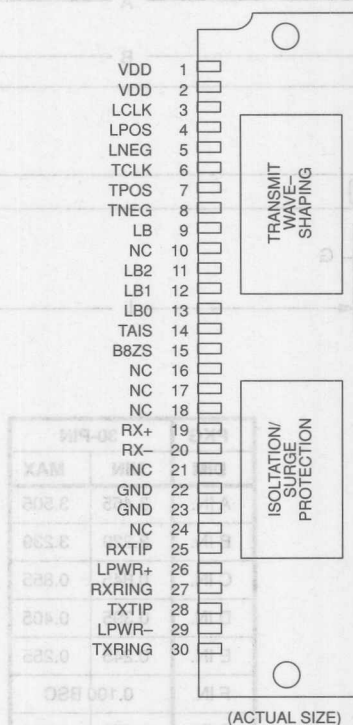
DS2290

T1 Isolation Stik

FEATURES

- Protected interface for connecting equipment to T1 lines
- Provides 800 volts of surge protection and 1500 volts of isolation
- FCC Part 68 registered
- Meets TR 62411 and T1.403–1989 for transmit pulse characteristics
- Line build outs of 0, –7.5, and –15 dB
- Companion to the DS2291 T1 Long Loop Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply
- Compatible with the DS2180A and DS2141A T1 Transceivers

PIN ASSIGNMENT



DESCRIPTION

The DS2290 T1 Isolation Stik provides all the surge and isolation protection that is necessary to connect a piece of equipment to a T1 line. It offers a function similar to that provided by a Data Access Arrangement (DAA) when a modem is connected to a phone line. The DS2290 is FCC Part 68 pre-registered so the user can connect equipment to T1 lines without any further testing or qualification. It contains onboard waveshaping

circuitry that creates transmit pulses meeting the latest T1 specifications including TR 62411 (Accunet* T1.5 Service Description and Interface Specifications, – December 1990) and T1.403–1989 (Carrier to Carrier Installation – DS1 Metallic Interface). Applications include Channel Service Units and similar equipment that requires a fully protected interface.

* Service mark of AT&T Communications

OVERVIEW

The DS2290 contains all the isolation and surge protection required to connect equipment to T1 lines. The Isolation Stik has a receive and a transmit section. (See Figure 1.) In the receive section, inputs RXTIP and RXRING are connected directly to the receive T1 twisted pair. These inputs are terminated at 100 ohms. The T1 signal received at RXTIP and RXRING is coupled through a 2:1 transformer and presented at the RX+ and RX- outputs. See Figure 2. There is a full 1500 volts of isolation between the Network Side pins and the Customer Side pins.

In the transmit section, data that is to be transmitted is sourced from either the TPOS and TNEG inputs or the LPOS and LNEG inputs. The Data Mux will transmit data at the TCLK rate from the TPOS and TNEG inputs if the LB pin is either tied low or left open. It will transmit data at the LCLK rate from the LPOS and LNEG inputs if the LB pin is tied high. In order to comply with the latest T1 standards, the clock presented at either TCLK or LCLK must be at a 1.544 MHz rate (± 32 ppm) and must not jitter beyond 0.05 unit intervals peak-to-peak (UIpp). TPOS and TNEG can be tied together if the source of the transmit data is in a NRZ format. The DS2290 will automatically sense that these inputs are tied together and will create a bipolar data stream from them. The same holds true for the LPOS and LNEG inputs.

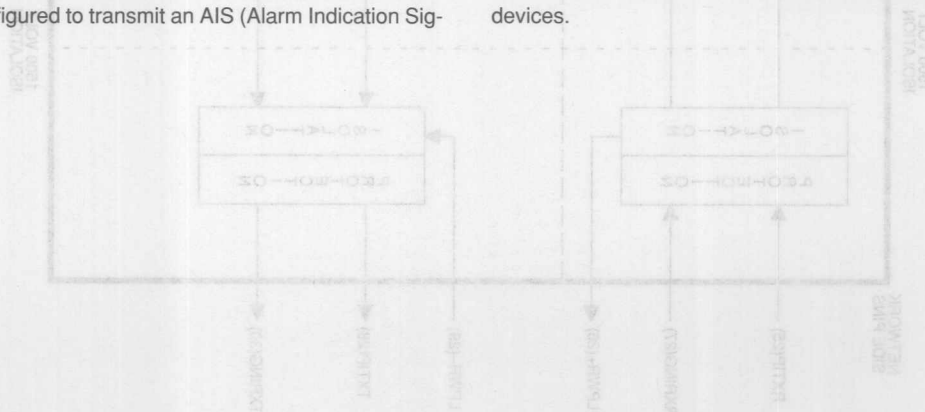
Data out of the Data Mux is passed to a B8ZS encoder and AIS generator. If the B8ZS pin is tied high, then the DS2290 will properly encode the transmit data stream for the B8ZS zero code suppression scheme. If the B8ZS pin is tied low or left open, the DS2290 will not encode the transmit data for B8ZS. Also, the DS2290 can be configured to transmit an AIS (Alarm Indication Sig-

nal). If the TAIS pin is tied high, the DS2290 will transmit an unframed, all ones signal at either the TCLK (LB=0) or LCLK (LB=1) rate.

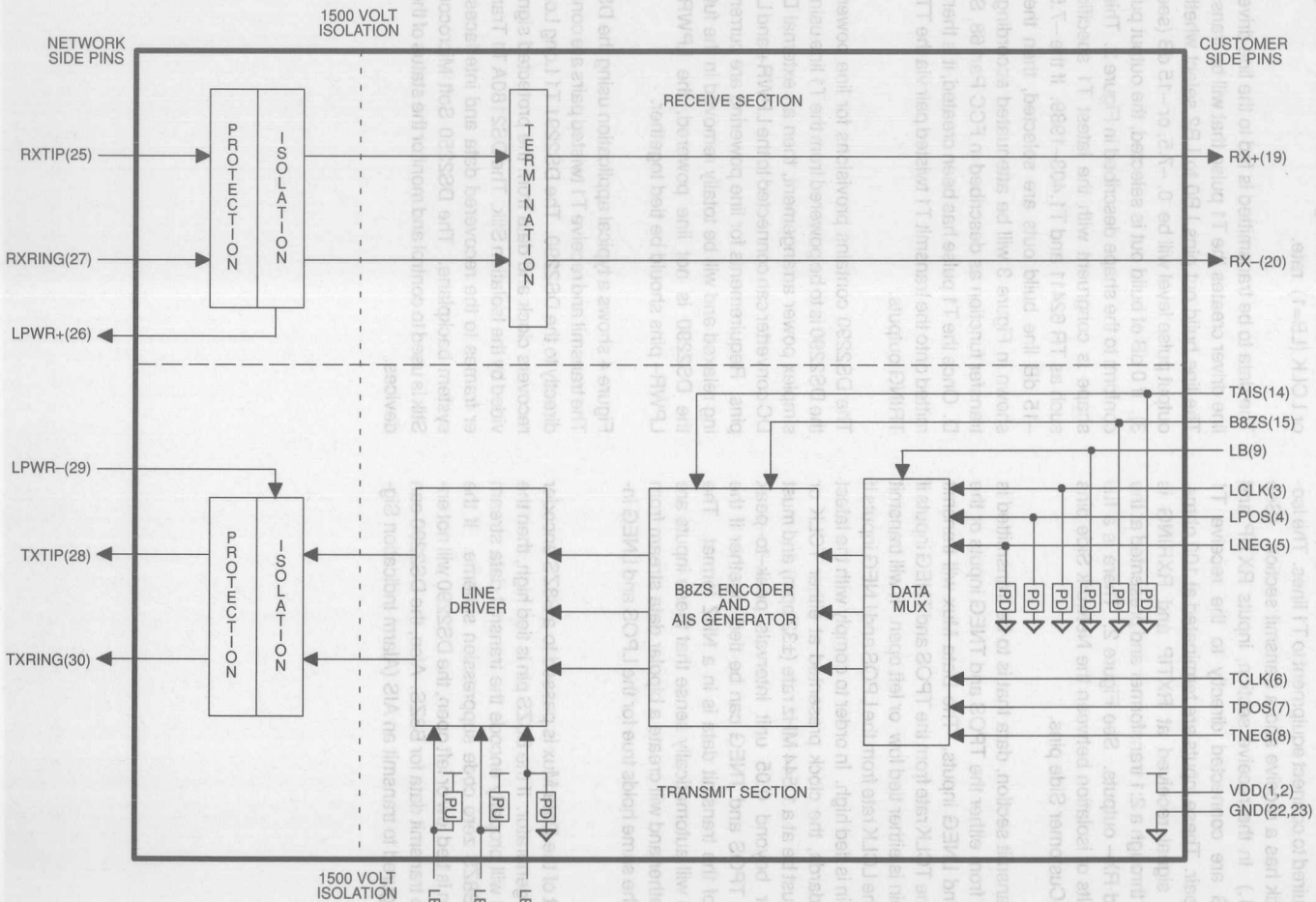
The data to be transmitted is fed to the line driver. The line driver creates the T1 pulse that will be transmitted. The line build out pins LB0 to LB2 select whether the output pulse level will be 0, -7.5, or -15 dB (see Table 3). If 0 dB of build out is selected, the output pulse will conform to the shape described in Figure 2. This pulse shape is congruent with the latest T1 specifications such as TR 62411 and T1.403-1989. If the -7.5 dB or -15 dB line build outs are selected, then the pulse shown in Figure 3 will be attenuated according to the transfer function as described in FCC Part 68, Subpart D. Once the T1 pulse has been created, it is then transmitted onto the transmit T1 twisted pair via the TTIP and TRING outputs.

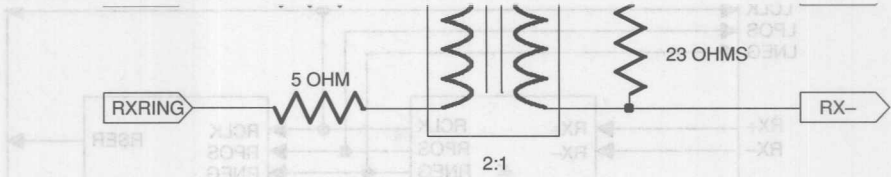
The DS2290 contains provisions for line powering. If the DS2290 is to be powered from the T1 line using a DC simplex power arrangement, then an external DC-to-DC converter can be connected to the LPWR+ and LPWR- pins. Requirements for line powering are currently being relaxed and will be totally removed in the future. If the DS2290 is not line powered, the LPWR+ and LPWR- pins should be tied together.

Figure 4 shows a typical application using the DS2290. The transmit and receive T1 twisted pairs are connected directly to the DS2290. The DS2291 T1 Long Loop Stik recovers clock and data from the protected signal provided by the Isolation Stik. The DS2180A T1 Transceiver frames to the recovered data and interfaces to the system backplane. The DS2250 Soft Microcontroller Stik is used to control and monitor the status of the other devices.

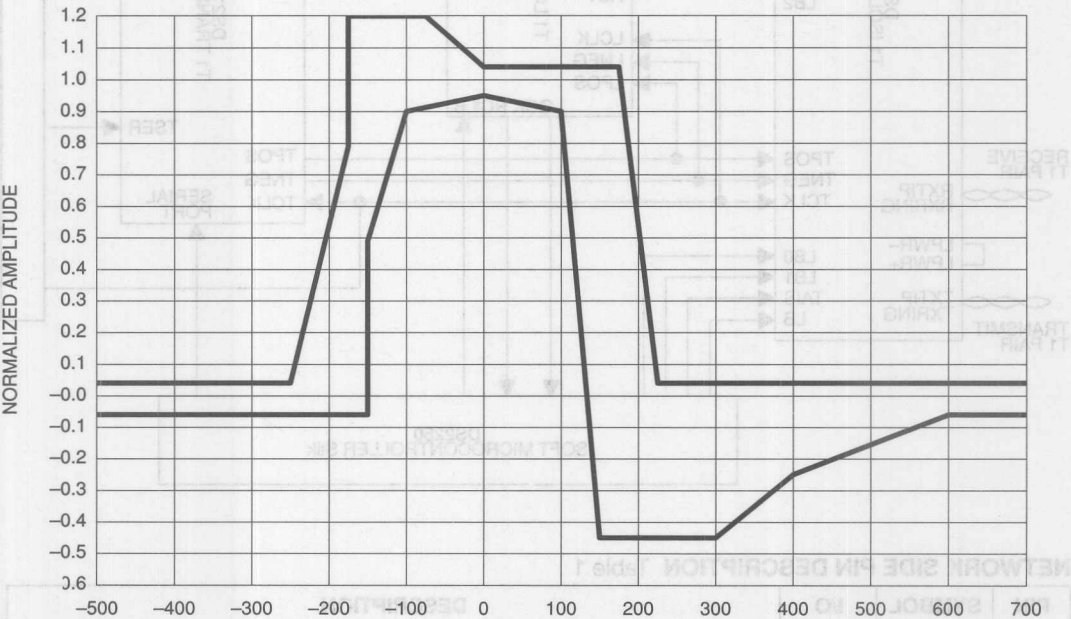


DS2290 BLOCK DIAGRAM Figure 1



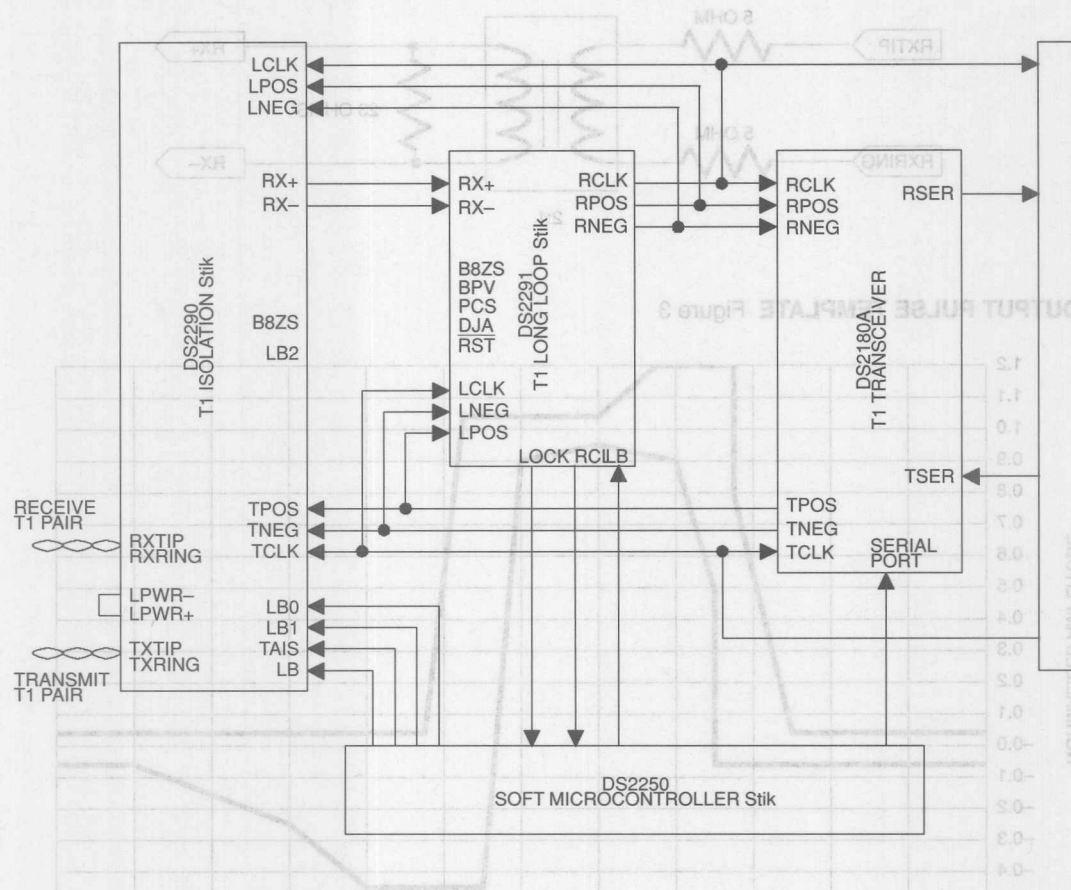


OUTPUT PULSE TEMPLATE Figure 3



25	RXRING	I	Receive T1p and Ring Inputs. Connects directly to the receive T1 twisted pair. These inputs are coupled and terminated at 100 ohms. See Figure 3.
26	TXRING	O	Transmit T1p and Ring Outputs. Connects directly to the transmit T1 twisted pair. Output signal level is programmable via the L80 to L82 pins. (See Table 3).
28	LPWR+	-	Loop Power Connections. These pins connect to the internal center-taps of the transmit and receive transformers. They provide access to the DC power on the T1 line (may not be provided by carrier in the future). The together it no simplex power management is needed.

TYPICAL DS2290 APPLICATION Figure 4



NETWORK SIDE PIN DESCRIPTION Table 1

PIN	SYMBOL	I/O	DESCRIPTION
25 27	RXTIP RXRING	I	Receive Tip and Ring Inputs. Connects directly to the receive T1 twisted pair. These inputs are transformer coupled and terminated at 100 ohms. See Figure 2.
28 30	TX TIP TXRING	O	Transmit Tip and Ring Outputs. Connects directly to the transmit T1 twisted pair. Output signal level is programmable via the LB0 to LB2 pins. (See Table 3.)
26 29	LPWR+ LPWR-	-	Loop Power Connections. These pins connect to the internal center-taps of the transmit and receive transformers. They provide access to the DC power on the T1 line (may not be provided by carriers in the future). Tie together if no simplex power arrangement is needed.

CUSTOMER SIDE PIN DESCRIPTION Table 2

PIN	SYMBOL	I/O	DESCRIPTION
1,2	V _{DD}	—	Positive Supply. 5.0 Volts.
3	LCLK	I	Loopback Clock. Clock for loopback data. Internally pulled low by 100K Ω .
4 5	LPOS LNEG	I	Loopback Bipolar Data. Sampled on the falling edge of LCLK if LB is tied high. Internally pulled low by 100K Ω .
6	TCLK	I	Transmit Clock. Apply a 1.544 MHz (± 32 ppm) clock here.
7 8	TPOS TNEG	I	Transmit Bipolar Data. Data that is to be transmitted. Sampled on the falling edge of TCLK when LB is tied low or left open. TPOS and TNEG can be tied together for an NRZ data input.
9	LB	I	Loopback Enable. Tie high to transmit data from LPOS and LNEG; tie low or leave open to transmit data from TPOS and TNEG. Internally pulled low by 100K ohm.
11 12 13	LB2 LB1 LB0	I	Line Build Out Select. State determines whether the transmitted signal has 0, -7.5, or -15 dB of line build out. See Table 3. LB0 and LB1 are internally pulled high by 100K Ω ; LB2 is pulled low by 100K Ω . If all three build out pins are left open, the default state is 0 dB.
14	TAIS	I	Transmit Alarm Indication Signal. Tie high to transmit an unframed all ones signal at either the TCLK (LB=0) or LCLK (LB=1) rate. Internally pulled low by 100K Ω .
15	B8ZS	I	B8ZS Enable. Tie high to enable B8ZS encoding; tie low or leave open to disable B8ZS encoding. Internally pulled low by 100K Ω .
19 20	RX+ RX-	O	Receive Analog Output. Protected differential T1 signal output here.
22,23	GND	—	Ground. 0.0 volts.

NOTE: Do not connect any signal to pins 10, 16, 17, 18, 21, and 24.

LINE BUILD OUT SELECTS Table 3

LINE BUILD OUT SELECTS	LB0	LB1	LB2
0 dB	1	1	0
-7.5 dB	1	0	0
-15 dB	0	1	0

SINGLE IN-LINE CONNECTOR

The DS2290 is designed to connect directly into a 30-position single in-line connector. These connectors are available from a number of vendors.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground (Customer Side pins only)	-0.3V to $V_{CC} + 0.3V$
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	3
Logic 0	V_{IL}	-0.3		+0.8	V	3
Supply	V_{DD}	4.75		5.25	V	

CAPACITANCE

($t_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_{IN}		30		pF	3
Output Capacitance	C_{OUT}		50		pF	3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $V_{DD}=5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		60	80	mA	1
Input Leakage	I_I	-100		+100	μA	2,3
Output Current (2.4V)	I_{OH}	-1.0			mA	3
Output Current (0.4V)	I_{OL}	+4.0			mA	3

NOTES:

1. $TCLK = 1.544\text{ MHz}$; $V_{DD} = 5.25V$; outputs open; driving all ones into 6000 feet of 22 AWG.
2. $V_{SS} < V_{IN} < V_{DD}$.
3. Does not apply to any of the network side pins nor RX+ or RX-.

ANALOG ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Impedance at RXTIP and RXRING at 772 KHz	I _Z	95	100	105	ohms	1
Transmit Jitter Generation	J _{GEN}			0.03	U _{Ipp}	2
Transmit Pulse Amplitude	P _{AMP}	2.5	3.0	3.5	V _{pk}	3,4,5
Pulse Width Balance @ 50%	PW _{BAL}		1	10	ns	3,6
Pulse Amplitude Balance	PA _{BAL}		10	100	mV	3,6
Power Level at 772 KHz	P _{LVL}	12		19	dBm	7

NOTES:

1. RX+ and RX- left open circuited.
2. Jitter present at TXTIP and TXRING with no jitter at TCLK (LB=0) or LCLK (LB=1).
3. Measured with 100 ohm (±5%) termination at TXTIP and TXRING.
4. Measured directly at TXTIP and TXRING with 0 dB of line build out.
5. Pulse shape meets template in Figure 3 over temperature and voltage.
6. Measured over 17 consecutive pulses.
7. Measured in a 2 KHz to 3 KHz band about 772 KHz; power level in a 2 to 3 KHz band at 1.544 MHz is at least 25 dB lower.

DIGITAL ELECTRICAL CHARACTERISTICS

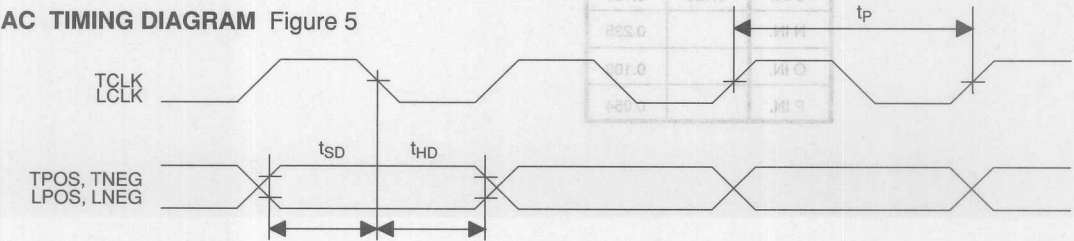
(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t _p		±32		ppm	1
TPOS, TNEG or LPOS, LNEG Setup Time to TCLK or LCLK Falling	t _{SD}	50			ns	
TPOS, TNEG or LPOS, LNEG Hold Time from TCLK or LCLK Falling	t _{HD}	50			ns	

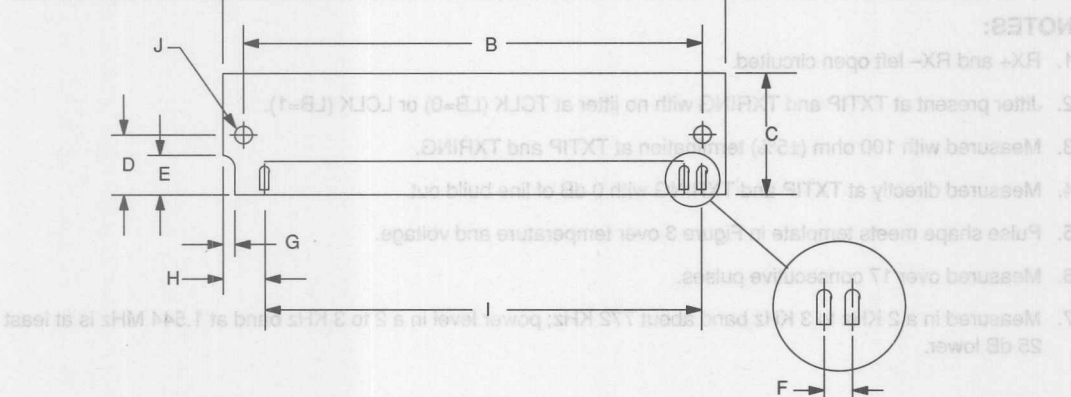
NOTE:

1. Necessary to meet current carrier and FCC specifications.

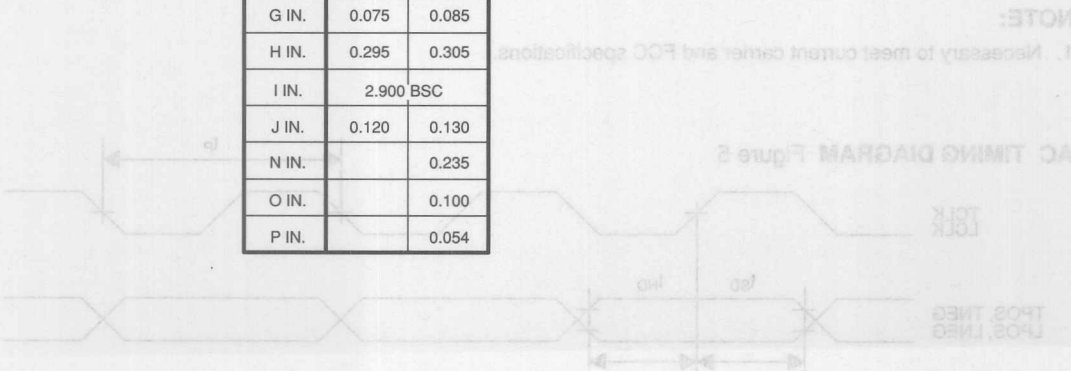
AC TIMING DIAGRAM Figure 5



1	ohms	105	100	95	15	Input Impedance at RXTP and RXRING at 775 KHz
2	Uqlp	0.63				Transmit Filter Gain
3,4,5	Vpk	3.5				Transmit Pulse Amplitude
3,6	ns	10				Pulse Width Balance
3,8	mV	100	10			Pulse Amplitude Balance
7	dBm	19				Power Level at 775 KHz



PARAMETER	SYMBOL	MIN	30-PIN		UNITS	NOTES
			DIM	MIN		
CLK Period	T_{CLK}		A IN.	3.455	3.505	1
TP05, TNEG or LP05, LNEG Setup Time to TCLK or LCLK	t_{SU}	50	B IN.	3.229	3.239	
Falling			C IN.	0.845	0.855	
TP05, TNEG or LP05, LNEG Hold Time from TCLK or LCLK	t_{HD}	50	D IN.	0.395	0.405	
Falling			E IN.	0.245	0.255	
			F IN.	0.100	BSC	
			G IN.	0.075	0.085	
			H IN.	0.295	0.305	
			I IN.	2.900	BSC	
			J IN.	0.120	0.130	
			N IN.		0.235	
			O IN.		0.100	
			P IN.		0.054	



DALLAS SEMICONDUCTOR

FEATURES

- Recovers clock and data off of T1 lines from 0 to 6,000 feet in length
- +0 to -30dB SX receiver sensitivity
- Built-in Automatic Line Build Out (ALBO) circuitry; no tuning or external components required
- Dejitters the recovered clock and data
- Meets TR 62411 (Dec. 1990) for jitter tolerance and attenuation
- Companion to the DS2290 T1 Isolation Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply
- Compatible with the DS2180A or DS2141A T1 Transceivers

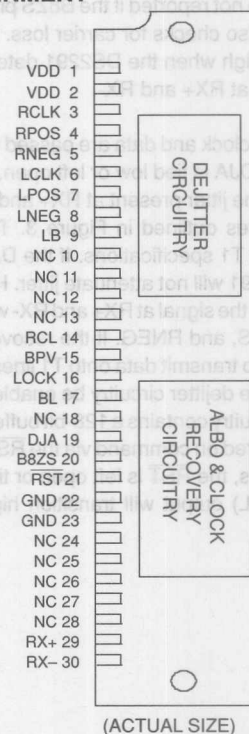
DESCRIPTION

The DS2291 T1 Long Loop Stik contains all the circuitry necessary to recover clock and data from a T1 line. The DS2291 contains an Automatic Line Build Out (ALBO) circuit that allows it to adapt to T1 lines varying in length from 0 to 6,000 feet. It also will dejitter the recovered clock and data according to the jitter attenuation curves outlined in AT&T Communications Document TR 62411 (Accunet* T1.5 Service Description and Interface specification - December 1990). Applications area include Channel Service Units (CSU), T1 monitoring equipment, and T1 test equipment.

* Service mark of AT&T Communications

DS2291 T1 Long Loop Stik

PIN ASSIGNMENT

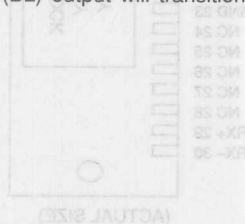


OVERVIEW

The DS2291 contains onboard ALBO circuitry that allows it to recover clock and data from T1 lines up to 6,000 feet in length. (See Figure 1.) Unlike alternative methods of clock and data recovery from T1 lines, the DS2291 does not require any tuning, nor does it need any additional external circuitry. The state of the LOCK pin indicates whether the DS2291 has been able to phase and frequency lock to the incoming T1 signal. If the LOCK pin is high, the DS2291 is properly locked onto the incoming signal. The DS2291 meets the latest T1 specification for jitter tolerance. The jitter tolerance curve in Figure 2 is applicable over the full dynamic input range of the DS2291.

Once the Long Loop Stik has recovered data from the T1 line, it can decode B8ZS code words and check for bipolar violations and carrier loss. If the B8ZS pin is tied high, the DS2291 will automatically replace incoming B8ZS code words with eight zeros. If the B8ZS pin is tied low or left open, no replacement occurs. Bipolar violations are reported via the BPV pin. The BPV pin will transition high for a full T1 bit period (648 ns) each time a violation is detected. Bipolar violations inherent in B8ZS code words are not reported if the B8ZS pin is tied high. The DS2291 also checks for carrier loss. The RCL pin will transition high when the DS2291 detects 192 consecutive zeros at RX+ and RX-.

The recovered clock and data are passed to the dejitter circuitry. If the DJA is tied low or left open, the DS2291 will attenuate the jitter present at RX+ and RX- according to the curves outlined in Figure 3. These curves meet the latest T1 specifications. If the DJA pin is tied high, the DS2291 will not attenuate jitter. Hence, all the jitter inherent in the signal at RX+ and RX- will be passed to RCLK, RPOS, and RNEG. If the recovered clock at RCLK is used to transmit data onto T1 lines, it is recommended that the dejitter circuitry be enabled (DJA = 0). The dejitter circuitry contains a 128-bit buffer. This buffer can be recentered on command via the $\overline{\text{RST}}$ pin. In normal applications, the $\overline{\text{RST}}$ is left open or tied high. The Buffer Limit (BL) output will transition high when the



OVERVIEW

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DS2291 is receiving more than 120 unit intervals peak-to-peak (Ulp) of jitter at RX+ and RX-. As long as the incoming jitter is less than 120Ulp, the BL pin will remain low.

The DS2291 contains a data mux that allows data to be routed from either the T1 recovery circuitry or from a local source. The mux is helpful locating faults in a system. For example, it could be used to implement a "local" loopback.

Two typical applications with the DS2291 are shown in Figure 4 and Figure 5. In both applications, the DS2291 is used to recover data from T1 lines up to 6,000 feet in length. The application in Figure 4 is with an unprotected interface; it might be used in T1 test equipment. The application in Figure 5 is with the DS2290 T1 Isolation Stik, which provides all the necessary protection as required by FCC Part 68. This could be used in a Channel Service Unit (CSU) or in similar types of equipment in which full surge and isolation protection is required.

SINGLE IN-LINE CONNECTOR

The DS2291 is designed to connect directly into a 30-pin single in-line connector. These connectors are available from a number of vendors.

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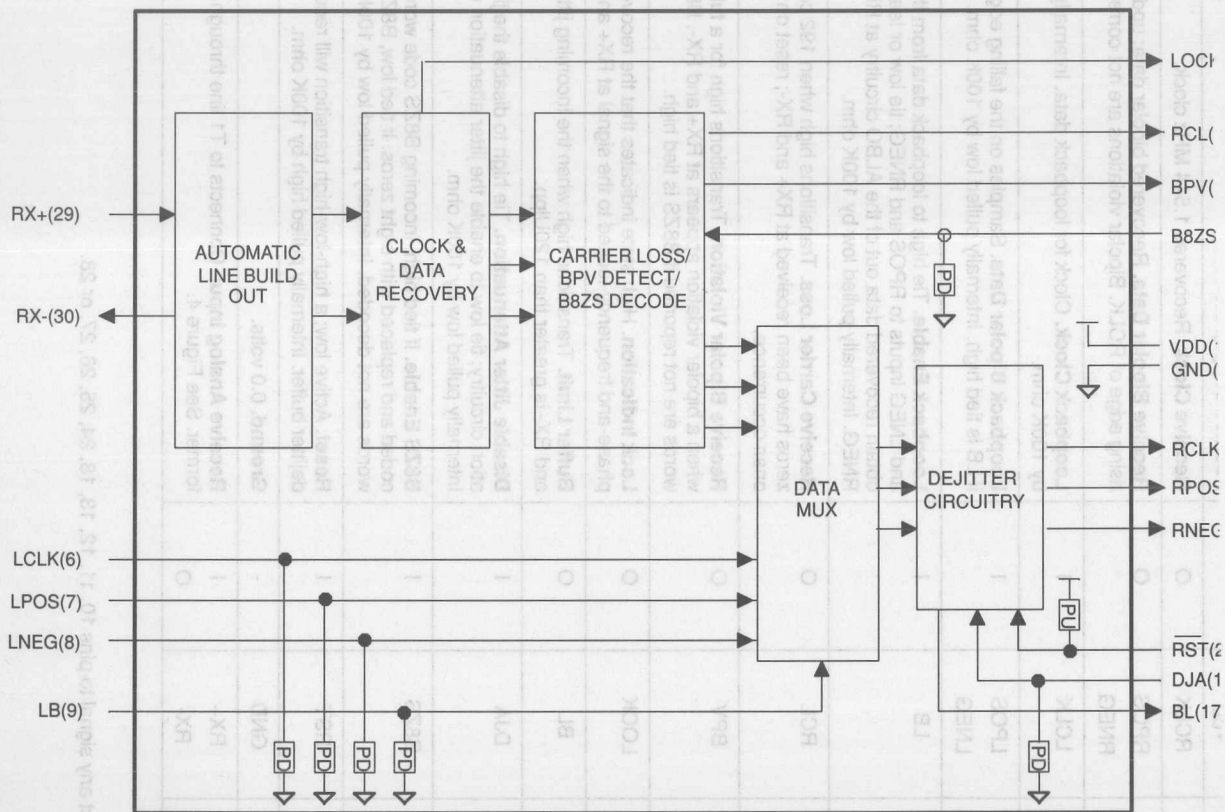
* Service mark of AT&T Communications

PIN DESCRIPTION Table 1

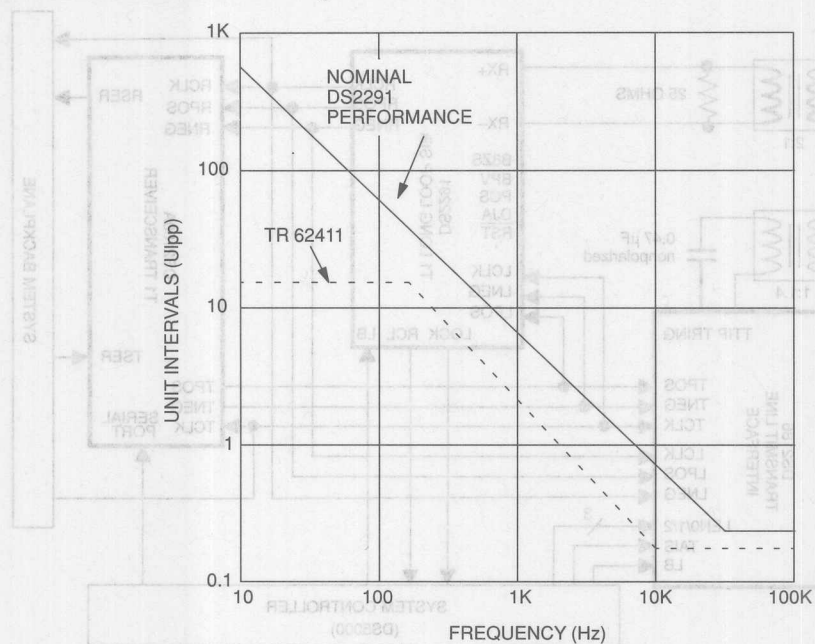
PIN	SYMBOL	I/O	DESCRIPTION
1,2	V _{DD}	-	Positive Supply. 5.0 volts.
3	RCLK	O	Receive Clock. Recovered 1.544 MHz clock.
4	RPOS	O	Receive Bipolar Data. Recovered bipolar data; updated on the rising edge of RCLK. Bipolar violations are not corrected.
5	RNEG		
6	LCLK	I	Loopback Clock. Clock for loopback data. Internally pulled low by 100K ohm.
7	LPOS	I	Loopback Bipolar Data. Samples on the falling edge of LCLK if LB is tied high. Internally pulled low by 100K ohm.
8	LNEG		
9	LB	I	Loopback Enable. Tie high to loopback data from the LPOS and LNEG inputs to RPOS and RNEG; tie low or leave open to obtain recovered data out of the ALBO circuitry at RPOS and RNEG. Internally pulled low by 100K ohm.
14	RCL	O	Receive Carrier Loss. Transitions high when 192 consecutive zeros have been received at RX+ and RX-; reset on the next ones occurrence.
15	BPV	O	Receive Bipolar Violation. Transitions high for a full bit period when a bipolar violation appears at RX+ and RX-. B8ZS code words are not reported if B8ZS is tied high.
16	LOCK	O	Lock Indication. High state indicates that the recovery circuit is phase-and frequency-locked to the signal at RX+ and RX-.
17	BL	O	Buffer Limit. Transitions high when the incoming jitter at RX+ and RX- is greater than 120Upp.
19	DJA	I	Disable Jitter Attenuation. Tie high to disable the jitter attenuation circuitry; tie low to enable the jitter attenuation circuitry. Internally pulled low by 100K ohm.
20	B8ZS	I	B8ZS Enable. If tied high, incoming B8ZS code words are decoded and replaced with eight zeros. If tied low, B8ZS code words are not decoded. Internally pulled low by 100K ohm.
21	RST	I	Reset. Active low; a high-low-high transition will recenter the dejitter buffer. Internally pulled high by 100K ohm.
22, 23	GND	-	Ground. 0.0 volts.
29	RX+	I	Receive Analog Input. Connects to T1 line through a 2:1 transformer. See Figure 4.
30	RX-	O	

NOTE:

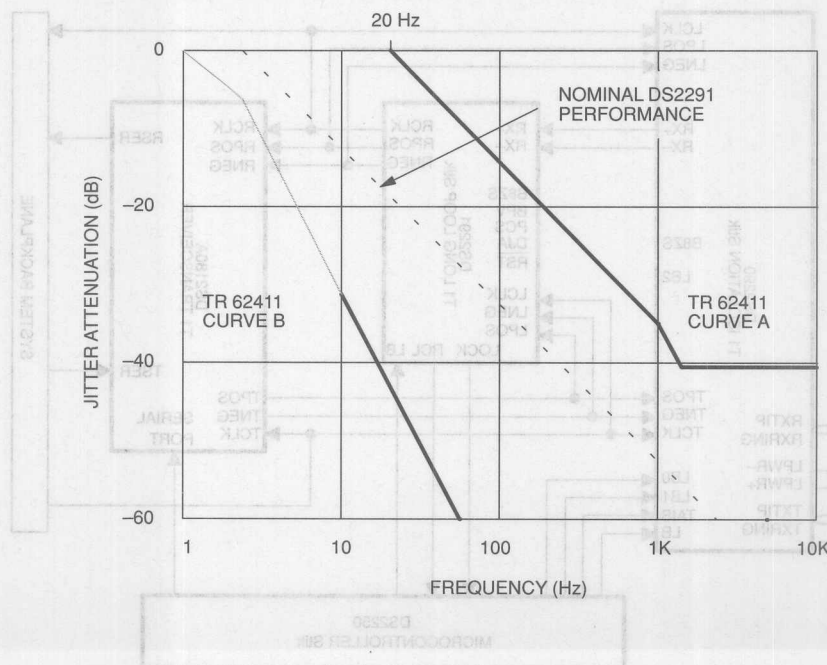
Do not connect any signal to pins 10, 11, 12, 13, 18, 24, 25, 26, 27, or 28.



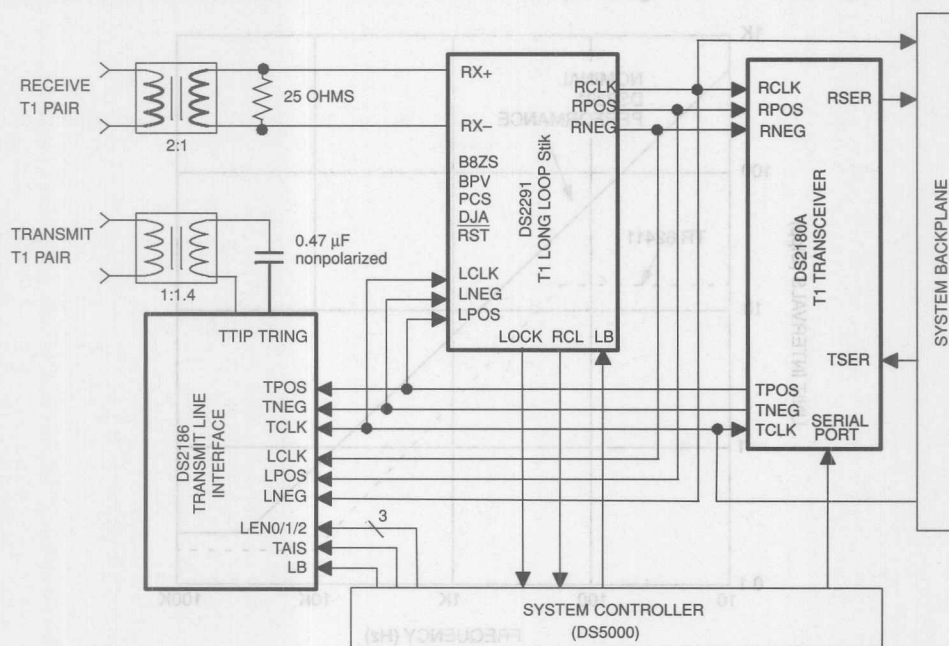
DS2291 JITTER TOLERANCE Figure 2



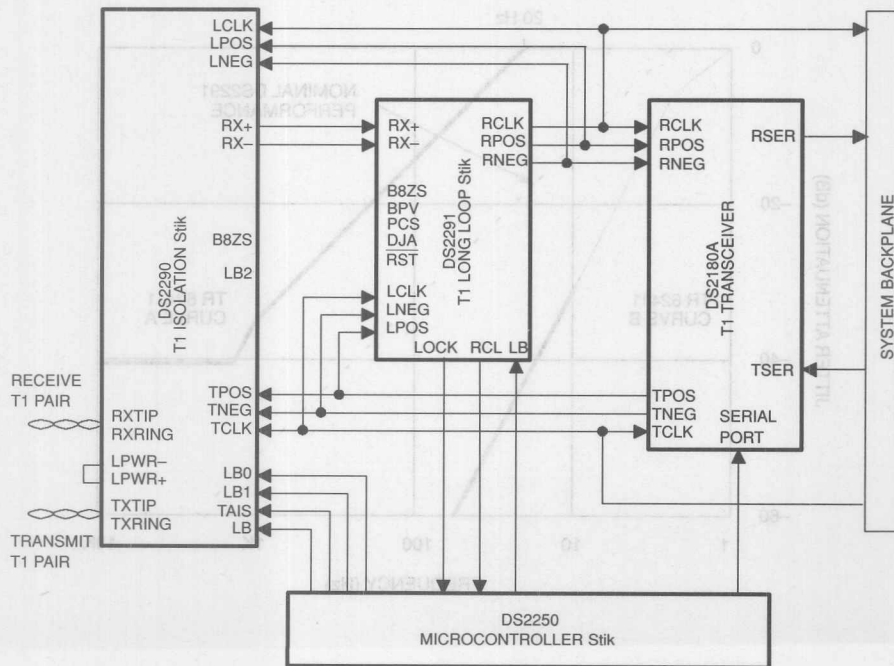
DS2291 JITTER ATTENUATION PERFORMANCE Figure 3



DS2291 APPLICATION (UNISOLATED INTERFACE) Figure 4



DS2291 APPLICATION (ISOLATED INTERFACE) Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground

-0.3V to $V_{CC} + 0.3V$

Operating Temperature

0°C to 70°C

Storage Temperature

-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC} + 0.3$	V	3, 4
Logic 0	V_{IL}	-0.3		+0.8	V	3, 4
Supply	V_{DD}	4.75		5.25	V	

CAPACITANCE(t_A=25°C)

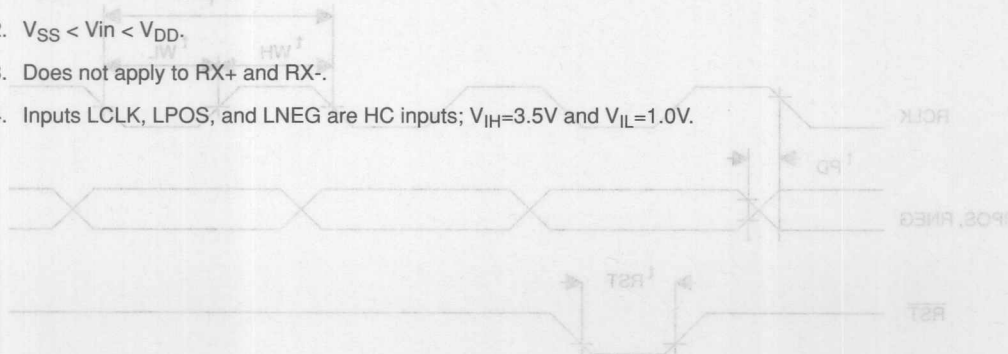
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			30	pF	3
Output Capacitance	C_{OUT}			50	pF	3

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		40	50	mA	1
Input Leakage	I_I	-100		+100	μA	2, 3
Output Current (2.4V)	I_{OH}	-1.0			mA	3
Output Current (0.4V)	I_{OL}	+4.0			mA	3

NOTES:

1. $V_{DD} = 5.25V$; output open.
2. $V_{SS} < V_{in} < V_{DD}$.
3. Does not apply to RX+ and RX-.
4. Inputs LCLK, LPOS, and LNEG are HC inputs; $V_{IH}=3.5V$ and $V_{IL}=1.0V$.



LPOS, LNEG Setup to LCLK Falling	t_{SD}	50			ns	
LPOS, LNEG Hold from LCLK Falling	t_{HD}	50			ns	
Propagation Delay from RCLK to RPOS, RNEG Valid	t_{PD}			50	ns	
RCLK Period	t_P		648		ns	
RCLK Pulse Width	t_{WL}, t_{WH}		324		ns	
RST Pulse Width	t_{RST}	1			μs	

ANALOG ELECTRICAL CHARACTERISTICS

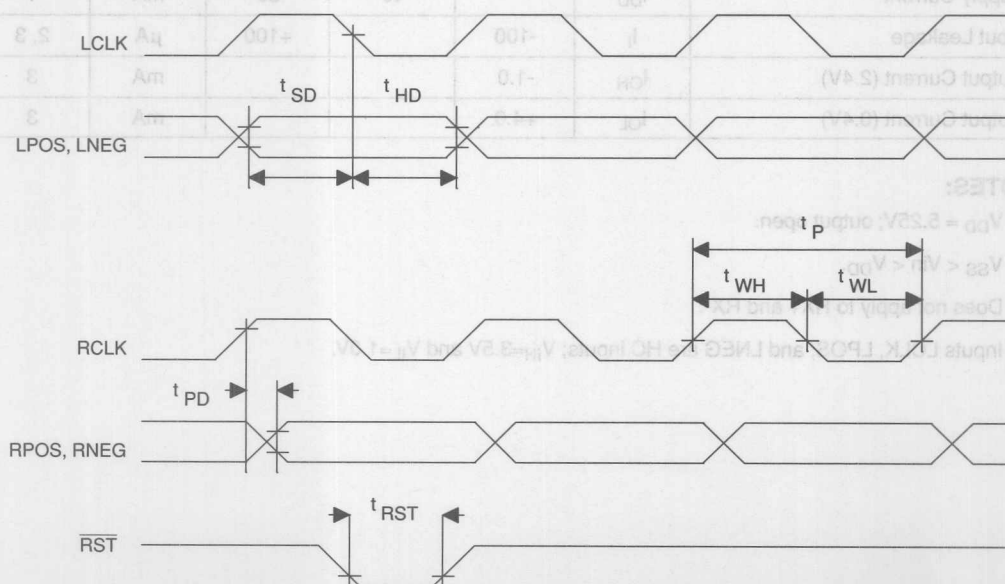
(0°C to 70°C; $V_{DD} = 5V \pm 5\%$)

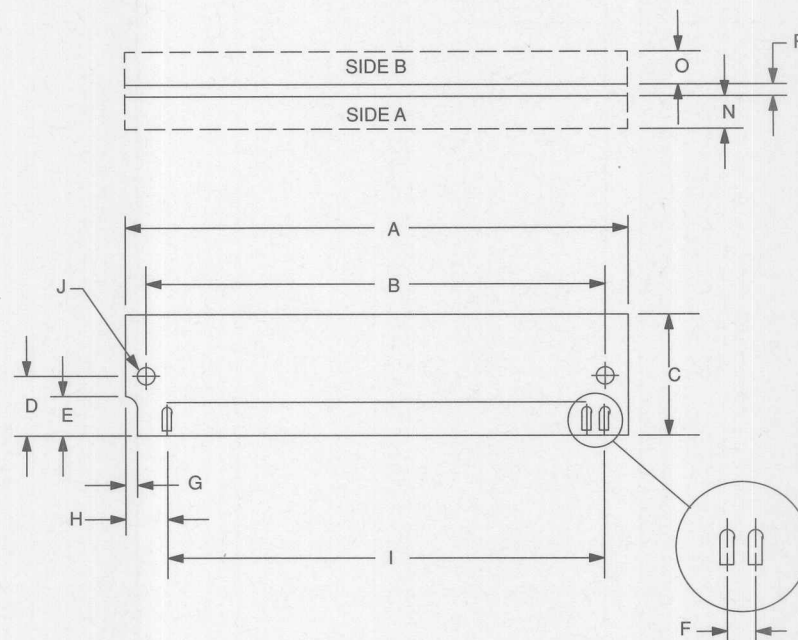
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Signal Range	V_{IR}	-30		+0	dBSX	1
Input Impedance at 772 KHz	Z_{IN}		1100		ohms	1

NOTE:

1. dBSX = 3Vpk; signal defined at the primary side of a 2:1 transformer with the secondary shunted by 25 Ω and connected to RX+ and RX- (see Figure 4 for an example).

AC TIMING DIAGRAM Figure 6





PKG	30-PIN	
DIM	MIN	MAX
A IN.	3.455	3.505
B IN.	3.229	3.239
C IN.	0.845	0.855
D IN.	0.395	0.405
E IN.	0.245	0.255
F IN.	0.100	BSC
G IN.	0.075	0.085
H IN.	0.295	0.305
I IN.	2.900	BSC
J IN.	0.120	0.130
N IN.		0.180
O IN.		0.115
P IN.		0.054

